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April 2010

FDZ375P

P-Channel 1.5 V Specified PowerTrench $^{(\!R\!)}$ Thin WL-CSP MOSFET -20 V, -3.7 A, 78 m Ω

Features

- Max $r_{DS(on)}$ = 78 m Ω at V_{GS} = -4.5 V, I_D = -2.0 A
- Max $r_{DS(on)}$ = 92 m Ω at V_{GS} = -2.5 V, I_D = -1.5 A
- Max $r_{DS(on)} = 112 \text{ m}\Omega$ at $V_{GS} = -1.8 \text{ V}$, $I_D = -1.0 \text{ A}$
- Max $r_{DS(on)}$ = 150 m Ω at V_{GS} = -1.5 V, I_D = -1.0 A
- Occupies only 1.0 mm² of PCB area. Less than 30% of the area of 2 x 2 BGA
- Ultra-thin package: less than 0.4 mm height when mounted to PCB
- RoHS Compliant

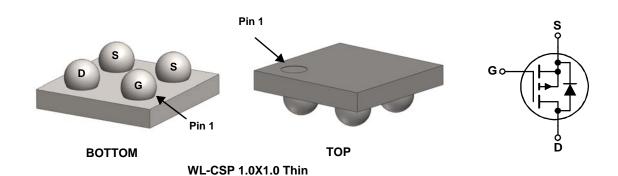


General Description

Designed on Fairchild's advanced 1.5 V PowerTrench® process with state of the art "fine pitch" Thin WLCSP packaging process, the FDZ375P minimizes both PCB space and $r_{\text{DS}(\text{on})}.$ This advanced WLCSP MOSFET embodies a breakthrough in packaging technology which enables the device to combine excellent thermal transfer characteristics, ultra-low profile packaging, low gate charge, and low $r_{\text{DS}(\text{on})}.$

Applications

- Battery management
- Load switch
- Battery protection



MOSFET Maximum Ratings T_A = 25 °C unless otherwise noted

Symbol	Param	eter		Ratings	Units
V _{DS}	Drain to Source Voltage			-20	V
V _{GS}	Gate to Source Voltage			±8	V
	-Continuous	T _A = 25°C	(Note 1a)	-3.7	^
^I D	-Pulsed			-12	A
D	Power Dissipation	T _A = 25°C	(Note 1a)	1.7	W
P_{D}	Power Dissipation	T _A = 25°C	(Note 1b)	0.5	VV
T _J , T _{STG}	Operating and Storage Junction Temperature Range			-55 to +150	°C

Thermal Characteristics

$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1a)	75	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1b)	260	C/VV

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
N	FDZ375P	WL-CSP 1.0X1.0 Thin	7 "	8 mm	5000 units

Electrical Characteristics $T_J = 25$ °C unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Тур	Max	Units
Off Chara	cteristics					
BV _{DSS}	Drain to Source Breakdown Voltage	$I_D = -250 \mu A, V_{GS} = 0 V$	-20			V
$\frac{\Delta BV_{DSS}}{\Delta T_{J}}$	Breakdown Voltage Temperature Coefficient	I_D = -250 μ A, referenced to 25 °C		-12		mV/°C
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} = -16 V, V _{GS} = 0 V			-1	μΑ
I_{GSS}	Gate to Source Leakage Current	$V_{GS} = \pm 8 \text{ V}, V_{DS} = 0 \text{ V}$			±100	nA

On Characteristics

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}, I_{D} = -250 \mu A$	-0.3	-0.5	-1.2	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	I_D = -250 μ A, referenced to 25 °C		2		mV/°C
	$V_{GS} = -4.5 \text{ V}, I_D = -2.0 \text{ A}$		65	78		
	Static Drain to Source On Resistance	$V_{GS} = -2.5 \text{ V}, I_D = -1.5 \text{A}$		77	92	mΩ
rno()		$V_{GS} = -1.8 \text{ V}, I_D = -1.0 \text{ A}$		92	112	
r _{DS(on)}		$V_{GS} = -1.5 \text{ V}, I_D = -1.0 \text{ A}$		112	150	11132
		$V_{GS} = -4.5 \text{ V}, I_D = -2.0 \text{ A},$ $T_J = 125^{\circ}\text{C}$		98	143	
9 _{FS}	Forward Transconductance	$V_{DD} = -5 \text{ V}, I_{D} = -3.3 \text{ A}$		11		S

Dynamic Characteristics

C _{iss}	Input Capacitance	V 40 V V 0 V	650	865	pF
C _{oss}	Output Capacitance	$V_{DS} = -10 \text{ V}, V_{GS} = 0 \text{ V},$ f = 1 MHz	110	145	pF
C _{rss}	Reverse Transfer Capacitance	1 - 1 1/11/12	95	150	pF

Switching Characteristics

t _{d(on)}	Turn-On Delay Time		5.3	11	ns
t _r	Rise Time	V _{DD} = -10 V, I _D = -3.3 A,	8.2	15	ns
t _{d(off)}	Turn-Off Delay Time	$V_{GS} = -4.5 \text{ V}, R_{GEN} = 6 \Omega$	138	221	ns
t _f	Fall Time		84	124	ns
Q_g	Total Gate Charge	V 45VV 40V	11	15	nC
Q_{gs}	Gate to Source Charge	$V_{GS} = -4.5 \text{ V}, V_{DD} = -10 \text{ V},$ $I_{D} = -3.3 \text{ A}$	0.8		nC
Q_{gd}	Gate to Drain "Miller" Charge	ID = -0.0 A	3		nC

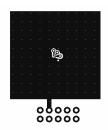
Drain-Source Diode Characteristics

I _S	Maximum Continuous Drain-Source Diode Forward Current				-1.1	Α
V_{SD}	Source to Drain Diode Forward Voltage	$V_{GS} = 0 \text{ V}, I_{S} = -1.3 \text{ A}$ (Note 2)		-0.7	-1.2	V
t _{rr}	Reverse Recovery Time	-I _E = -3.3 A, di/dt = 100 A/μs		68	109	ns
Q _{rr}	Reverse Recovery Charge	i _F = -3.3 A, αί/αι = 100 A/μS		43	69	nC

Notes

Notes.

1. R_{0JA} is determined with the device mounted on a 1 in² pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material. R_{0JC} is guaranteed by design while R_{0CA} is determined by the user's board design.



a. 75 °C/W when mounted on a 1 in² pad of 2 oz copper.



b. 260 °C/W when mounted on a minimum pad of 2 oz copper.

^{2.} Pulse Test: Pulse Width < $300\mu s$, Duty cycle < 2.0%.

Typical Characteristics T_J = 25°C unless otherwise noted

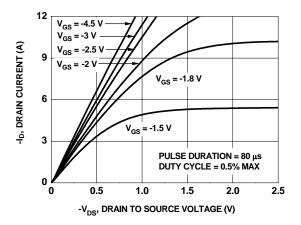


Figure 1. On Region Characteristics

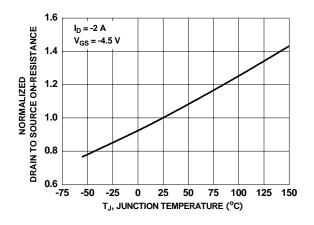


Figure 3. Normalized On Resistance vs Junction Temperature

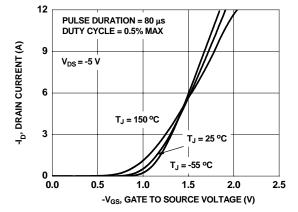


Figure 5. Transfer Characteristics

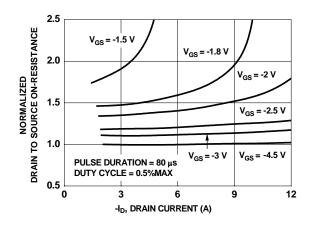


Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

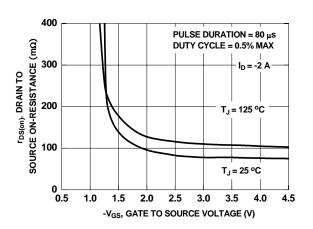


Figure 4. On-Resistance vs Gate to Source Voltage

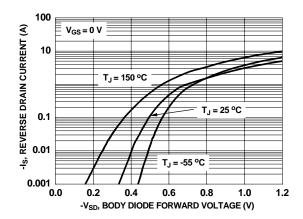


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

Typical Characteristics T_J = 25°C unless otherwise noted

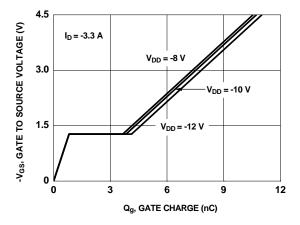


Figure 7. Gate Charge Characteristics

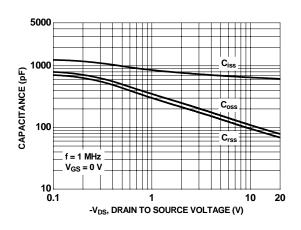


Figure 8. Capacitance vs Drain to Source Voltage

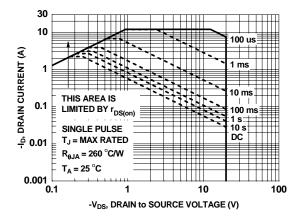


Figure 9. Forward Bias Safe Operating Area

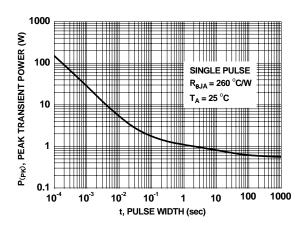


Figure 10. Single Pulse Maximum Power Dissipation

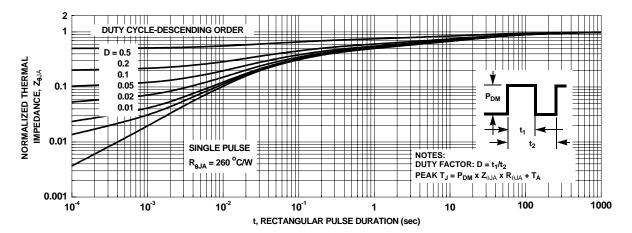
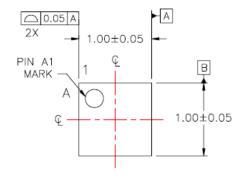
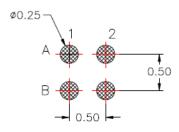


Figure 11. Junction-to-Ambient Transient Thermal Response Curve

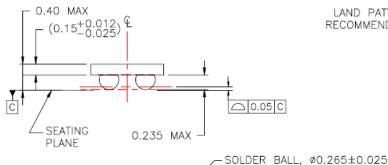
Dimensional Outline and Pad Layout



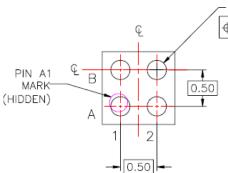


0.05 B 2X

Ø0.10@CAB Ø0.05@C



LAND PATTERN RECOMMENDATION



NOTES: UNLESS OTHERWISE SPECIFIED

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- B) DIMENSIONS ARE IN MILLIMETERS.
 C) DRAWING CONFORMS TO ASME
 Y14.5M-1994
- D) TERMINAL CONFIGURATION TABLE:

GATE	SOURCE	DRAIN
A1	A2, B2	B1

E) DRAWING FILENAME: MKT-UC004ADREV2





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