HEF4082B

Dual 4-input AND gate

Rev. 6 — 28 May 2015

Product data sheet

1. General description

The HEF4082B is a dual 4-input AND gate. The outputs are fully buffered for highest noise immunity and pattern insensitivity to output impedance variations.

It operates over a recommended V_{DD} power supply range of 3 V to 15 V referenced to V_{SS} (usually ground). Unused inputs must be connected to V_{DD} , V_{SS} , or another input.

2. Features and benefits

- Fully static operation
- 5 V, 10 V, and 15 V parametric ratings
- Standardized symmetrical output characteristics
- Inputs and outputs are protected against electrostatic effects
- Specified from -40 °C to +85 °C and -40 °C to +125 °C
- Complies with JEDEC standard JESD 13-B

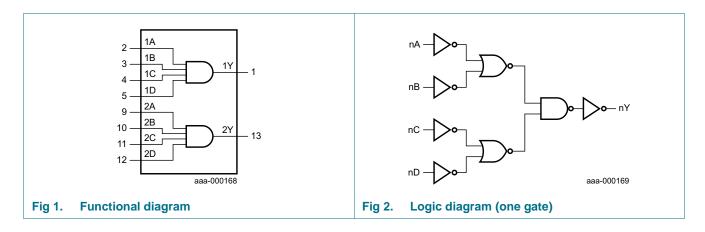
3. Ordering information

Table 1. Ordering information

All types operate from -40 °C to +125 °C.

Type number	Package				
	Name	ame Description V			
HEF4082BT	SO14	plastic small outline package; 14 leads; body width 3.9 mm	SOT108-1		

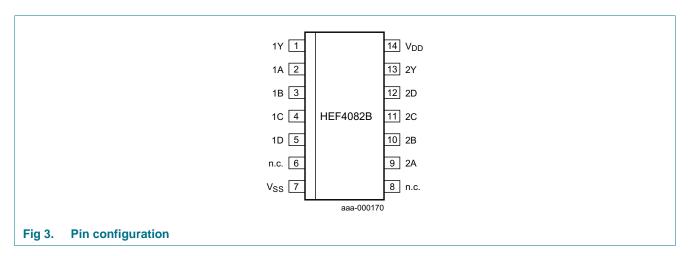
4. Functional diagram





5. Pinning information

5.1 Pinning



5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
1A, 1B, 1C, 1D	2, 3, 4, 5	input
2A, 2B, 2C, 2D	9, 10, 11, 12	input
1Y, 2Y	1, 13	output
n.c.	6, 8	not connected
V _{SS}	7	ground (0 V)
V_{DD}	14	supply voltage

6. Functional description

Table 3. Function table[1]

Input	Output			
nA	nB	nC	nD	nY
L	X	X	X	L
X	L	X	X	L
X	X	L	Х	L
X	X	Х	L	L
Н	Н	Н	Н	Н

[1] H = HIGH voltage level; L = LOW voltage level; X = don't care.

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to $V_{SS} = 0 \text{ V}$ (ground).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DD}	supply voltage		-0.5	+18	V
I _{IK}	input clamping current	$V_{I} < -0.5 \text{ V or } V_{I} > V_{DD} + 0.5 \text{ V}$	-	±10	mA
VI	input voltage		-0.5	$V_{DD} + 0.5$	V
I _{OK}	output clamping current	$V_{O} < -0.5 \text{ V or } V_{O} > V_{DD} + 0.5 \text{ V}$	-	±10	mA
I _{I/O}	input/output current		-	±10	mA
I _{DD}	supply current		-	50	mA
T _{stg}	storage temperature		-65	+150	°C
T _{amb}	ambient temperature		-40	+125	°C
P _{tot}	total power dissipation	$T_{amb} = -40 ^{\circ}\text{C} \text{ to + 125 } ^{\circ}\text{C}$			
		SO14 [1]	-	500	mW
Р	power dissipation	per output	-	100	mW

^[1] For SO14 packages: above T_{amb} = 70 °C, P_{tot} derates linearly with 8 mW/K.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DD}	supply voltage		3	15	V
V _I	input voltage		0	V_{DD}	V
T _{amb}	ambient temperature	in free air	-40	+125	°C
Δt/ΔV	input transition rise and fall rate	V _{DD} = 5 V	-	3.75	ns/V
		V _{DD} = 10 V	-	0.5	ns/V
		V _{DD} = 15 V	-	0.08	ns/V

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9. Static characteristics

Table 6. Static characteristics

 $V_{SS} = 0$ V; $V_I = V_{SS}$ or V_{DD} ; unless otherwise specified.

Symbol	Parameter	Conditions	V_{DD}	T _{amb} =	–40 °C	T _{amb} =	+25 °C	T _{amb} =	+85 °C	T _{amb} =	+125 °C	Unit
				Min	Max	Min	Max	Min	Max	Min	Max	
V _{IH}	HIGH-level	$ I_{O} < 1 \mu A$	5 V	3.5	-	3.5	-	3.5	-	3.5	-	V
	input voltage		10 V	7.0	-	7.0	-	7.0	-	7.0	-	V
			15 V	11.0	-	11.0	-	11.0	-	11.0	-	V
V_{IL}	LOW-level	$ I_{O} < 1 \mu A$	5 V	-	1.5	-	1.5	-	1.5	-	1.5	V
	input voltage		10 V	-	3.0	-	3.0	-	3.0	-	3.0	V
			15 V	-	4.0	-	4.0	-	4.0	-	4.0	V
V _{OH}	HIGH-level	$ I_{O} < 1 \mu A$	5 V	4.95	-	4.95	-	4.95	-	4.95	-	V
	output voltage		10 V	9.95	-	9.95	-	9.95	-	9.95	-	V
			15 V	14.95	-	14.95	-	14.95	-	14.95	-	V
V _{OL}		OW-level $ I_O < 1 \mu A$ utput voltage	5 V	-	0.05	-	0.05	-	0.05	-	0.05	V
	output voltage		10 V	-	0.05	-	0.05	-	0.05	-	0.05	V
			15 V	-	0.05	-	0.05	-	0.05	-	0.05	V
I _{OH}	HIGH-level	V _O = 2.5 V	5 V	-	-1.7	-	-1.4	-	-1.1	-	-1.1	mA
	output current	$V_0 = 4.6 \text{ V}$	5 V	-	-0.64	-	-0.5	-	-0.36	-	-0.36	mA
		$V_0 = 9.5 \text{ V}$	10 V	-	-1.6	-	-1.3	-	-0.9	-	-0.9	mA
		V _O = 13.5 V	15 V	-	-4.2	-	-3.4	-	-2.4	-	-2.4	mA
I _{OL}	LOW-level	evel $V_O = 0.4 \text{ V}$	5 V	0.64	-	0.5	-	0.36	-	0.36	-	mA
	output current	$V_0 = 0.5 \ V$	10 V	1.6	-	1.3	-	0.9	-	0.9	-	mA
		V _O = 1.5 V	15 V	4.2	-	3.4	-	2.4	-	2.4	-	mA
I _I	input leakage current		15 V	-	±0.1	-	±0.1	-	±1.0	-	±1.0	μА
I _{DD}	supply current	all valid input	5 V	-	0.25	-	0.25	-	7.5	-	7.5	μΑ
		combinations;	10 V	-	0.5	-	0.5	-	15.0	-	15.0	μΑ
		I _O = 0 A	15 V	-	1.0	-	1.0	-	30.0	-	30.0	μΑ
C _I	input capacitance			-	-	-	7.5	-	-	-	-	pF

10. Dynamic characteristics

Table 7. Dynamic characteristics

 T_{amb} = 25 °C; C_L = 50 pF; t_r = $t_f \le$ 20 ns; waveforms see <u>Figure 4</u>; test circuit see <u>Figure 5</u>; unless otherwise specified. [1]

Symbol	Parameter	Conditions	V_{DD}	Extrapolation formula	Min	Тур	Max	Unit
t _{pd}	propagation delay	nA, nB, nC,	5 V [2]	38 + 0.55 × C _L	-	65	125	ns
		nD to nY	10 V	19 + 0.23 × C _L	-	30	60	ns
			15 V	17 + 0.16 × C _L	-	25	45	ns
t _{THL}	HIGH to LOW output	nY	5 V	10 + 1.0 × C _L	-	60	120	ns
	transition time		10 V	9 + 0.42 × C _L	-	30	60	ns
		1	15 V	6 + 0.28 × C _L	-	20	40	ns
t _{TLH}	LOW to HIGH output	•	5 V	10 + 1.0 × C _L	-	60	120	ns
	transition time		10 V	9 + 0.42 × C _L	-	30	60	ns
			15 V	6 + 0.28 × C _L	-	20	40	ns

^[1] The typical value of the propagation delay and output transition time can be calculated with the extrapolation formula (C_L in pF).

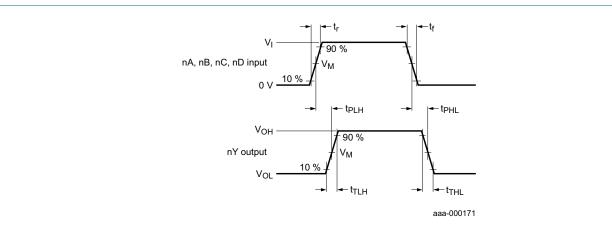
Table 8. Dynamic power dissipation

 $V_{SS} = 0 \text{ V; } t_r = t_f \le 20 \text{ ns; } T_{amb} = 25 \text{ °C.}$

Symbol	Parameter	V_{DD}	Typical formula	where:
P_D	dynamic power dissipation	5 V	$P_D = 1500 \times f_i + \Sigma(f_o \times C_L) \times V_{DD}^2 (\mu W)$	f_i = input frequency in MHz;
		10 V	$P_D = 6700 \times f_i + \Sigma (f_o \times C_L) \times V_{DD}^2 (\mu W)$	fo = output frequency in MHz;
		15 V	$P_D = 16800 \times f_i + \Sigma (f_o \times C_L) \times V_{DD}^2 (\mu W)$	C_L = output load capacitance in pF;
				$\Sigma(f_0 \times C_L)$ = sum of the outputs;
				V_{DD} = supply voltage in V.

^[2] t_{pd} is the same as t_{PHL} and t_{PLH} .

11. Waveforms



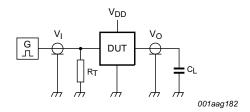
Measurement points are given in Table 9.

Logic levels: V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig 4. Input to output propagation delay and output transition times

Table 9. Measurement points

Supply voltage	Input	Output
V_{DD}	V _M	V _M
5 V to 15 V	0.5V _{DD}	0.5V _{DD}



Test data is given in Table 10.

Definitions for test circuit:

DUT = Device Under Test.

 C_L = load capacitance including jig and probe capacitance.

 R_T = termination resistance should be equal to the output impedance Z_0 of the pulse generator.

Fig 5. Test circuit for measuring switching times

Table 10. Test data

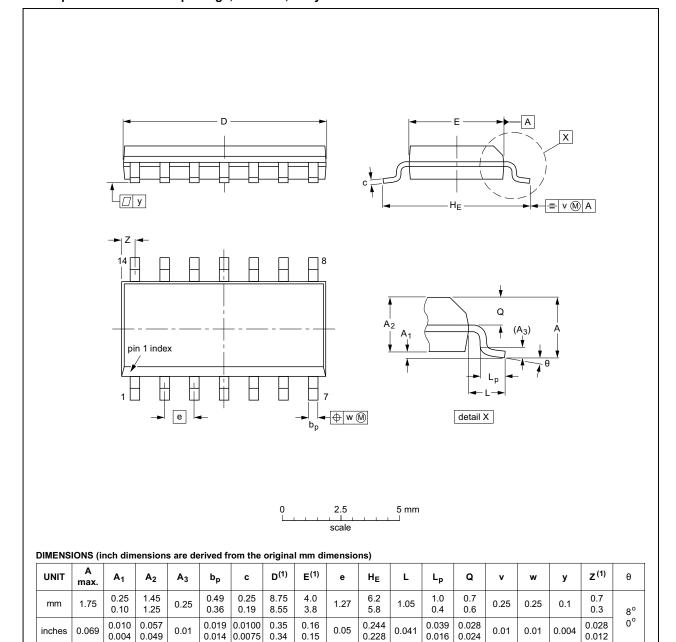
Supply voltage	Input	Load	
V_{DD}	VI	t _r , t _f	CL
5 V to 15 V	V _{SS} or V _{DD}	≤ 20 ns	50 pF

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12. Package outline

SO14: plastic small outline package; 14 leads; body width 3.9 mm

SOT108-1



Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

			EUROPEAN	ISSUE DATE	
IEC	JEDEC	JEITA	PROJECTION		
076E06	MS-012			99-12-27 03-02-19	
_				IEC JEDEC JEHA	

Fig 6. Package outline SOT108-1 (SO14)

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13. Abbreviations

Table 11. Abbreviations

Acronym	Description
DUT	Device Under Test

14. Revision history

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes		
HEF4082B v.6	20150528	Product data sheet	-	HEF4082B v.5		
Modifications:	Type number HEF4082BP (SOT27-1) removed.					
HEF4082B v.5	20111116	Product data sheet	-	HEF4082B v.4		
Modifications:	Legal pages updated.					
	 Changes in "General description" and "Features and benefits". 					
HEF4082B v.4	20110823	Product data sheet	-	HEF4082B_CNV v.3		
HEF4082B_CNV v.3	19950101	Product specification	-	HEF4082B_CNV v.2		
HEF4082B_CNV v.2	19950101	Product specification	-	-		

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15.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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Product [short] data sheet	Production	This document contains the product specification.

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