

# MC74HC164B

## 8-Bit Serial-Input/Parallel-Output Shift Register

### High-Performance Silicon-Gate CMOS

The MC74HC164B is identical in pinout to the LS164. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

The MC74HC164B is an 8-bit, serial-input to parallel-output shift register. Two serial data inputs, A1 and A2, are provided so that one input may be used as a data enable. Data is entered on each rising edge of the clock. The active-low asynchronous Reset overrides the Clock and Serial Data inputs. Schmitt-trigger action at the Clock input enhances the device's tolerance to slower rise and fall times and immunity to noise of the input clock signal.

#### Features

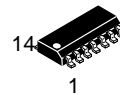
- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2.0 V to 6.0 V
- Low Input Current: 1  $\mu$ A
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the JEDEC Standard No. 7 A Requirements
- Chip Complexity: 244 FETs or 61 Equivalent Gates
- NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant



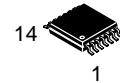
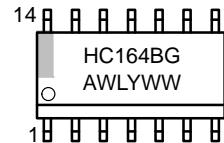
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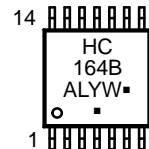
#### MARKING DIAGRAMS



SOIC-14  
D SUFFIX  
CASE 751A



TSSOP-14  
DT SUFFIX  
CASE 948G



A = Assembly Location  
L, WL = Wafer Lot  
Y = Year  
W, WW = Work Week  
G or ■ = Pb-Free Package

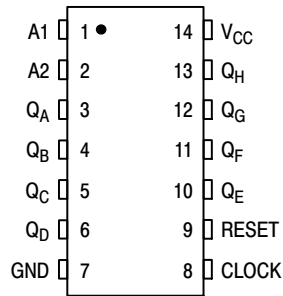
(Note: Microdot may be in either location)

#### ORDERING INFORMATION

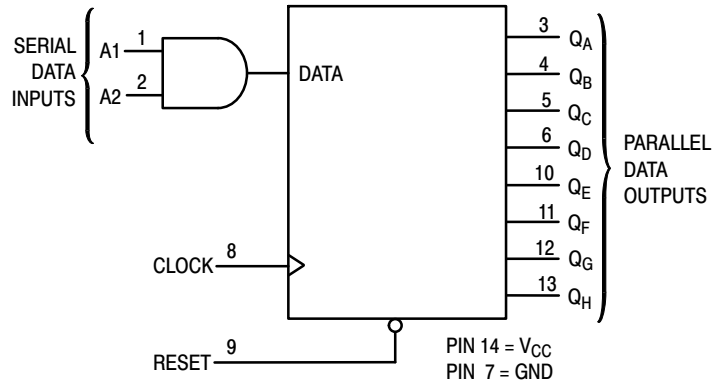
See detailed ordering and shipping information in the package dimensions section on page 2 of this data sheet.

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## PIN ASSIGNMENT



## LOGIC DIAGRAM



## FUNCTION TABLE

Inputs				Outputs			
Reset	Clock	A1	A2	QA	QB	...	QH
L	X	X	X	L	L	...	L
H		X	X	No Change			
H		H	D	D	QA <sub>n</sub>	...	QG <sub>n</sub>
H		D	H	D	QA <sub>n</sub>	...	QG <sub>n</sub>

D = data input

QA<sub>n</sub> – QG<sub>n</sub> = data shifted from the preceding stage on a rising edge at the clock input.

## ORDERING INFORMATION

Device	Package	Shipping†
MC74HC164BDG	SOIC-14 (Pb-Free)	55 Units / Rail
MC74HC164BDR2G		2500 / Tape & Reel
NLV74HC164BDR2G*		2500 / Tape & Reel
MC74HC164BDTR2G	TSSOP-14 (Pb-Free)	2500 / Tape & Reel
NLV74HC164BDTR2G*		2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

\*NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable

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## MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
$V_{CC}$	DC Supply Voltage (Referenced to GND)	- 0.5 to + 7.0	V
$V_{in}$	DC Input Voltage (Referenced to GND)	- 0.5 to $V_{CC} + 0.5$	V
$V_{out}$	DC Output Voltage (Referenced to GND)	- 0.5 to $V_{CC} + 0.5$	V
$I_{in}$	DC Input Current, per Pin	$\pm 20$	mA
$I_{out}$	DC Output Current, per Pin	$\pm 25$	mA
$I_{CC}$	DC Supply Current, $V_{CC}$ and GND Pins	$\pm 50$	mA
$P_D$	Power Dissipation in Still Air, SOIC Package† TSSOP Package†	500 450	mW
$T_{stg}$	Storage Temperature	- 65 to + 150	°C
$T_L$	Lead Temperature, 1 mm from Case for 10 Seconds (SOIC or TSSOP Package)	260	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range  $GND \leq (V_{in} \text{ or } V_{out}) \leq V_{CC}$ . Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or  $V_{CC}$ ). Unused outputs must be left open.

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

†Derating — SOIC Package: - 7 mW/°C from 65° to 125°C  
TSSOP Package: - 6.1 mW/°C from 65° to 125°C

## RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit	
$V_{CC}$	DC Supply Voltage (Referenced to GND)	2.0	6.0	V	
$V_{in}, V_{out}$	DC Input Voltage, Output Voltage (Referenced to GND)	0	$V_{CC}$	V	
$T_A$	Operating Temperature, All Package Types	- 55	+ 125	°C	
$t_r, t_f$	Input Rise and Fall Time (Figure 1)	$V_{CC} = 2.0 \text{ V}$ $V_{CC} = 4.5 \text{ V}$ $V_{CC} = 6.0 \text{ V}$	0 0 0	No Limit No Limit No Limit	ns

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

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## DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V <sub>CC</sub> V	Guaranteed Limit			Unit
				-55°C to 25°C	≤ 85°C	≤ 125°C	
V <sub>T+</sub> max	Maximum Positive-Going Input Threshold Voltage (Figure 3)	V <sub>out</sub> = 0.1V  I <sub>out</sub>   ≤ 20μA	2.0	1.50	1.50	1.50	V
			3.0	2.15	2.15	2.15	
			4.5	3.15	3.15	3.15	
			6.0	4.20	4.20	4.20	
V <sub>T+</sub> min	Minimum Positive-Going Input Threshold Voltage (Figure 3)	V <sub>out</sub> = 0.1V  I <sub>out</sub>   ≤ 20μA	2.0	1.0	0.95	0.95	V
			3.0	1.5	1.45	1.45	
			4.5	2.3	2.25	2.25	
			6.0	3.0	2.95	2.95	
V <sub>T-</sub> max	Maximum Negative-Going Input Threshold Voltage (Figure 3)	V <sub>out</sub> = V <sub>CC</sub> - 0.1V  I <sub>out</sub>   ≤ 20μA	2.0	0.9	0.95	0.95	V
			3.0	1.4	1.45	1.45	
			4.5	2.0	2.05	2.05	
			6.0	2.6	2.65	2.65	
V <sub>T-</sub> min	Minimum Negative-Going Input Threshold Voltage (Figure 3)	V <sub>out</sub> = V <sub>CC</sub> - 0.1V  I <sub>out</sub>   ≤ 20μA	2.0	0.3	0.3	0.3	V
			3.0	0.5	0.5	0.5	
			4.5	0.9	0.9	0.9	
			6.0	1.2	1.2	1.2	
V <sub>H</sub> max (Note 1)	Maximum Hysteresis Voltage (Figure 3)	V <sub>out</sub> = 0.1V or V <sub>CC</sub> - 0.1V  I <sub>out</sub>   ≤ 20μA	2.0	1.20	1.20	1.20	V
			3.0	1.65	1.65	1.65	
			4.5	2.25	2.25	2.25	
			6.0	3.00	3.00	3.00	
V <sub>H</sub> min (Note 1)	Minimum Hysteresis Voltage (Figure 3)	V <sub>out</sub> = 0.1V or V <sub>CC</sub> - 0.1V  I <sub>out</sub>   ≤ 20μA	2.0	0.20	0.20	0.20	V
			3.0	0.25	0.25	0.25	
			4.5	0.40	0.40	0.40	
			6.0	0.50	0.50	0.50	
V <sub>OH</sub>	Minimum High-Level Output Voltage	V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 20 μA	2.0	1.9	1.9	1.9	V
			4.5	4.4	4.4	4.4	
			6.0	5.9	5.9	5.9	
			V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 2.4 mA	3.0	2.48	2.34	
I <sub>out</sub>   ≤ 4.0 mA	4.5	3.98	3.84	3.70			
I <sub>out</sub>   ≤ 5.2 mA	6.0	5.48	5.34	5.20			
V <sub>OL</sub>	Maximum Low-Level Output Voltage	V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 20 μA	2.0	0.1	0.1	0.1	V
			4.5	0.1	0.1	0.1	
			6.0	0.1	0.1	0.1	
			V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 2.4 mA	3.0	0.26	0.33	
I <sub>out</sub>   ≤ 4.0 mA	4.5	0.26	0.33	0.40			
I <sub>out</sub>   ≤ 5.2 mA	6.0	0.26	0.33	0.40			
I <sub>in</sub>	Maximum Input Leakage Current	V <sub>in</sub> = V <sub>CC</sub> or GND	6.0	± 0.1	± 1.0	± 1.0	μA
I <sub>CC</sub>	Maximum Quiescent Supply Current (per Package)	V <sub>in</sub> = V <sub>CC</sub> or GND I <sub>out</sub> = 0 μA	6.0	4	40	160	μA

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

1. V<sub>H</sub>min > (V<sub>T+</sub> min) - (V<sub>T-</sub> max); V<sub>H</sub>max = (V<sub>T+</sub> max) - (V<sub>T-</sub> min).

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## AC ELECTRICAL CHARACTERISTICS (C<sub>L</sub> = 50 pF, Input t<sub>r</sub> = t<sub>f</sub> = 6 ns)

Symbol	Parameter	V <sub>CC</sub> V	Guaranteed Limit			Unit
			-55°C to 25°C	≤ 85°C	≤ 125°C	
f <sub>max</sub>	Maximum Clock Frequency (50% Duty Cycle) (Figures 1 and 4)	2.0	10	10	10	MHz
		3.0	20	20	20	
		4.5	40	35	30	
		6.0	50	45	40	
t <sub>PLH</sub> , t <sub>PHL</sub>	Maximum Propagation Delay, Clock to Q (Figures 1 and 4)	2.0	160	200	250	ns
		3.0	100	150	200	
		4.5	32	40	48	
		6.0	27	34	42	
t <sub>PHL</sub>	Maximum Propagation Delay, Reset to Q (Figures 2 and 4)	2.0	175	220	260	ns
		3.0	100	150	200	
		4.5	35	44	53	
		6.0	30	37	45	
t <sub>TLH</sub> , t <sub>THL</sub>	Maximum Output Transition Time, Any Output (Figures 1 and 4)	2.0	75	95	110	ns
		3.0	27	32	36	
		4.5	15	19	22	
		6.0	13	16	19	
C <sub>in</sub>	Maximum Input Capacitance	—	10	10	10	pF
C <sub>PD</sub>	Power Dissipation Capacitance (Per Package)*	Typical @ 25°C, V <sub>CC</sub> = 5.0 V			pF	
		180				

## TIMING REQUIREMENTS (Input t<sub>r</sub> = t<sub>f</sub> = 6 ns)

Symbol	Parameter	V <sub>CC</sub> V	Guaranteed Limit			Unit
			-55°C to 25°C	≤ 85°C	≤ 125°C	
t <sub>su</sub>	Minimum Setup Time, A1 or A2 to Clock (Figure 3)	2.0	25	35	40	ns
		3.0	15	20	25	
		4.5	7	8	9	
		6.0	5	6	6	
t <sub>h</sub>	Minimum Hold Time, Clock to A1 or A2 (Figure 3)	2.0	3	3	3	ns
		3.0	3	3	3	
		4.5	3	3	3	
		6.0	3	3	3	
t <sub>rec</sub>	Minimum Recovery Time, Reset Inactive to Clock (Figure 2)	2.0	3	3	3	ns
		3.0	3	3	3	
		4.5	3	3	3	
		6.0	3	3	3	
t <sub>w</sub>	Minimum Pulse Width, Clock (Figure 1)	2.0	50	60	75	ns
		3.0	26	35	45	
		4.5	12	15	20	
		6.0	10	12	15	
t <sub>w</sub>	Minimum Pulse Width, Reset (Figure 2)	2.0	50	60	75	ns
		3.0	26	35	45	
		4.5	12	15	20	
		6.0	10	12	15	

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## PIN DESCRIPTIONS

### INPUTS

#### A1, A2 (Pins 1, 2)

Serial Data Inputs. Data at these inputs determine the data to be entered into the first stage of the shift register. For a high level to be entered into the shift register, both A1 and A2 inputs must be high, thereby allowing one input to be used as a data–enable input. When only one serial input is used, the other must be connected to  $V_{CC}$ .

#### Clock (Pin 8)

Shift Register Clock. A positive–going transition on this pin shifts the data at each stage to the next stage. The shift

register is completely static, allowing clock rates down to DC in a continuous or intermittent mode.

### OUTPUTS

#### $Q_A - Q_H$ (Pins 3, 4, 5, 6, 10, 11, 12, 13)

Parallel Shift Register Outputs. The shifted data is presented at these outputs in true, or noninverted, form.

### CONTROL INPUT

#### Reset (Pin 9)

Active–Low, Asynchronous Reset Input. A low voltage applied to this input resets all internal flip–flops and sets Outputs  $Q_A - Q_H$  to the low level state.

## SWITCHING WAVEFORMS

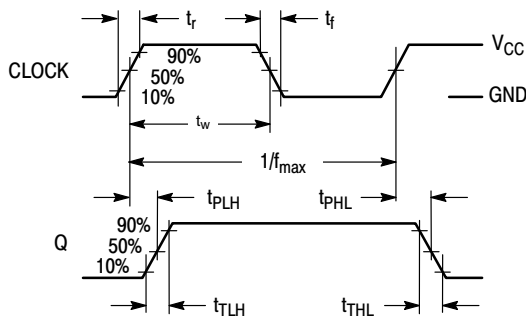


Figure 1.

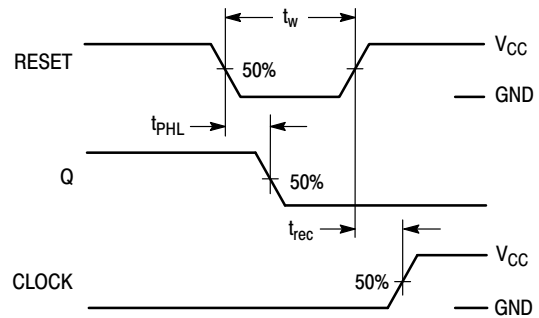


Figure 2.

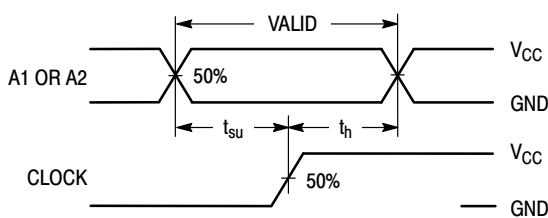
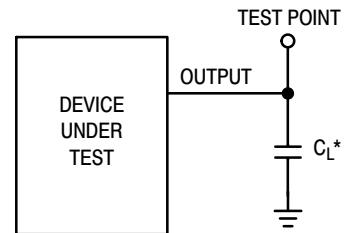


Figure 3.

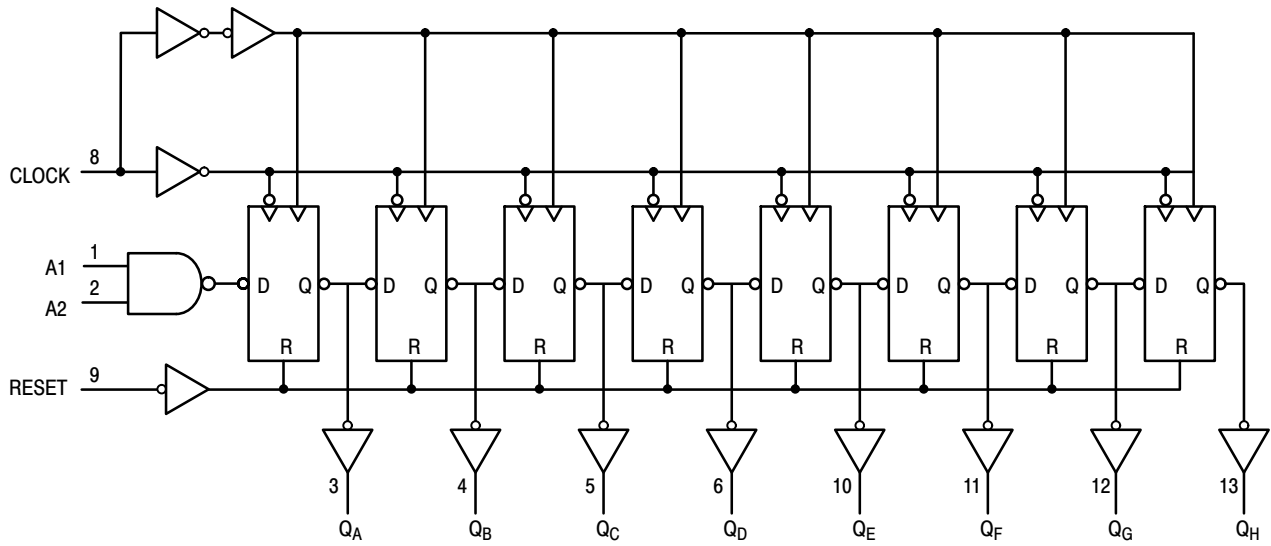


\*Includes all probe and jig capacitance

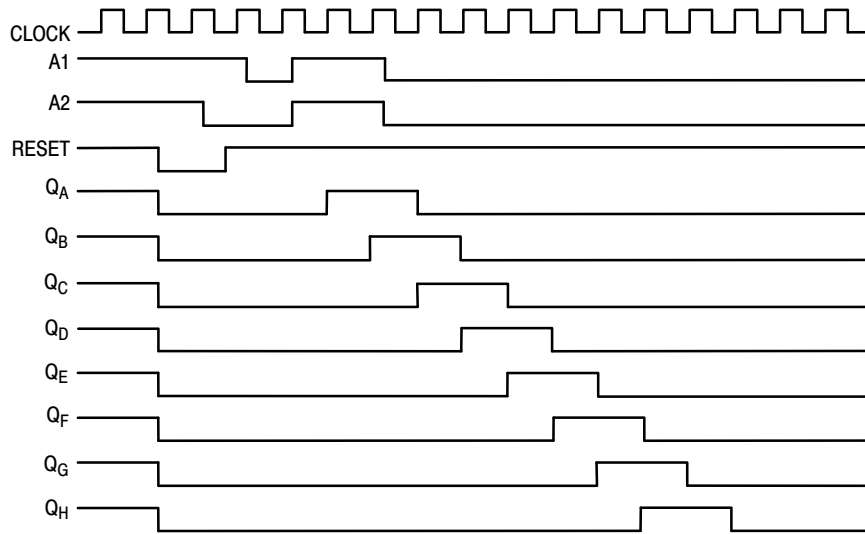
Figure 4. Test Circuit

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## EXPANDED LOGIC DIAGRAM



## TIMING DIAGRAM



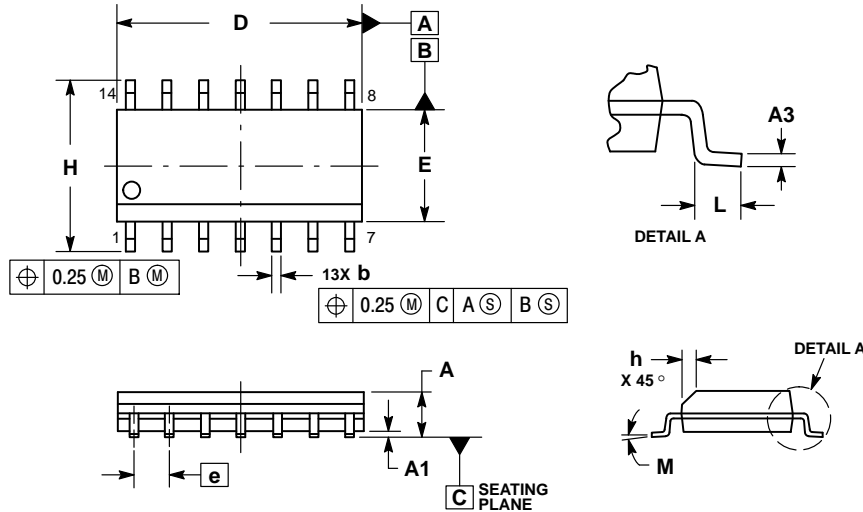




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## PACKAGE DIMENSIONS

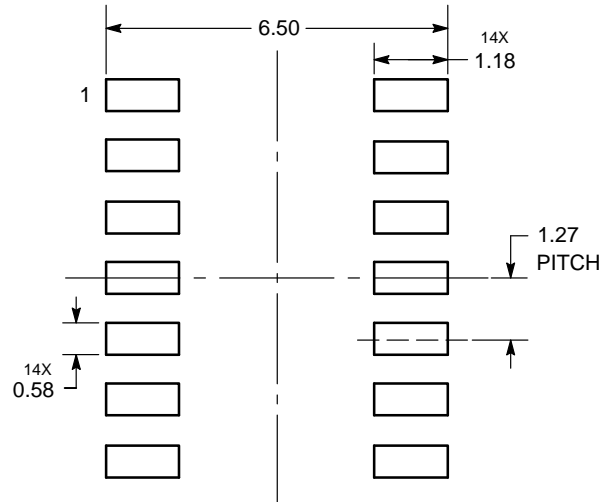
SOIC-14 NB  
CASE 751A-03  
ISSUE K



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF AT MAXIMUM MATERIAL CONDITION.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSIONS.
5. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.

### SOLDERING FOOTPRINT\*



DIMENSIONS: MILLIMETERS

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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Сотрудничество с глобальными дистрибьюторами электронных компонентов, предоставляет возможность заказывать и получать с международных складов практически любой перечень компонентов в оптимальные для Вас сроки.

На всех этапах разработки и производства наши партнеры могут получить квалифицированную поддержку опытных инженеров.

Система менеджмента качества компании отвечает требованиям в соответствии с ГОСТ Р ИСО 9001, ГОСТ РВ 0015-002 и ЭС РД 009

### Офис по работе с юридическими лицами:

105318, г.Москва, ул.Щербаковская д.3, офис 1107, 1118, ДЦ «Щербаковский»

Телефон: +7 495 668-12-70 (многоканальный)

Факс: +7 495 668-12-70 (доб.304)

E-mail: [info@moschip.ru](mailto:info@moschip.ru)

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