

DATA SHEET

For a complete data sheet, please also download:

- The IC06 74HC/HCT/HCU/HCMOS Logic Family Specifications
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Information
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Outlines

74HC/HCT4511 BCD to 7-segment latch/decoder/driver

Product specification
File under Integrated Circuits, IC06

December 1990

BCD to 7-segment latch/decoder/driver

74HC/HCT4511

FEATURES

- Latch storage of BCD inputs
- Blanking input
- Lamp test input
- Driving common cathode LED displays
- Guaranteed 10 mA drive capability per output
- Output capability: non-standard
- I_{CC} category: MSI

GENERAL DESCRIPTION

The 74HC/HCT4511 are high-speed Si-gate CMOS devices and are pin compatible with "4511" of the "4000B" series. They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT4511 are BCD to 7-segment latch/decoder/drivers with four address inputs (D₁ to D₄), an active LOW latch enable input ($\overline{\text{LE}}$), an active LOW

ripple blanking input ($\overline{\text{BI}}$), an active LOW lamp test input ($\overline{\text{LT}}$), and seven active HIGH segment outputs (Q_a to Q_g).

When $\overline{\text{LE}}$ is LOW, the state of the segment outputs (Q_a to Q_g) is determined by the data on D₁ to D₄.

When $\overline{\text{LE}}$ goes HIGH, the last data present on D₁ to D₄ are stored in the latches and the segment outputs remain stable.

When $\overline{\text{LT}}$ is LOW, all the segment outputs are HIGH independent of all other input conditions. With $\overline{\text{LT}}$ HIGH, a LOW on $\overline{\text{BI}}$ forces all segment outputs LOW. The inputs $\overline{\text{LT}}$ and $\overline{\text{BI}}$ do not affect the latch circuit.

APPLICATIONS

- Driving LED displays
- Driving incandescent displays
- Driving fluorescent displays
- Driving LCD displays
- Driving gas discharge displays

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25 °C; t_r = t_f = 6 ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t _{PHL} / t _{PLH}	propagation delay	C _L = 15 pF; V _{CC} = 5 V			
	D _n to Q _n		24	24	ns
	$\overline{\text{LE}}$ to Q _n		23	24	ns
	$\overline{\text{BI}}$ to Q _n		19	20	ns
	$\overline{\text{LT}}$ to Q _n		12	13	ns
C _I	input capacitance		3.5	3.5	pF
C _{PD}	power dissipation capacitance per latch	notes 1 and 2	64	64	pF

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f_i = input frequency in MHz

f_o = output frequency in MHz

$\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs

C_L = output load capacitance in pF

V_{CC} = supply voltage in V

2. For HC the condition is V_I = GND to V_{CC}

For HCT the condition is V_I = GND to V_{CC} – 1.5 V

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ORDERING INFORMATION

See *“74HC/HCT/HCU/HCMOS Logic Package Information”*.

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
3	$\overline{\text{LT}}$	lamp test input (active LOW)
4	$\overline{\text{BI}}$	ripple blanking input (active LOW)
5	$\overline{\text{LE}}$	latch enable input (active LOW)
7, 1, 2, 6	D ₁ to D ₄	BCD address inputs
8	GND	ground (0 V)
13, 12, 11, 10, 9, 15, 14	Q _a to Q _g	segments outputs
16	V _{CC}	positive supply voltage

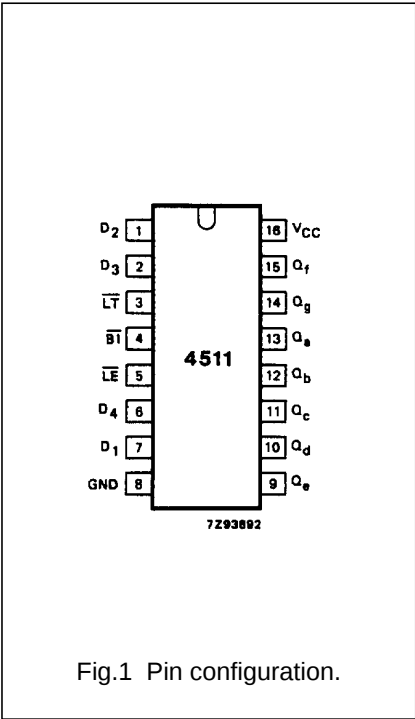


Fig.1 Pin configuration.

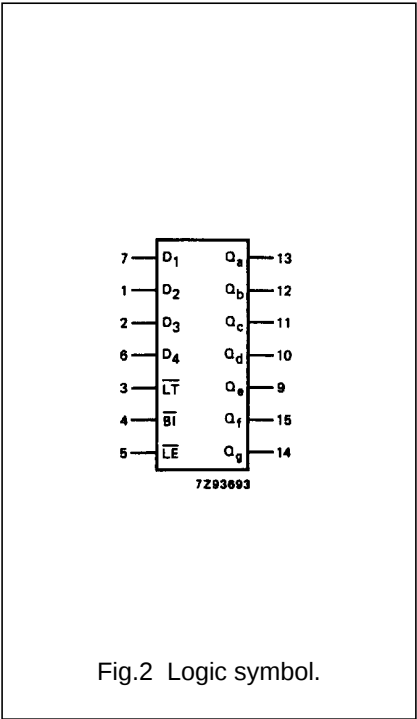


Fig.2 Logic symbol.

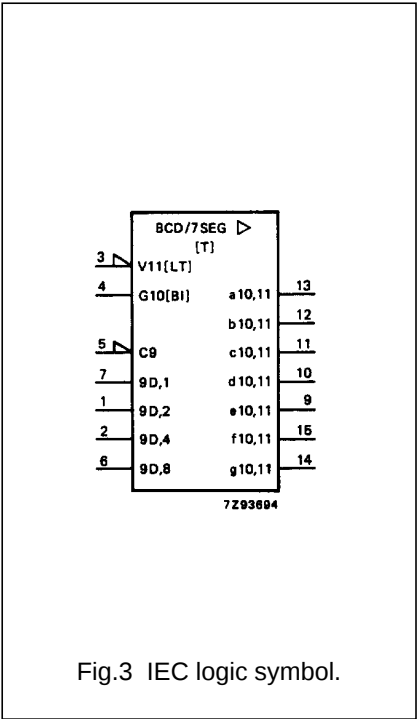
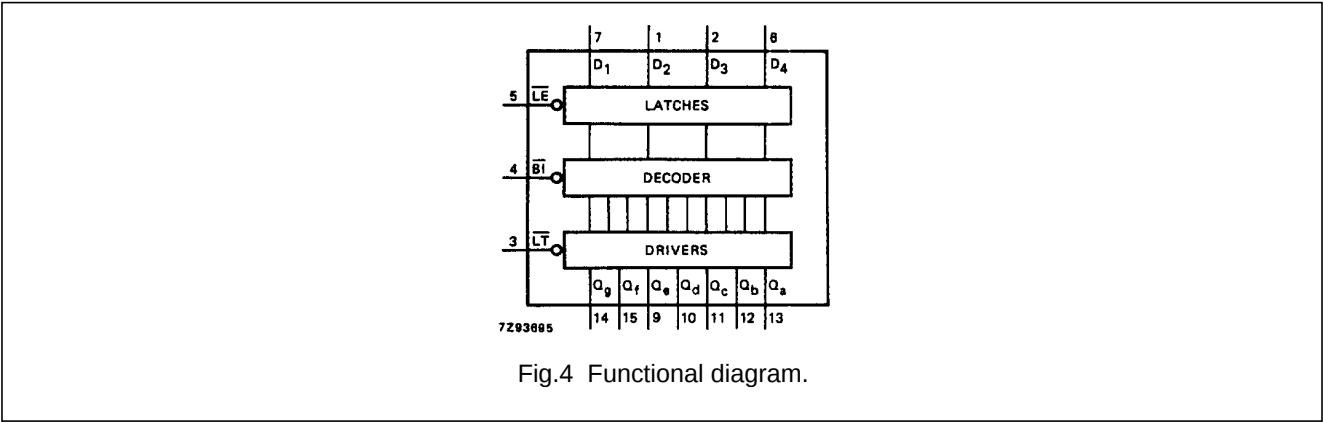


Fig.3 IEC logic symbol.

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FUNCTION TABLE

INPUTS							OUTPUTS							DISPLAY
LE	BI	LT	D4	D3	D2	D1	Qa	Qb	Qc	Qd	Qe	Qf	Qg	
X	X	L	X	X	X	X	H	H	H	H	H	H	H	8
X	L	H	X	X	X	X	L	L	L	L	L	L	L	blank
L	H	H	L	L	L	L	H	H	H	H	H	H	L	0
L	H	H	L	L	L	H	L	H	H	L	L	L	L	1
L	H	H	L	L	H	L	H	H	L	H	H	L	H	2
L	H	H	L	L	H	H	H	H	H	H	L	L	H	3
L	H	H	L	H	L	L	L	H	H	L	L	H	H	4
L	H	H	L	H	L	H	H	L	H	H	L	H	H	5
L	H	H	L	H	H	L	L	L	H	H	H	H	H	6
L	H	H	L	H	H	H	H	H	H	L	L	L	L	7
L	H	H	H	L	L	L	H	H	H	H	H	H	H	8
L	H	H	H	L	L	H	H	H	H	L	L	H	H	9
L	H	H	H	L	H	L	L	L	L	L	L	L	L	blank
L	H	H	H	L	H	H	L	L	L	L	L	L	L	blank
L	H	H	H	H	L	L	L	L	L	L	L	L	L	blank
L	H	H	H	H	L	H	L	L	L	L	L	L	L	blank
L	H	H	H	H	H	L	L	L	L	L	L	L	L	blank
L	H	H	H	H	H	H	L	L	L	L	L	L	L	blank
H	H	H	X	X	X	X	(1)							(1)

- Note**
1. Depends upon the BCD-code applied during the LOW-to-HIGH transition of LE.
H = HIGH voltage level
L = LOW voltage level
X = don't care

BCD to 7-segment latch/decoder/driver

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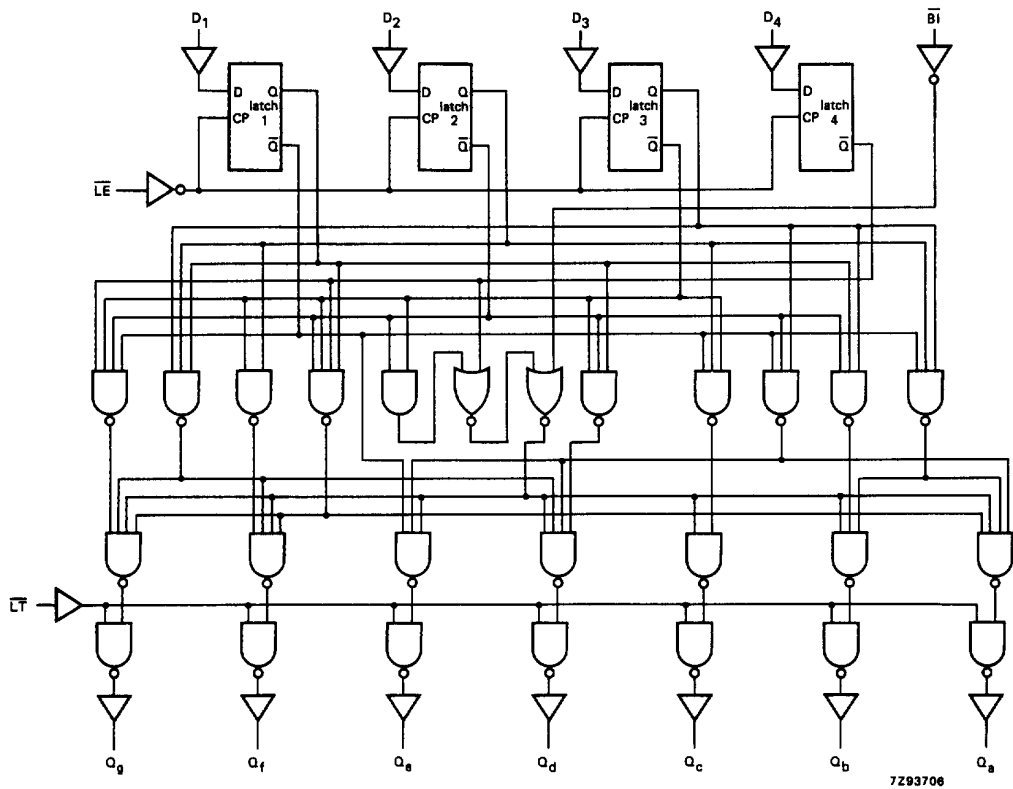


Fig.5 Logic diagram.

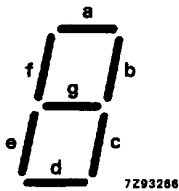


Fig.6 Segment designation.



Fig.7 Display.

BCD to 7-segment latch/decoder/driver

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DC CHARACTERISTICS FOR 74HC

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: standard, excepting V_{OH} which is given below

I_{CC} category: MSI

Non-standard DC characteristics for 74HC

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T _{amb} (°C)							UNIT	TEST CONDITIONS		
		74HC								V _{CC} (V)	V _I	–I _o (mA)
		+25			–40 to +85		–40 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
V _{OH}	HIGH level output voltage	3.98 3.60			3.84 3.35		3.70 3.10		V	4.5	V _{IH} or V _{IL}	7.5 10.0
V _{OH}	HIGH level output voltage	5.60 5.48 4.80			5.45 5.34 4.50		5.35 5.20 4.20		V	6.0	V _{IH} or V _{IL}	7.5 10.0 15.0

BCD to 7-segment latch/decoder/driver

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AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f = 6$ ns; $C_L = 50$ pF

SYMBOL	PARAMETER	T _{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V _{CC} (V)	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t _{PHL} / t _{PLH}	propagation delay D _n to Q _n		77 28 22	300 60 51		375 75 64		450 90 77	ns	2.0 4.5 6.0	Fig.8
t _{PHL} / t _{PLH}	propagation delay LE to Q _n		74 27 22	270 54 46		330 68 58		405 81 69	ns	2.0 4.5 6.0	Fig.9
t _{PHL} / t _{PLH}	propagation delay BI to Q _n		61 22 18	220 44 37		275 55 47		330 66 56	ns	2.0 4.5 6.0	Fig.10
t _{PHL} / t _{PLH}	propagation delay LT to Q _n		41 15 12	150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig.8
t _{THL} / t _{TLH}	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Figs 8, 9 and 10
t _w	latch enable pulse width LOW	80 16 14	11 4 3		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig.9
t _{su}	set-up time D _n to LE	60 12 10	14 5 4		75 15 13		90 18 15		ns	2.0 4.5 6.0	Fig.11
t _h	hold time D _n to LE	0 0 0	−11 −4 −3		0 0 0		0 0 0		ns	2.0 4.5 6.0	Fig.11

BCD to 7-segment latch/decoder/driver

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DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: standard, excepting V_{OH} which is given below

I_{CC} category: MSI

Non-standard DC characteristics for 74HCT

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T _{amb} (°C)							UNIT	TEST CONDITIONS		
		74HCT								V _{CC} (V)	V _I	-I _o (mA)
		+25			-40 to +85		-40 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
V _{OH}	HIGH level output voltage	3.98 3.60			3.84 3.35		3.70 3.10		V	4.5	V _{IH} or V _{IL}	7.5 10.0

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications.

To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
$\overline{LT}$, $\overline{LE}$	1.50
$\overline{BI}$, D_n	0.30

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AC CHARACTERISTICS FOR 74HCT

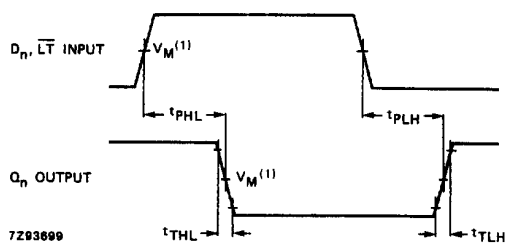
GND = 0 V; $t_r = t_f = 6$ ns; $C_L = 50$ pF

SYMBOL	PARAMETER	T _{amb} (°C)							UNIT	TEST CONDITIONS	
		74HCT								V _{CC} (V)	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t _{PHL} / t _{PLH}	propagation delay D _n to Q _n		28	60		75		90	ns	4.5	Fig.8
t _{PHL} / t _{PLH}	propagation delay $\overline{LE}$ to Q _n		27	54		68		81	ns	4.5	Fig.9
t _{PHL} / t _{PLH}	propagation delay BI to Q _n		23	44		55		66	ns	4.5	Fig.10
t _{PHL} / t _{PLH}	propagation delay $\overline{LT}$ to Q _n		16	30		38		45	ns	4.5	Fig.8
t _{THL} / t _{TLH}	output transition time		7	15		19		22	ns	4.5	Figs 8, 9 and 10
t _W	latch enable pulse width LOW	16	5		20		24		ns	4.5	Fig.9
t _{su}	set-up time D _n to $\overline{LE}$	12	5		15		18		ns	4.5	Fig.11
t _h	hold time D _n to $\overline{LE}$	0	−4		0		0		ns	4.5	Fig.11

BCD to 7-segment latch/decoder/driver

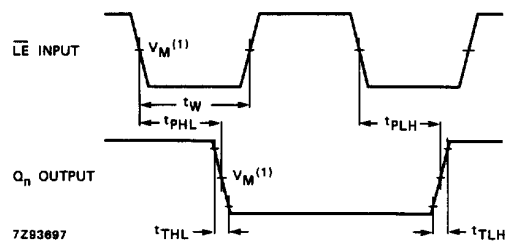
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AC WAVEFORMS



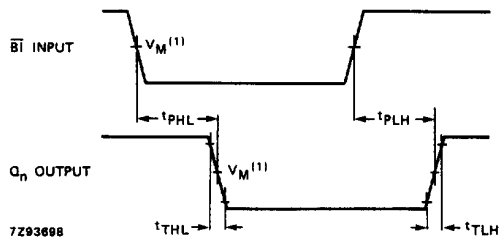
- (1) HC : $V_M = 50\%$; $V_I = \text{GND to } V_{CC}$.
HCT: $V_M = 1.3 \text{ V}$; $V_I = \text{GND to } 3 \text{ V}$.

Fig.8 Waveforms showing the input ($D_n, \overline{LT}$) to output (Q_n) propagation delays and the output transition times.



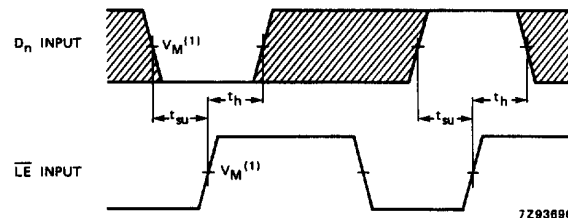
- (1) HC : $V_M = 50\%$; $V_I = \text{GND to } V_{CC}$.
HCT: $V_M = 1.3 \text{ V}$; $V_I = \text{GND to } 3 \text{ V}$.

Fig.9 Waveforms showing the input ($\overline{LE}$) to output (Q_n) propagation delays and the latch enable pulse width.



- (1) HC : $V_M = 50\%$; $V_I = \text{GND to } V_{CC}$.
HCT: $V_M = 1.3 \text{ V}$; $V_I = \text{GND to } 3 \text{ V}$.

Fig.10 Waveforms showing the input ($\overline{BI}$) to output (Q_n) propagation delays.



The shaded areas indicate when the input is permitted to change for predictable output performance.

- (1) HC : $V_M = 50\%$; $V_I = \text{GND to } V_{CC}$.
HCT: $V_M = 1.3 \text{ V}$; $V_I = \text{GND to } 3 \text{ V}$.

Fig.11 Waveforms showing the data set-up and hold times for D_n input to $\overline{LE}$ input.

BCD to 7-segment latch/decoder/driver

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APPLICATION DIAGRAMS

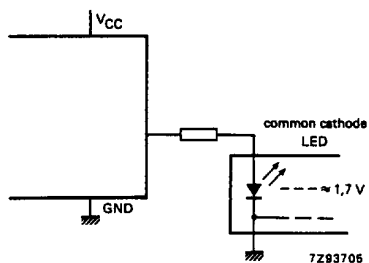


Fig.12 Connection to common cathode LED display readout.

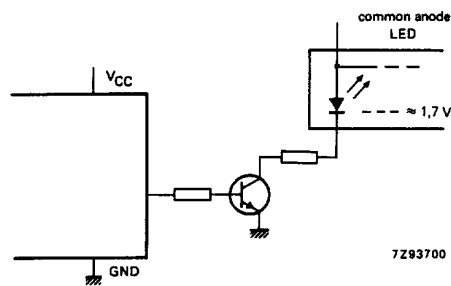
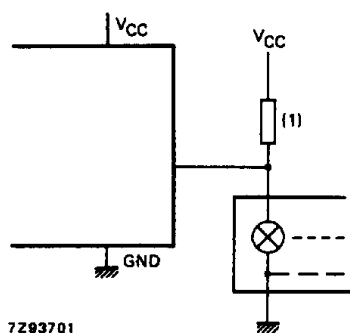


Fig.13 Connection to common anode LED display readout.



(1) A filament pre-warm resistor to reduce thermal shock and to increase effective cold resistance of the filament is recommended.

Fig.14 Connection to incandescent display readout.

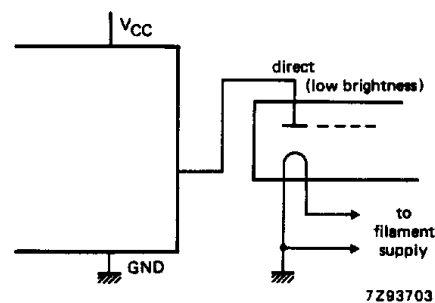


Fig.15 Connection to fluorescent display readout.

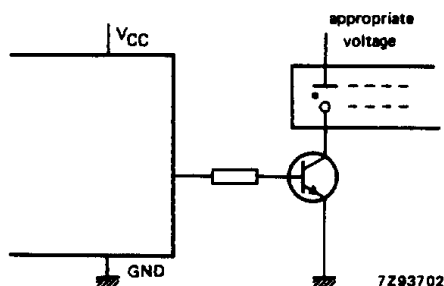


Fig.16 Connection to gas discharge display readout.

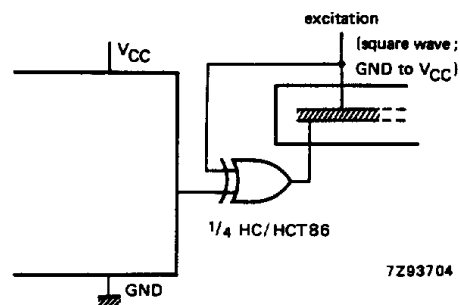


Fig.17 Connection to LCD display readout. (Direct DC drive is not recommended as it can shorten the life of LCD displays).

BCD to 7-segment latch/decoder/driver

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PACKAGE OUTLINES

See *"74HC/HCT/HCU/HCMOS Logic Package Outlines"*.

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Сотрудничество с глобальными дистрибьюторами электронных компонентов, предоставляет возможность заказывать и получать с международных складов практически любой перечень компонентов в оптимальные для Вас сроки.

На всех этапах разработки и производства наши партнеры могут получить квалифицированную поддержку опытных инженеров.

Система менеджмента качества компании отвечает требованиям в соответствии с ГОСТ Р ИСО 9001, ГОСТ РВ 0015-002 и ЭС РД 009

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