



Power MOSFET

PRODUCT SUMMARY

V_{DS} (V) at T_J max.	560	
$R_{DS(on)}$ (Ω)	$V_{GS} = 10$ V	1
Q_g (Max.) (nC)	34	
Q_{gs} (nC)	7.8	
Q_{gd} (nC)	10.4	
Configuration	Single	

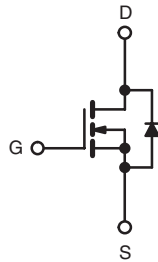
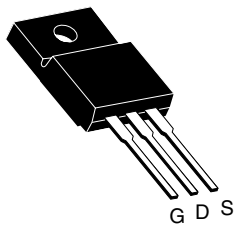
FEATURES

- Low Figure-of-Merit $R_{on} \times Q_g$
- 100 % Avalanche Tested
- Gate Charge Improved
- T_{rr}/Q_{rr} Improved
- Compliant to RoHS Directive 2002/95/EC



Available
RoHS*
COMPLIANT

TO-220 FULLPAK



N-Channel MOSFET

ORDERING INFORMATION

Package	TO-220 FULLPAK
Lead (Pb)-free	SiHF8N50L-E3

ABSOLUTE MAXIMUM RATINGS $T_C = 25^\circ\text{C}$, unless otherwise noted

PARAMETER	SYMBOL	LIMIT	UNIT
Drain-Source Voltage	V_{DS}	500	V
Gate-Source Voltage	V_{GS}	± 30	
Continuous Drain Current ^a	I_D	8	A
Pulsed Drain Current ^b	I_{DM}	22	
Linear Derating Factor		0.32	W/ $^\circ\text{C}$
Single Pulse Avalanche Energy ^c	E_{AS}	180	mJ
Maximum Power Dissipation	P_D	40	W
Peak Diode Recovery dV/dt ^d	dV/dt	24	V/ns
Operating Junction and Storage Temperature Range	T_J, T_{stg}	- 55 to + 150	$^\circ\text{C}$
Soldering Recommendations (Peak Temperature) ^e	for 10 s	300	

Notes

- Drain current limited by maximum junction temperature.
- Repetitive rating; pulse width limited by maximum junction temperature.
- $V_{DD} = 50$ V, starting $T_J = 25^\circ\text{C}$, $L = 10$ mH, $R_g = 25\ \Omega$, $I_{AS} = 6$ A.
- $I_{SD} \leq 8$ A, $dI/dt \leq 460$ A/ μs , $V_{DD} \leq V_{DS}$, $T_J \leq 150^\circ\text{C}$.
- 1.6 mm from case.

SiHF8N50L

Vishay Siliconix



THERMAL RESISTANCE RATINGS

PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient	R_{thJA}	-	65	°C/W
Maximum Junction-to-Case (Drain)	R_{thJC}	-	3.1	

SPECIFICATIONS $T_J = 25\text{ }^{\circ}\text{C}$, unless otherwise noted

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Drain-Source Breakdown Voltage	V _{DS}	V _{GS} = 0 V, I _D = 250 μA		500	-	-	V
V _{DS} Temperature Coefficient	ΔV _{DS} /T _J	Reference to 25 °C, I _D = 1 mA		-	0.5	-	V/°C
Gate-Source Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA		3.0	-	5.0	V
Gate-Source Leakage	I _{GSS}	V _{GS} = ± 30 V		-	-	± 100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 500 V, V _{GS} = 0 V		-	-	50	μA
		V _{DS} = 400 V, V _{GS} = 0 V, T _J = 125 °C		-	-	250	
Drain-Source On-State Resistance	R _{DS(on)}	V _{GS} = 10 V	I _D = 4.0 A	-	0.85	1	Ω
Forward Transconductance	g _{fs}	V _{DS} = 50 V, I _D = 3 A		-	2	-	S
Dynamic							
Input Capacitance	C _{iss}	V _{GS} = 0 V, V _{DS} = 25 V, f = 1.0 MHz		-	873	-	pF
Output Capacitance	C _{oss}			-	105	-	
Reverse Transfer Capacitance	C _{rss}			-	11	-	
Total Gate Charge	Q _g	V _{GS} = 0 V	I _D = 6 A, V _{DS} = 400 V	-	22	34	nC
Gate-Source Charge	Q _{gs}			-	7.8	-	
Gate-Drain Charge	Q _{gd}			-	10.4	-	
Turn-On Delay Time	t _{d(on)}	V _{DD} = 250 V, I _D = 6 A R _G = 14 Ω, V _{GS} = 10 V		-	17.3	-	ns
Rise Time	t _r			-	35	-	
Turn-Off Delay Time	t _{d(off)}			-	23.6	-	
Fall Time	t _f			-	17	-	
Gate Input Resistance	R _g	f = 1 MHz, open drain		-	0.7	-	Ω
Drain-Source Body Diode Characteristics							
Continuous Source-Drain Diode Current	I _S	MOSFET symbol showing the integral reverse p - n junction diode 		-	-	8	A
Pulsed Diode Forward Current	I _{SM}			-	-	22	
Body Diode Voltage	V _{SD}	T _J = 25 °C, I _S = 8 A, V _{GS} = 0 V		-	-	1.5	V
Body Diode Reverse Recovery Time	t _{rr}	T _J = 25 °C, I _F = I _S , dI/dt = 100 A/μs, V _R = 15 V		-	63	-	ns
Body Diode Reverse Recovery Charge	Q _{rr}			-	114	-	nC
Body Diode Reverse Recovery Current	I _{RRM}			-	3.3	-	A

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

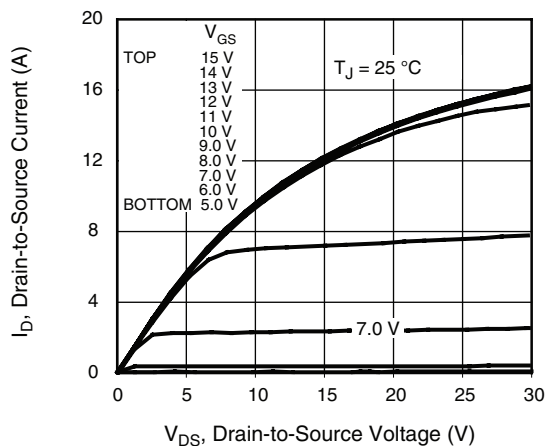


Fig. 1 - Typical Output Characteristics

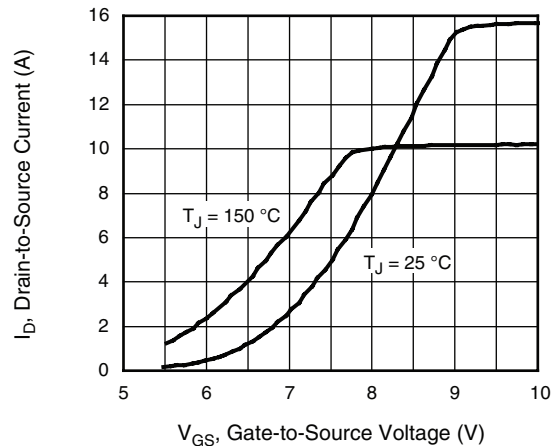


Fig. 3 - Typical Transfer Characteristics

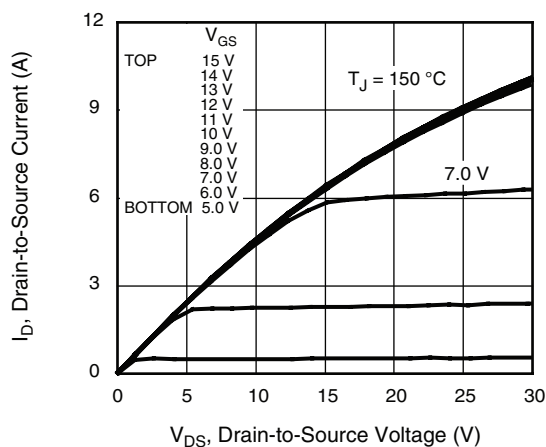


Fig. 2 - Typical Output Characteristics

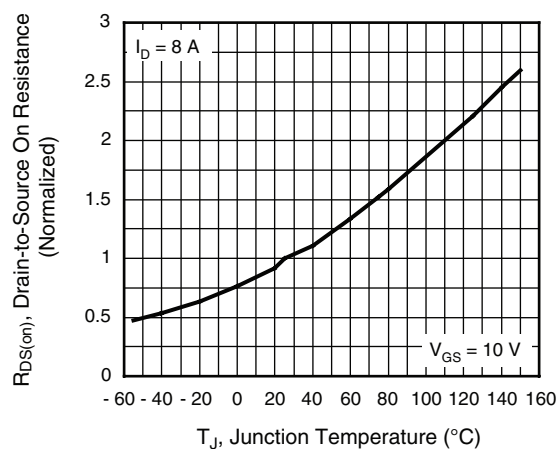


Fig. 4 - Normalized On-Resistance vs. Temperature

SiHF8N50L

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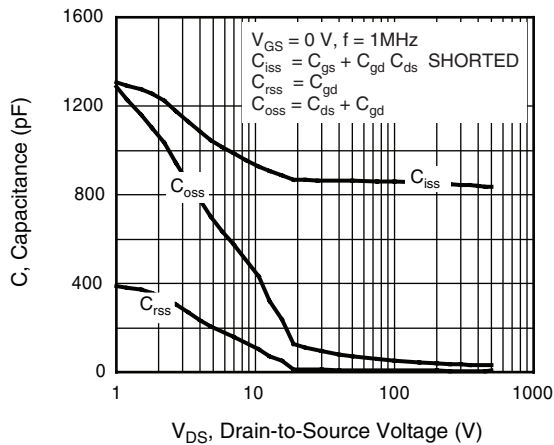


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

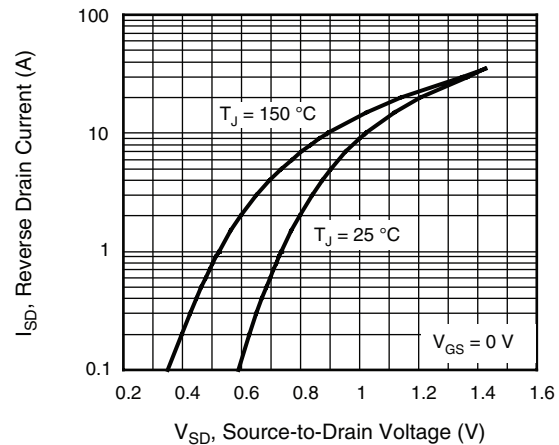


Fig. 7 - Typical Source-Drain Diode Forward Voltage

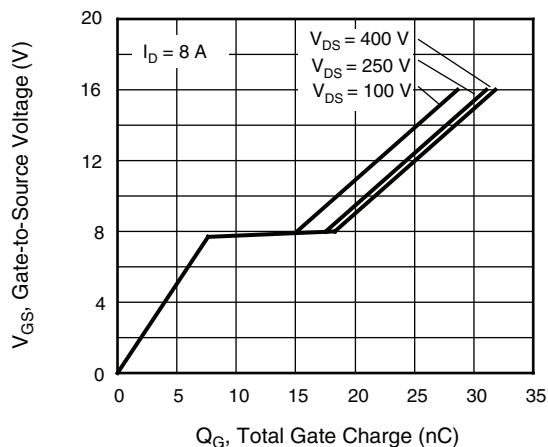


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

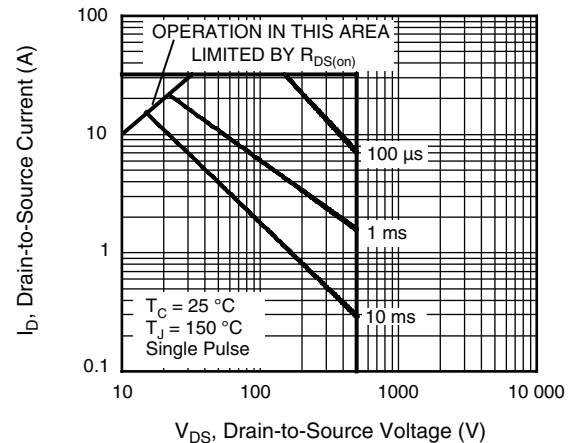


Fig. 8 - Maximum Safe Operating Area

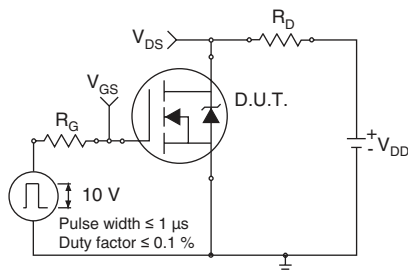


Fig. 9a - Switching Time Test Circuit

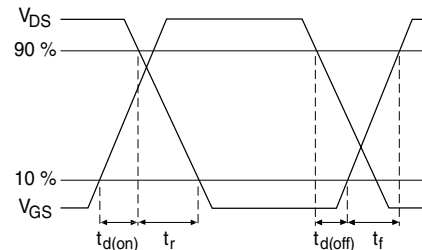


Fig. 9b - Switching Time Waveforms

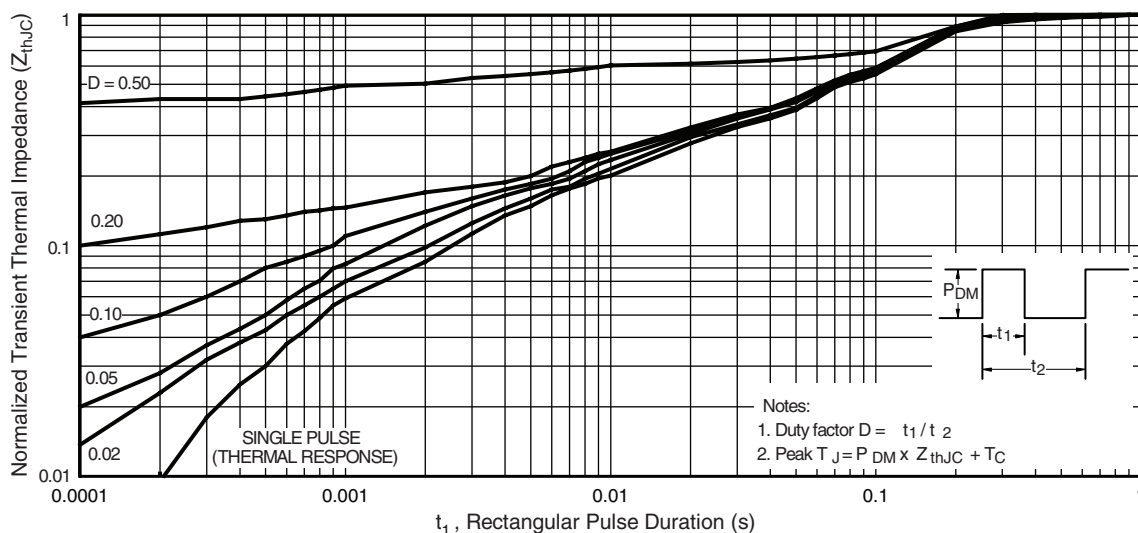


Fig. 10 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

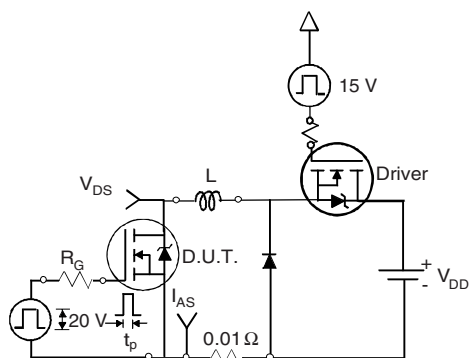


Fig. 11a - Unclamped Inductive Test Circuit

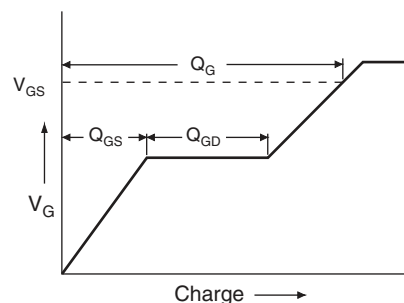


Fig. 12a - Basic Gate Charge Waveform

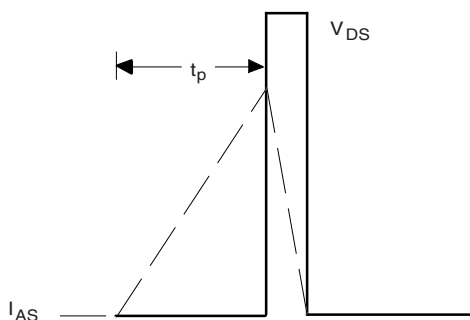


Fig. 11b - Unclamped Inductive Waveforms

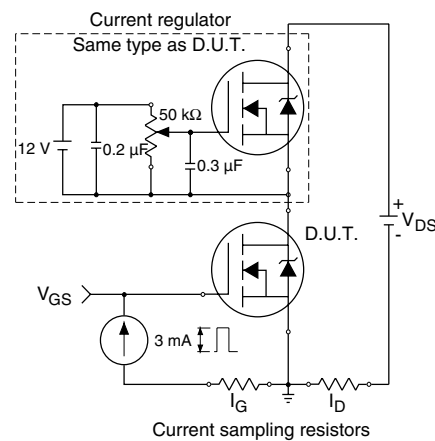


Fig. 12b - Gate Charge Test Circuit

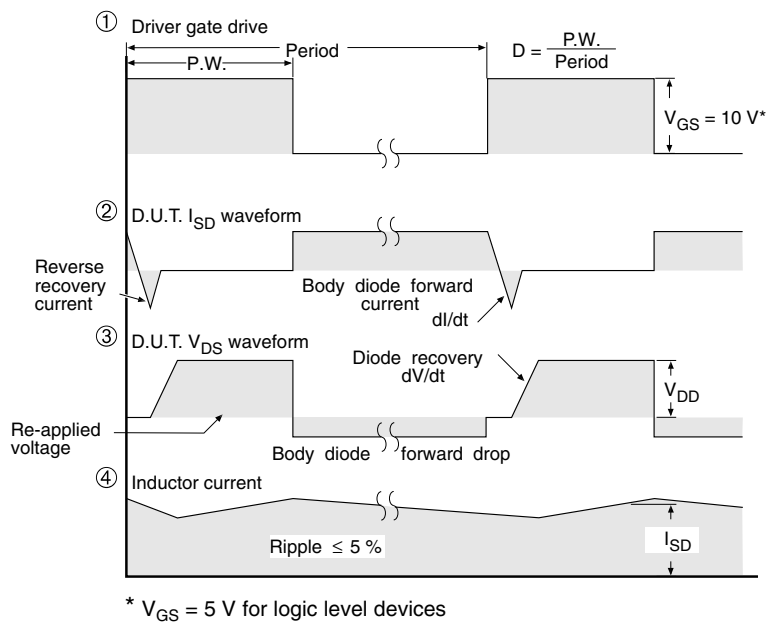
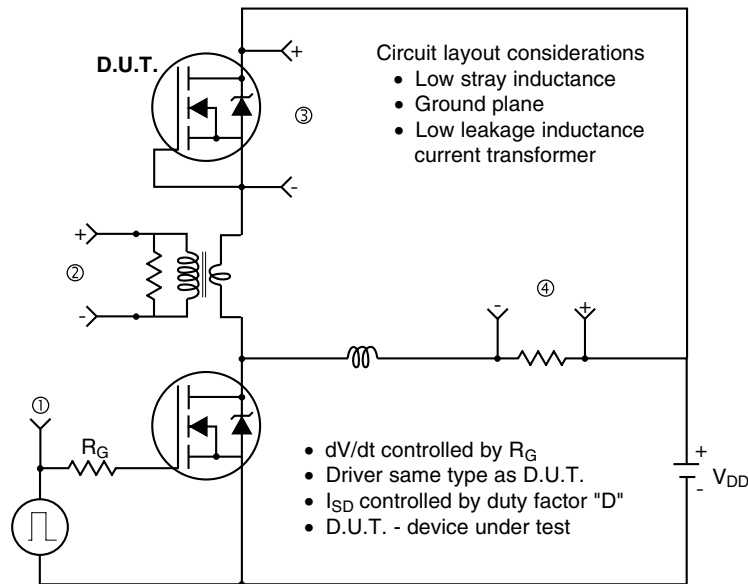
Peak Diode Recovery dV/dt Test Circuit

Fig. 13 - For N-Channel

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