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FDMS86182

September 2016

N-Channel Shielded Gate PowerTrench® MOSFET 100 V, 78 A, 7.2 m Ω

Features

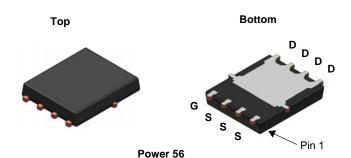
- Shielded Gate MOSFET Technology
- Max $r_{DS(on)} = 7.2 \text{ m}\Omega$ at $V_{GS} = 10 \text{ V}$, $I_D = 28 \text{ A}$
- Max $r_{DS(on)}$ = 19.5 m Ω at V_{GS} = 6 V, I_D = 14 A
- 50% Lower Qrr than Other MOSFET Suppliers
- Lowers Switching Noise/EMI
- MSL1 Robust Package Design
- 100% UIL Tested
- RoHS Compliant

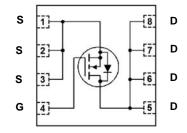
General Description

This N-Channel MV MOSFET is produced using Fairchild Semiconductor's advanced PowerTrench® process that incorporates Shielded Gate technology. This process has been optimized to minimize on-state resistance and yet maintain superior switching performance with best in class soft body diode.

Applications

- Primary DC-DC MOSFET
- Synchronous Rectifier in DC-DC and AC-DC
- Motor Drive
- Solar





MOSFET Maximum Ratings T_A = 25 °C unless otherwise noted.

Symbol	Param	eter		Ratings	Units
V _{DS}	Drain to Source Voltage			100	V
V_{GS}	Gate to Source Voltage			±20	V
	Drain Current -Continuous	T _C = 25 °C	(Note 5)	78	
	-Continuous	T _C = 100 °C	(Note 5)	49	^
ID	-Continuous	T _A = 25 °C	(Note 1a)	13	Α
	-Pulsed		(Note 4)	364	
E _{AS}	Single Pulse Avalanche Energy		(Note 3)	216	mJ
D	Power Dissipation	T _C = 25 °C		83	W
P_{D}	Power Dissipation	T _A = 25 °C	(Note 1a)	2.5	VV
T _J , T _{STG}	Operating and Storage Junction Tempera	ature Range		-55 to +150	°C

Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction to Case		1.5	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Not	te 1a)	50	C/VV

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDMS86182	FDMS86182	Power 56	13 "	12 mm	3000 units

Electrical Characteristics $T_J = 25$ °C unless otherwise noted.

Syllibol	i arameter	rest conditions	IAIIII.	ıyρ.	IVIAA.	Ullita
Off Chara	acteristics					
BV_{DSS}	Drain to Source Breakdown Voltage	$I_D = 250 \mu A, V_{GS} = 0 V$	100			V
$\Delta BV_{DSS} \over \Delta T_{J}$	Breakdown Voltage Temperature Coefficient	I_D = 250 μ A, referenced to 25 °C		56		mV/°C
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} = 80 V, V _{GS} = 0 V			1	μΑ
I_{GSS}	Gate to Source Leakage Current	$V_{GS} = \pm 20 \text{ V}, V_{DS} = 0 \text{ V}$			100	nA

On Characteristics

V _{GS(th)}	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}, I_{D} = 150 \mu A$	2.0	3.2	4.0	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	I_D = 150 μ A, referenced to 25 °C		-9		mV/°C
		V _{GS} = 10 V, I _D = 28 A		5.9	7.2	
r _{DS(on)}	Static Drain to Source On Resistance	$V_{GS} = 6 \text{ V}, I_D = 14 \text{ A}$		9.3	19.5	mΩ
, ,		$V_{GS} = 10 \text{ V}, I_D = 28 \text{ A}, T_J = 125 \text{ °C}$		9.9	12.1	
g _{FS}	Forward Transconductance	V _{DS} = 5 V, I _D = 28 A		63		S

Dynamic Characteristics

C _{iss}	Input Capacitance	V 50 V V 0 V		1880	2635	pF
C _{oss}	Output Capacitance	$V_{DS} = 50 \text{ V}, V_{GS} = 0 \text{ V},$ f = 1 MHz		1105	1550	pF
C _{rss}	Reverse Transfer Capacitance	1 - 1 1/11/12		13	25	pF
R_g	Gate Resistance		0.1	0.5	1.2	Ω

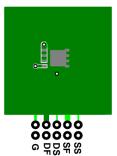
Switching Characteristics

t _{d(on)}	Turn-On Delay Time		13	24	ns
t _r	Rise Time	V _{DD} = 50 V, I _D = 28 A,	4	10	ns
t _{d(off)}	Turn-Off Delay Time	$V_{DD} = 50 \text{ V}, I_{D} = 28 \text{ A},$ $V_{GS} = 10 \text{ V}, R_{GEN} = 6 \Omega$	18	33	ns
t _f	Fall Time		4	10	ns
Q _q	Total Gate Charge	V _{GS} = 0 V to 10 V	26	37	nC
Q_q	Total Gate Charge	$V_{GS} = 0 \text{ V to 6 V}$ $V_{DD} = 50 \text{ V},$	17	24	nC
Q_{gs}	Gate to Source Charge	I _D = 28 A	8.2		nC
Q_{gd}	Gate to Drain "Miller" Charge		5.1		nC
Q _{oss}	Output Charge	V _{DD} = 50 V, V _{GS} = 0 V	73		nC

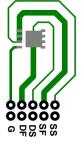
Drain-Source Diode Characteristics

V _{SD}	Source to Drain Diode Forward Voltage	$V_{GS} = 0 \text{ V}, I_S = 2.1 \text{ A}$ (Note	2)	0.7	1.2	V
	Source to Drain Diode Polward Voltage	$V_{GS} = 0 \text{ V}, I_S = 28 \text{ A}$ (Note	2)	0.8	1.3	
t _{rr}	Reverse Recovery Time	I _F = 14 A, di/dt = 300 A/μs		28	45	ns
Q _{rr}	Reverse Recovery Charge	-1 _F = 14 A, α/αι = 300 A/μs		52	84	nC
t _{rr}	Reverse Recovery Time	I _E = 14 A, di/dt = 1000 A/μs		22	36	ns
Q _{rr}	Reverse Recovery Charge	- 1 _F = 14 A, di/dt = 1000 A/μs		116	186	nC

^{1.} R_{BJA} is determined with the device mounted on a 1 in² pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material. R_{BCA} is determined by the user's board design.



a) 50 °C/W when mounted on a 1 in² pad of 2 oz copper



b) 125 °C/W when mounted on a minimum pad of 2 oz copper.

- 2. Pulse Test: Pulse Width < 300 µs, Duty cycle < 2.0%.
 3. E_{AS} of 216 mJ is based on starting T_J = 25 °C; N-ch: L = 3 mH, I_{AS} = 12 A, V_{DD} = 100 V, V_{GS} =10 V. 100% test at L = 0.1 mH, I_{AS} = 38 A.
 4. Pulsed Id please refer to Fig 11 SOA graph for more details.
 5. Computed continuous current limited to Max Junction Temperature only, actual continuous current will be limited by thermal & electro-mechanical application board design.

Typical Characteristics $T_J = 25$ °C unless otherwise noted.

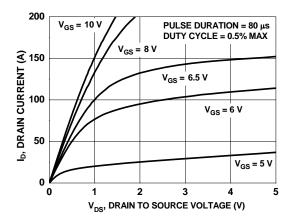


Figure 1. On-Region Characteristics

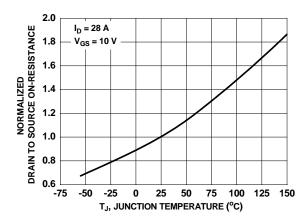


Figure 3. Normalized On-Resistance vs. Junction Temperature

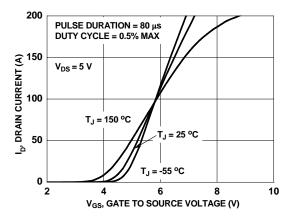


Figure 5. Transfer Characteristics

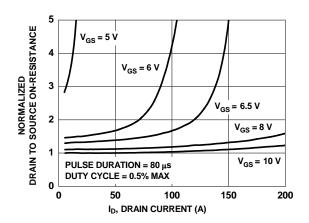


Figure 2. Normalized On-Resistance vs. Drain Current and Gate Voltage

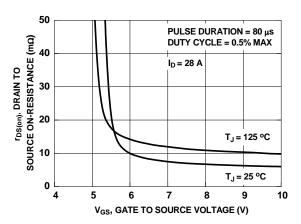


Figure 4. On-Resistance vs. Gate to Source Voltage

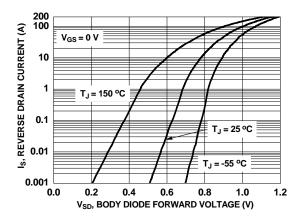


Figure 6. Source to Drain Diode Forward Voltage vs. Source Current

Typical Characteristics $T_J = 25$ °C unless otherwise noted.

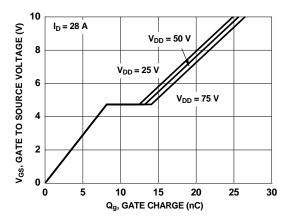


Figure 7. Gate Charge Characteristics

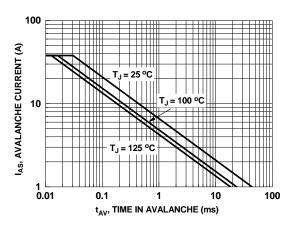


Figure 9. Unclamped Inductive Switching Capability

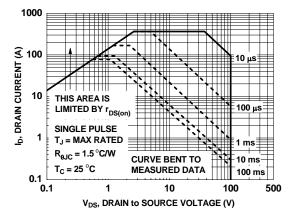


Figure 11. Forward Bias Safe Operating Area

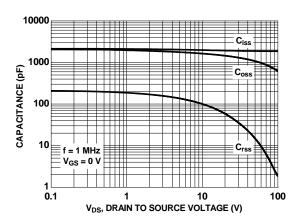


Figure 8. Capacitance vs. Drain to Source Voltage

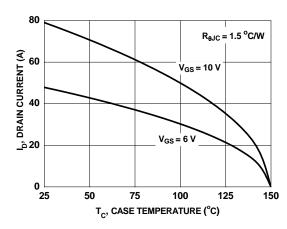


Figure 10. Maximum Continuous Drain Current vs. Case Temperature

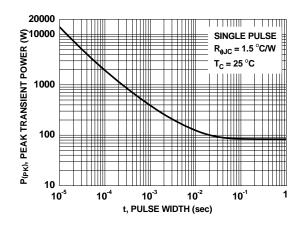


Figure 12. Single Pulse Maximum Power Dissipation

Typical Characteristics $T_J = 25 \, ^{\circ}\text{C}$ unless otherwise noted.

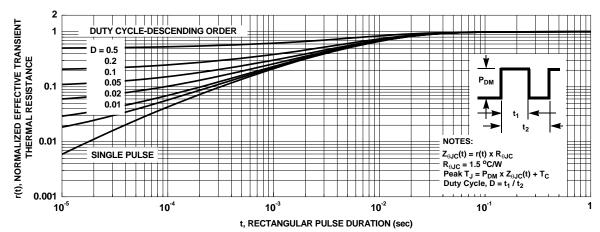


Figure 13. Junction-to-Case Transient Thermal Response Curve



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