

4 OUTPUT PCIE GEN1/2 SYNTHESIZER

IDT5V41066

Recommended Applications

4 Output synthesizer for PCIe Gen1/2

General Description

The IDT5V41066 is a PCIe Gen2 compliant spread-spectrum-capable clock generator. The device has 4 differential HCSL outputs and can be used in communication or embedded systems to substantially reduce electro-magnetic interference (EMI). The spread amount and output frequency are selectable via select pins.

Output Features

- 4 - 0.7V current mode differential HCSL output pairs

Features/Benefits

- 20-pin TSSOP package; small board footprint
- Spread-spectrum capable; reduces EMI
- Outputs can be terminated to LVDS; can drive a wider variety of devices
- Power down pin; greater system power management
- OE control pin; greater system power management
- Spread% and frequency pin selection; no software required to configure device
- Industrial temperature range available; supports demanding embedded applications
- **For PCIe Gen3 applications, see the 5V41236**

Key Specifications

- Cycle-to-cycle jitter < 100 ps
- Output-to-output skew < 50 ps
- PCIe Gen2 phase jitter < 3.0ps RMS

Block Diagram



Pin Assignment



20-pin (173 mil) TSSOP

Spread Spectrum Selection Table

| S2 | S1 | S0 | Spread% | Spread Type | Output Frequency |
|----|----|----|-----------|----------------|------------------|
| 0 | 0 | 0 | -0.5 | Down | 100 |
| 0 | 0 | 1 | -1.0 | Down | 100 |
| 0 | 1 | 0 | -1.5 | Down | 100 |
| 0 | 1 | 1 | No Spread | Not Applicable | 100 |
| 1 | 0 | 0 | -0.5 | Down | 200 |
| 1 | 0 | 1 | -1.0 | Down | 200 |
| 1 | 1 | 0 | -1.5 | Down | 200 |
| 1 | 1 | 1 | No Spread | Not Applicable | 200 |

Pin Descriptions

| Pin | Pin Name | Pin Type | Pin Description |
|-----|----------|----------|--|
| 1 | VDDXD | Power | Connect to +3.3 V digital supply. |
| 2 | S0 | Input | Spread spectrum select pin #0. See table above. Internal pull-up resistor. |
| 3 | S1 | Input | Spread spectrum select pin #1. See table above. Internal pull-up resistor. |
| 4 | S2 | Input | Spread spectrum select pin #2. See table above. Internal pull-up resistor. |
| 5 | X1 | Input | Crystal connection. Connect to a fundamental mode crystal or clock input. |
| 6 | X2 | Output | Crystal connection. Connect to a fundamental mode crystal or leave open. |
| 7 | PD | Input | Powers down all PLL's and tri-states outputs when low. Internal pull-up resistor. |
| 8 | OE | Input | Provides output on, tri-states output (High = enable outputs; Low = disable outputs). Internal pull-up resistor. |
| 9 | GND | Power | Connect to digital ground. |
| 10 | IREF | Output | Precision resistor attached to this pin is connected to the internal current reference. |
| 11 | CLKD | Output | Selectable 100/200 MHz spread spectrum differential Complement output clock D. |
| 12 | CLKD | Output | Selectable 100/200 MHz spread spectrum differential True output clock D. |
| 13 | CLKC | Output | Selectable 100/200 MHz spread spectrum differential Complement output clock C. |
| 14 | CLKC | Output | Selectable 100/200 MHz spread spectrum differential True output clock C. |
| 15 | VDDODA | Power | Connect to +3.3 V analog supply. |
| 16 | GND | Power | Connect to analog ground. |
| 17 | CLKB | Output | Selectable 100/200 MHz spread spectrum differential Complement output clock B. |
| 18 | CLKB | Output | Selectable 100/200 MHz spread spectrum differential True output clock B. |
| 19 | CLKA | Output | Selectable 100/200 MHz spread spectrum differential Complement output clock A. |
| 20 | CLKA | Output | Selectable 100/200 MHz spread spectrum differential True output clock A. |

Application Information

Decoupling Capacitors

As with any high-performance mixed-signal IC, the IDT5V41066 must be isolated from system power supply noise to perform optimally.

Decoupling capacitors of 0.01 μ F must be connected between each VDD and the PCB ground plane.

PCB Layout Recommendations

For optimum device performance and lowest output phase noise, the following guidelines should be observed.

Each 0.01 μ F decoupling capacitor should be mounted on the component side of the board as close to the VDD pin as possible. No vias should be used between decoupling capacitor and VDD pin. The PCB trace to VDD pin should be kept as short as possible, as should the PCB trace to the ground via. Distance of the ferrite bead and bulk decoupling from the device is less critical.

2) An optimum layout is one with all components on the same side of the board, minimizing vias through other signal layers (the ferrite bead and bulk decoupling capacitor can be mounted on the back). Other signal traces should be routed away from the IDT5V41066.

This includes signal traces just underneath the device, or on layers adjacent to the ground plane layer used by the device.

External Components

A minimum number of external components are required for proper operation. Decoupling capacitors of 0.01 μ F should be connected between VDD and GND pairs (1,9 and 15,16) as close to the device as possible.

On chip capacitors- Crystal capacitors should be connected from pins X1 to ground and X2 to ground to optimize the initial accuracy. The value (in pf) of these crystal caps equal $(C_L - 12) * 2$ in this equation, C_L = crystal load capacitance in pf. For example, for a crystal with a 16 pF load cap, each external crystal cap would be 8 pF.
 $[(16 - 12) * 2] = 8$.

Current Reference Source R_r (I_{ref})

If board target trace impedance (Z) is 50 Ω , then $R_r = 475\Omega$ (1%), providing IREF of 2.32 mA, output current (I_{OH}) is equal to 6*IREF.

Load Resistors R_L

Since the clock outputs are open source outputs, 50 ohm external resistors to ground are to be connected at each clock output.

Output Termination

The PCI-Express differential clock outputs of the IDT5V41066 are open source drivers and require an external series resistor and a resistor to ground. These resistor values and their allowable locations are shown in detail in the **PCI-Express Layout Guidelines** section.

The IDT5V41066 can also be configured for LVDS compatible voltage levels. See the **LVDS Compatible Layout Guidelines** section.

Output Structures



General PCB Layout Recommendations

For optimum device performance and lowest output phase noise, the following guidelines should be observed.

1. Each $0.01 \mu\text{F}$ decoupling capacitor should be mounted on the component side of the board as close to the VDD pin as possible.
2. No vias should be used between decoupling capacitor and VDD pin.
3. The PCB trace to VDD pin should be kept as short as possible, as should the PCB trace to the ground via. Distance of the ferrite bead and bulk decoupling from the device is less critical.
4. An optimum layout is one with all components on the same side of the board, minimizing vias through other signal layers (any ferrite beads and bulk decoupling capacitors can be mounted on the back). Other signal traces should be routed away from the IDT5V41066. This includes signal traces just underneath the device, or on layers adjacent to the ground plane layer used by the device.

Layout Guidelines

| SRC Reference Clock | | | |
|---|--------------------|------|--------|
| Common Recommendations for Differential Routing | Dimension or Value | Unit | Figure |
| L1 length, route as non-coupled 50ohm trace | 0.5 max | inch | 1 |
| L2 length, route as non-coupled 50ohm trace | 0.2 max | inch | 1 |
| L3 length, route as non-coupled 50ohm trace | 0.2 max | inch | 1 |
| Rs | 33 | ohm | 1 |
| Rt | 49.9 | ohm | 1 |

| Down Device Differential Routing | | | |
|--|---------------------|------|---|
| L4 length, route as coupled microstrip 100ohm differential trace | 2 min to 16 max | inch | 1 |
| L4 length, route as coupled stripline 100ohm differential trace | 1.8 min to 14.4 max | inch | 1 |

| Differential Routing to PCI Express Connector | | | |
|--|-----------------------|------|---|
| L4 length, route as coupled microstrip 100ohm differential trace | 0.25 to 14 max | inch | 2 |
| L4 length, route as coupled stripline 100ohm differential trace | 0.225 min to 12.6 max | inch | 2 |

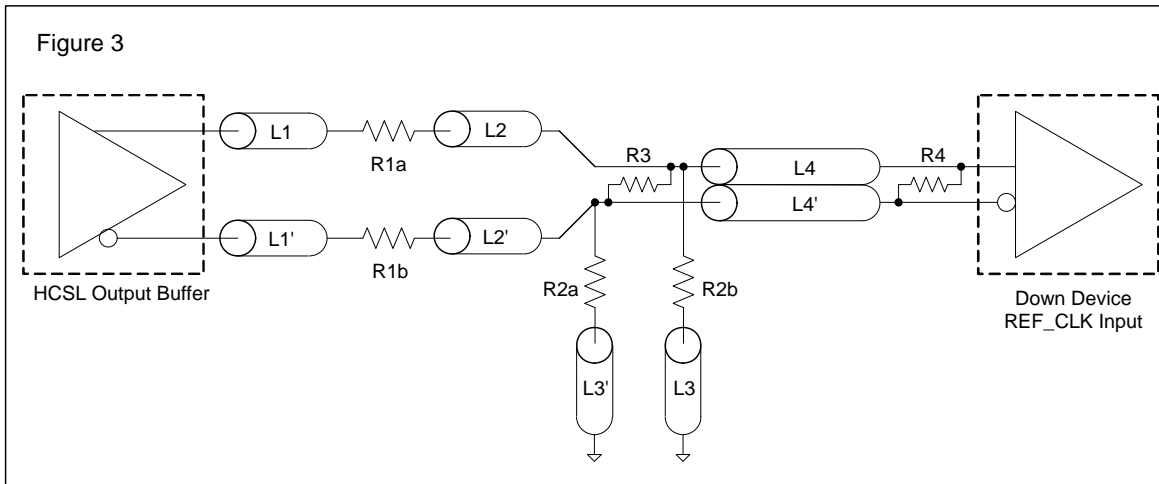


Alternative Termination for LVDS and other Common Differential Signals (figure 3)

| Vdiff | Vp-p | Vcm | R1 | R2 | R3 | R4 | Note |
|-------|-------|------|----|------|------|-----|--------------------------------|
| 0.45v | 0.22v | 1.08 | 33 | 150 | 100 | 100 | |
| 0.58 | 0.28 | 0.6 | 33 | 78.7 | 137 | 100 | |
| 0.80 | 0.40 | 0.6 | 33 | 78.7 | none | 100 | ICS874003i-02 input compatible |
| 0.60 | 0.3 | 1.2 | 33 | 174 | 140 | 100 | Standard LVDS |

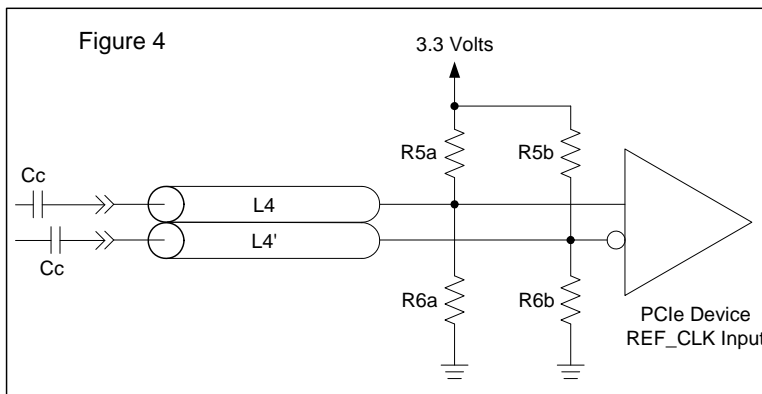
R1a = R1b = R1

R2a = R2b = R2



Cable Connected AC Coupled Application (figure 4)

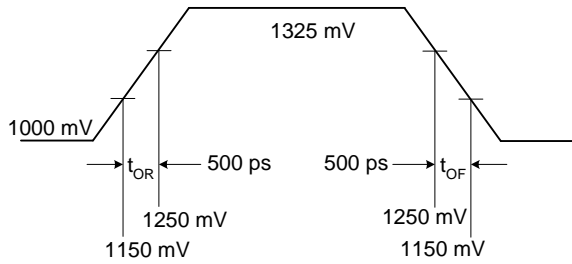
| Component | Value | Note |
|-----------|-------------|------|
| R5a, R5b | 8.2K 5% | |
| R6a, R6b | 1K 5% | |
| Cc | 0.1 μF | |
| Vcm | 0.350 volts | |



Typical PCI-Express (HCSL) Waveform



Typical LVDS Waveform



Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the IDT5V41066. These ratings are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

| Item | Rating |
|--|---------------------|
| Supply Voltage, VDD, VDDA | 5.5 V |
| All Inputs and Outputs | -0.5 V to VDD+0.5 V |
| Ambient Operating Temperature (commercial) | 0 to +70° C |
| Ambient Operating Temperature (industrial) | -40 to +85° C |
| Storage Temperature | -65 to +150° C |
| Junction Temperature | 125° C |
| Soldering Temperature | 260° C |
| ESD Protection (Input) | 2000 V min. (HBM) |

DC Electrical Characteristics

Unless stated otherwise, VDD = 3.3 V \pm 5%, Ambient Temperature -40 to +85° C

| Parameter | Symbol | Conditions | Min. | Typ. | Max. | Units |
|------------------------------------|-------------------|--|---------|------|----------|------------|
| Supply Voltage | V | | 3.135 | 3.3 | 3.465 | |
| Input High Voltage ¹ | V _{IH} | | 2.2 | | VDD +0.3 | V |
| Input Low Voltage ¹ | V _{IL} | | VSS-0.3 | | 0.8 | V |
| Input Leakage Current ² | I _{IL} | 0 < V _{in} < VDD | -5 | | 5 | μ A |
| Operating Supply Current @ 100 MHz | I _{DD} | R _S =33 Ω , R _P =50 Ω , C _L =2 pF | | 115 | 125 | mA |
| | I _{DDOE} | OE =Low | | 42 | 48 | mA |
| | I _{DDPD} | No load, \overline{PD} =Low | | 350 | 500 | μ A |
| Input Capacitance | C _{IN} | Input pin capacitance | | | 7 | pF |
| Output Capacitance | C _{OUT} | Output pin capacitance | | | 6 | pF |
| X1, X2 Capacitance | C _{INX} | | | | 5 | pF |
| Pin Inductance | L _{PIN} | | | | 5 | nH |
| Output Impedance | Z _o | CLK outputs | 3.0 | | | k Ω |
| Pull-up Resistance | R _{PUP} | OE, SEL, \overline{PD} pins | | 110 | | k Ω |

1. Single edge is monotonic when transitioning through region.
2. Inputs with pull-ups/-downs are not included.

AC Electrical Characteristics - CLKOUT (A:D)

Unless stated otherwise, $V_{DD}=3.3\text{ V} \pm 5\%$, Ambient Temperature -40 to +85° C

| Parameter | Symbol | Conditions | Min. | Typ. | Max. | Units |
|---|--------------|--|------|------|------|-------|
| Input Frequency | | | | 25 | | MHz |
| Output Frequency | | HCSL termination | 25 | | 200 | MHz |
| | | LVDS termination | 25 | | 100 | MHz |
| Output High Voltage ^{1,2} | V_{OH} | HCSL | | | 850 | mV |
| Output Low Voltage ^{1,2} | V_{OL} | HCSL | -150 | | | mV |
| Crossing Point Voltage ^{1,2} | | Absolute | 250 | | 550 | mV |
| Crossing Point Voltage ^{1,2,4} | | Variation over all edges | | | 140 | mV |
| Jitter, Cycle-to-Cycle ^{1,3} | | | | | 100 | ps |
| Frequency Synthesis Error | | All outputs | | 0 | | ppm |
| Modulation Frequency | | Spread spectrum | 30 | 32.9 | 33 | kHz |
| Rise Time ^{1,2} | t_{OR} | From 0.175 V to 0.525 V | 175 | | 700 | ps |
| Fall Time ^{1,2} | t_{OF} | From 0.525 V to 0.175 V | 175 | | 700 | ps |
| Rise/Fall Time Variation ^{1,2} | | | | | 125 | ps |
| Output to Output Skew | | | | | 50 | ps |
| Duty Cycle ^{1,3} | | | 45 | | 55 | % |
| Output Enable Time ⁵ | | All outputs | | 50 | 100 | ns |
| Output Disable Time ⁵ | | All outputs | | 50 | 100 | ns |
| Stabilization Time | t_{STABLE} | From power-up $V_{DD}=3.3\text{ V}$ | | | 1.8 | ms |
| Spread Spectrum Transition Time | t_{SPREAD} | Stabilization time after spread spectrum changes | 7 | | 30 | ms |

¹ Test setup is $R_S=33\Omega$, $R_P=50\Omega$ with $C_L=2\text{ pF}$, $R_r = 475\Omega$ (1%).

² Measurement taken from a single-ended waveform.

³ Measurement taken from a differential waveform.

⁴ Measured at the crossing point where instantaneous voltages of both CLKOUT and $\overline{\text{CLKOUT}}$ are equal.

⁵ CLKOUT pins are tri-stated when OE is asserted low. CLKOUT is driven differential when OE is high unless its $\overline{\text{PD}}$ is low.

Electrical Characteristics - Differential Phase Jitter

| Parameter | Symbol | Conditions | Min | Typ | Max | Units | Notes |
|---------------|-------------------------|---|-----|------|-----|----------|-------|
| Jitter, Phase | $t_{j\text{phasePLL}}$ | PCIe Gen1 | | 30 | 86 | ps (p-p) | 1,2,3 |
| | $t_{j\text{phaseLO}}$ | PCIe Gen2, 10 kHz < f < 1.5 MHz | | 0.76 | 3 | ps (RMS) | 1,2,3 |
| | $t_{j\text{phaseHIGH}}$ | PCIe Gen2, 1.5 MHz < f < Nyquist (50 MHz) | | 2.0 | 3.1 | ps (RMS) | 1,2,3 |

Note 1. Guaranteed by design and characterization, not 100% tested in production.

Note 2. See <http://www.pcisig.com> for complete specs.

Note 3: Applies to 100MHz, spread off and 0.5% down spread only.

Thermal Characteristics

| Parameter | Symbol | Conditions | Min. | Typ. | Max. | Units |
|--|---------------|----------------|------|------|------|-------|
| Thermal Resistance Junction to Ambient | θ_{JA} | Still air | | 93 | | °C/W |
| | θ_{JA} | 1 m/s air flow | | 78 | | °C/W |
| | θ_{JA} | 3 m/s air flow | | 65 | | °C/W |
| Thermal Resistance Junction to Case | θ_{JC} | | | 20 | | °C/W |

Marking Diagram (5V41066PGG)



Marking Diagram (5V41066PGGI)



Notes:

1. Line 1 and 2: IDT part number.
2. Line 3: # – Die revision; YYWW – Date code; \$ – Assembly location.
3. “G” after the two-letter package code designates RoHS compliant package.
4. “I” at the end of part number indicates industrial temperature range.
5. Bottom marking: country of origin if not USA.

Package Outline and Package Dimensions (20-pin TSSOP, 173 mil Body)

Package dimensions are kept current with JEDEC Publication No. 95, MO-153



| Symbol | Millimeters | | Inches* | |
|--------|-------------|------|--------------|-------|
| | Min | Max | Min | Max |
| A | | 1.20 | | 0.047 |
| A1 | 0.05 | 0.15 | 0.002 | 0.006 |
| A2 | 0.80 | 1.05 | 0.032 | 0.041 |
| b | 0.19 | 0.30 | 0.007 | 0.012 |
| c | 0.09 | 0.20 | 0.0035 | 0.008 |
| D | 6.40 | 6.60 | 0.252 | 0.260 |
| E | 6.40 BASIC | | 0.252 BASIC | |
| E1 | 4.30 | 4.50 | 0.169 | 0.177 |
| e | 0.65 Basic | | 0.0256 Basic | |
| L | 0.45 | 0.75 | 0.018 | 0.030 |
| a | 0° | 8° | 0° | 8° |
| aaa | -- | 0.10 | -- | 0.004 |

Ordering Information

| Part / Order Number | Marking | Shipping Packaging | Package | Temperature |
|---------------------|-------------|--------------------|--------------|---------------|
| 5V41066PGG | see page 10 | Tubes | 20-pin TSSOP | 0 to +70° C |
| 5V41066PGG8 | | Tape and Reel | 20-pin TSSOP | 0 to +70° C |
| 5V41066PGGI | | Tubes | 20-pin TSSOP | -40 to +85° C |
| 5V41066PGGI8 | | Tape and Reel | 20-pin TSSOP | -40 to +85° C |

“G” after the two-letter package code are the Pb-Free configuration and are RoHS compliant.

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Revision History

| Rev. | Originator | Date | Description of Change |
|------|------------|----------|---|
| A | RDW | 01/20/10 | New datasheet; Preliminary initial release. |
| B | RDW | 04/27/10 | Updated electrical tables per char; released to final. |
| C | RDW | 07/19/10 | 1. Updated title and general description 2. Updated cycle-to-cycle jitter spec from 125 to 100 ps. |
| D | RDW | 11/21/11 | 1. Changed title to "4 Output PCIe GEN1/2 Synthesizer" 2. Added note to Features section: "For PCIe Gen3 applications, see 5V41236" 3. Updated Differential Phase Jitter table. |

IDT5V41066

4 OUTPUT PCIE GEN1/2 SYNTHESIZER

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