±2.5°C Low-Power, Analog Out TEMPERATURE SENSOR

Check for Samples: TMP20

FEATURES

- **±2.5°C ACCURACY FROM –55°C to +130°C**
- **SUPPLY VOLTAGE RANGE: 1.8V to 5.5V**
- **LOW POWER: 4µA (max)**
- ***Micro*SIZE PACKAGES: SOT563, SC70-5**
- **SC70 PIN-COMPATIBLE WITH LM20**

APPLICATIONS

- **CELL PHONES**
- **DESKTOP AND NOTEBOOK COMPUTERS**
- **PORTABLE DEVICES**
- **CONSUMER ELECTRONICS**
- **BATTERY MANAGEMENT**
- **POWER SUPPLIES**
- **HVAC**
- **THERMAL MONITORING**
- **DISK DRIVES**
- **APPLIANCES/WHITE GOODS**
- **AUTOMOTIVE**

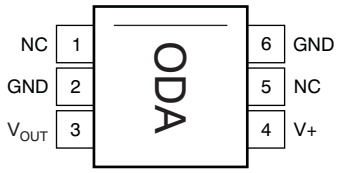
DESCRIPTION

The TMP20 is a CMOS, precision analog output temperature sensor available in the tiny SOT563 package. The TMP20 operates from –55°C to +130°C on a supply voltage of 2.7V to 5.5V with a supply current of 4µA. Operation as low as 1.8V is possible for temperatures between +15°C and +130°C. The linear transfer function has a slope of –11.77mV/°C (typ) and has an output voltage of 1.8639V (typ) at 0°C. The TMP20 has a ±2.5°C accuracy across the entire specified temperature range of –55°C to +130°C.

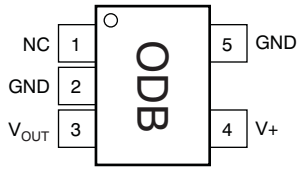
The TMP20 4µA (max) supply current limits self-heating of the device to less than 0.01°C. When V+ is less than 0.5V, the device is in shutdown mode and consumes less than 20nA (typ).

The TMP20 is available in either a 5-lead SC70 or 6-lead SOT563 package, reducing the overall board space required.

DRL PACKAGE
SOT563-6
(TOP VIEW)



DCK PACKAGE
SC70-5
(TOP VIEW)



Note: NC or no-connect pin must be grounded or left floating. Pin 2 on the DRL package has no internal connection; pin 2 on the DCK package is connected to the die substrate. See Layout Information for more information about optimizing the connection of pin 2 on the DCK package for thermal and electrical performance.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE INFORMATION(1)

PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR	PACKAGE MARKING
TMP20	SC70-5	DCK	ODB
TMP20	SOT563-6	DRL	ODA

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

ABSOLUTE MAXIMUM RATINGS(1)

Over operating free-air temperature range, unless otherwise noted.

		TMP20	UNIT
Supply Voltage, V+		+7.0	V
Operating Temperature Range		–55 to +150	°C
Storage Temperature Range		–65 to +150	°C
Junction Temperature (T_J max)		+150	°C
ESD Rating	Human Body Model (HBM)	4000	V
	Charged Device Model (CDM)	1000	V
	Machine Model (MM)	200	V

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.

ELECTRICAL CHARACTERISTICS

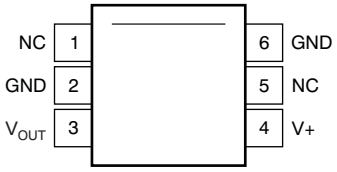
At T_A = +25°C and V+ = 2.7V to 5.5V, unless otherwise noted.

PARAMETER		CONDITIONS	TMP20 MIN	TMP20 TYP	TMP20 MAX	UNIT
TEMPERATURE MEASUREMENT(1)						
Accuracy(2)		T_A = –55°C to +130°C	–2.5		+2.5	°C
vs Supply		V+ = 1.8V to +5.5V, at T_A = +15°C to +130°C	–.0.05		+0.05	°C/V
		V+ = 2.7V to +5.5V, at T_A = –50°C to +130°C	–.0.05		+0.05	°C/V
Temperature Sensitivity(3)		T_A = –30°C to +100°C	–11.4	—11.77	–12.2	mV/°C
Output Voltage(4)						
		T_A = 0°C		1863.9		mV
		T_A = +25°C		1574		mV
Nonlinearity(5)		–20°C ≤ T_A ≤ +80°C		±0.4		%
ANALOG OUTPUT						
Output Resistance		–600µA ≤ I_{LOAD} ≤ 600µA		10		Ω
Load Regulation		–600µA ≤ I_{LOAD} ≤ 600µA		6		mV
Maximum Capacitive Load			1			nF
POWER SUPPLY						
Specified Voltage Range	V_S	T_A = –55°C to +130°C	2.7		5.5	V
		T_A = +15°C to +130°C(6)	1.8		5.5	V
Quiescent Current	I_Q	V+ = 5.5V, T_A = +25°C		2.6	4	µA
over Temperature		V+ = 5.5V, T = –55°C to +130°C			6	µA
Shutdown Current	I_{SD}	V+ < 0.5V		20		nA
TEMPERATURE RANGE						
Specified Operating Range		V+ = 2.7V to 5.5V	–55		+130	°C
		V+ = 1.8V to 5.5V(6)	+15		+130	°C
Operating Range		V+ = 2.7V to 5.5V	–55		+150	°C
Thermal Resistance	θ_{JA}					
SC70				185		°C/W
SOT563				238		°C/W
Self-Heating						
SC70					0.01	°C
SOT563					0.01	°C

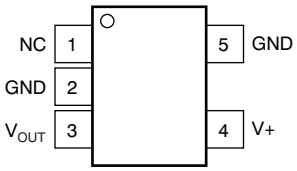
(1) 100% production tested at T_A = +25°C. Specifications over temperature range are assured by design.
(2) Power-supply rejection is encompassed in the accuracy specification.
(3) Temperature sensitivity is the average slope to the equation V_O = (–11.77 × T) + 1.860V.
(4) V_{OUT} is calculated from temperature with the following equation:
$V_O = (–3.88 \times 10^{–6} \times T^2) + (–1.15 \times 10^{–2} \times T) + 1.8639V$,
where T is in °C.
(5) Nonlinearity is the deviation of the calculated output voltage from the best fit straight line.
(6) The TMP20 transfer function requires the output voltage to rise above the 1.8V supply as the temperature decreases below +15°C. When operating at a 1.8V supply, it is normal for the TMP20 output to approach 1.8V and remain at that voltage as the temperature continues to decrease below +15°C. This condition does not damage the device. Once the temperature rises above +15°C, the output voltage resumes changing as the temperature changes, according to the transfer function specified in this document. For more information about the transfer function, see the *Transfer Function* section.

PIN CONFIGURATIONS

DRL PACKAGE
SOT563-6
(TOP VIEW)



DCK PACKAGE
SC70-5
(TOP VIEW)



Note: NC or no-connect pin must be grounded or left floating.

TMP20 PIN ASSIGNMENTS

TMP20			DESCRIPTION
PIN NAME	**DRL PACKAGE**	**DCK PACKAGE**	
NC	1	1	This pin must be grounded or left floating. See Layout Information for more information.
NC or GND	2, 5	2	This pin must be grounded or left floating. For best thermal response, connect to GND plane. See Layout Information for more information.
V_{OUT}	3	3	Analog output.
V+	4	4	Positive supply voltage.
GND	6	5	Ground pin.

TYPICAL CHARACTERISTICS

OUTPUT IMPEDANCE vs TEMPERATURE

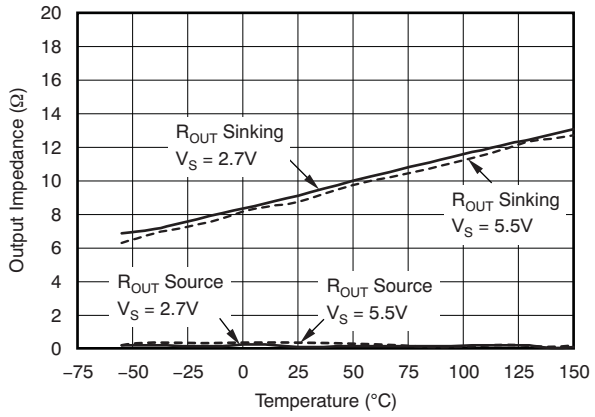


Figure 1.

QUIESCENT CURRENT vs TEMPERATURE

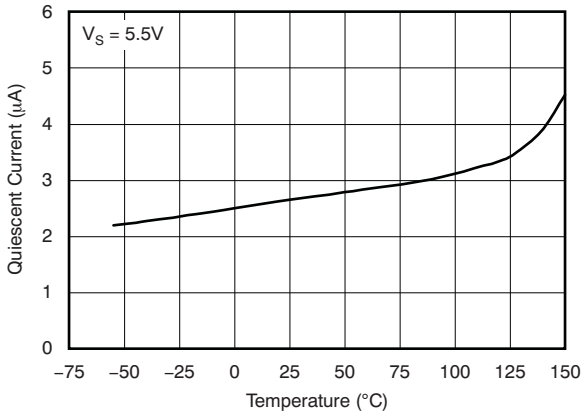


Figure 2.

OUTPUT VOLTAGE vs TEMPERATURE

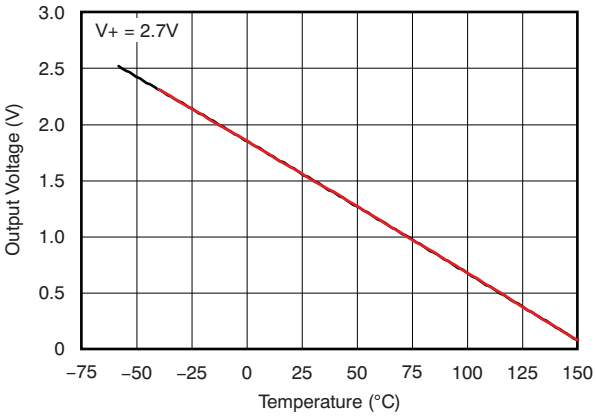


Figure 3.

QUIESCENT CURRENT vs SUPPLY VOLTAGE

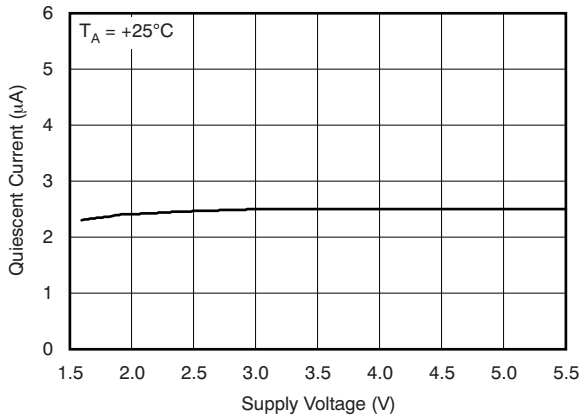


Figure 4.

POWER-SUPPLY REJECTION vs TEMPERATURE

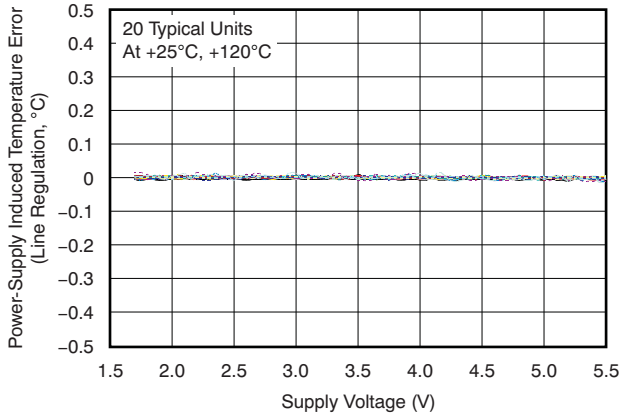


Figure 5.

POWER-SUPPLY REJECTION vs TEMPERATURE

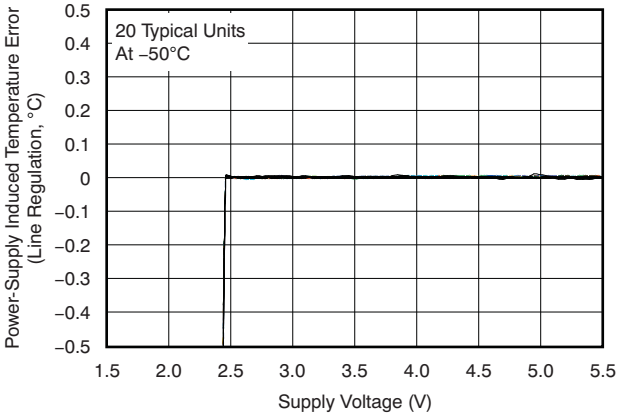


Figure 6.

TYPICAL CHARACTERISTICS (continued)

TEMPERATURE ERROR vs TEMPERATURE

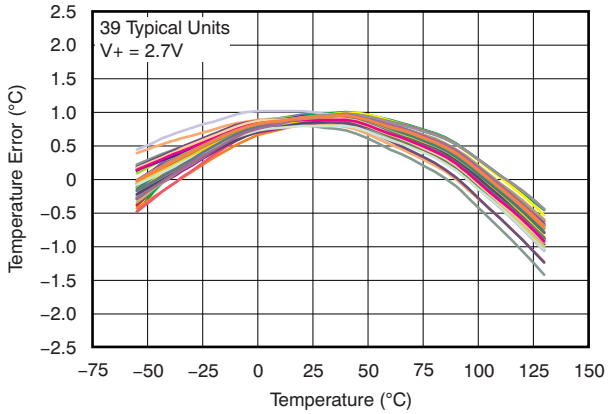


Figure 7.

MINIMUM SUPPLY VOLTAGE vs TEMPERATURE

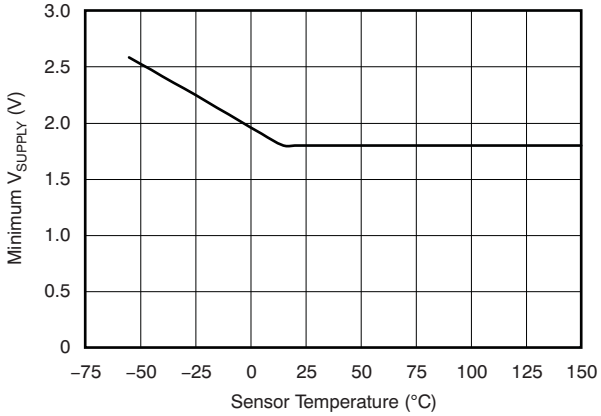


Figure 8.

WIDEBAND OUTPUT NOISE VOLTAGE

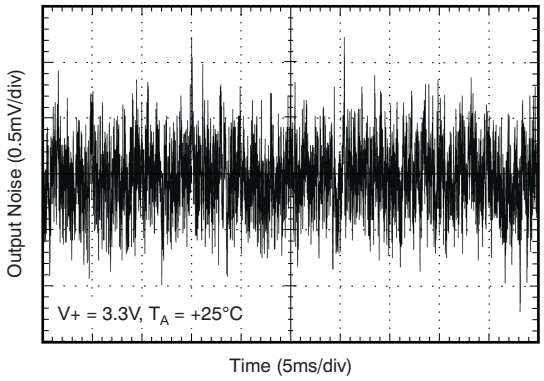


Figure 9.

THERMAL SETTLING (FLUID-FILLED TEMPERATURE BATH)

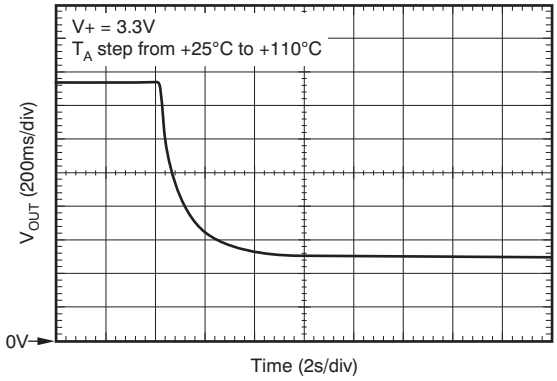


Figure 10.

APPLICATION INFORMATION

OVERVIEW

The TMP20 is a precision analog output temperature sensor. The temperature range of operation is –55°C to +130°C with supply voltages of 2.7V to 5.5V. The TMP20 can operate from power-supply voltages as low as 1.8V over a temperature range of +15°C to +130°C.

Power-supply bypassing is recommended; use a 100nF capacitor placed as closely as possible to the supply pin.

TRANSFER FUNCTION

The analog output of the TMP20 over the –55°C to +130°C temperature range corresponds to the parabolic transfer function:

$$V_{OUT} = (-3.88 \times 10^{-6} \times T^2) + (-1.15 \times 10^{-2} \times T) + 1.8639V$$

Where the temperature *T* is in °C.

When solved for temperature, the equation is:

$$T = -1481.96 + \sqrt{\frac{2.19262 \times 10^{6} + (1.8639 - V_O)}{3.88 \times 10^{-6}}}$$

These equations apply over the entire operating range, –55°C to +130°C.

A simplified linear transfer function for near +25°C measurement is:

$$V_{OUT} = -11.69mV/°C \times T + 1.8663V.$$

Linear transfer functions can be calculated for limited temperature ranges by calculating the slope and offset for that limited range, where slope is calculated by:

$$m = -7.76 \times 10^{-6} \times T - 0.0115$$

with T equal to the temperature at the middle of the temperature range of interest.

The offset in the linear transfer function is found by:

$$b = [V_{OUT}(T_{MAX}) + V_{OUT}(T) - m \times (T_{MAX} + T)]/2$$

where $V_{OUT}(T_{MAX})$ is the calculated output voltage at T_{MAX} as determined from the parabolic transfer function.

$V_{OUT}(T)$ is then the calculated output voltage at T as determined by using the parabolic transfer function.

Example 1

Determine the linear transfer function for –40°C to +110°C.

T_{MIN} = –40°C; T_{MAX} = +110°C; therefore, T = +35°C

$m = -11.77mV/°C$

V_{OUT} (110°C) = 0.5520V

V_{OUT} (35°C) = 1.4566V

b = 1.8576V

Therefore, the linear transfer function for –40°C to +110°C is:

$$V_{OUT} = -11.77mV/°C \times T + 1.8576V$$

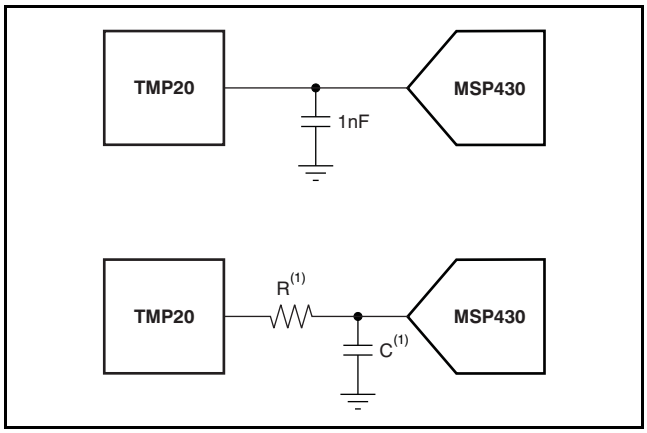
Table 1 shows many common temperature ranges of interest and the corresponding linear transfer functions for these ranges. Note that the error (maximum deviation) of the linear equation from the parabolic equation increases as the temperature ranges widen.

Table 1. Common Temperature Ranges and Corresponding Linear Transfer Functions

Temperature Range		Linear Equation (V)	Maximum Deviation of Linear Equation from Parabolic Equation (°C)
T_{MIN} (°C)	T_{MAX} (°C)		
–55	+130	$V_{OUT} = -11.79mV/°C \times T + 1.8528$	±1.41
–40	+110	$V_{OUT} = -11.77mV/°C \times T + 1.8577$	±0.93
–30	+100	$V_{OUT} = -11.77mV/°C \times T + 1.8605$	±0.70
–40	+85	$V_{OUT} = -11.67mV/°C \times T + 1.8583$	±0.65
–10	+65	$V_{OUT} = -11.71mV/°C \times T + 1.8641$	±0.23
+35	+45	$V_{OUT} = -11.81mV/°C \times T + 1.8701$	±0.004
+20	+30	$V_{OUT} = -11.69mV/°C \times T + 1.8663$	±0.004

OUTPUT DRIVE and CAPACITIVE LOADS

When used in noisy environments, adding a capacitor from the output to ground with a series resistor filters the TMP20 output; this configuration is illustrated in Figure 11. The TMP20 can directly drive up to 1nF of load capacitance while sourcing and sinking 600µA. Under this condition, capacitive loads in the range of 1nF to 10µF require a 150Ω series output resistor to achieve a stable temperature measurement. The output impedance of the TMP20 is 10Ω (typical) when sinking current and less than 1Ω when sourcing current, as shown in Figure 1.



(1) A series resistor, R, may be required depending upon the amount of capacitance, C, and the amount of source/sink current drawn from the output of the TMP20.

Figure 11. TMP20 Output Filtering

TINA-TI (FREE DOWNLOAD SOFTWARE)

Using TINA-TI SPICE-Based Analog Simulation Program with the TMP20

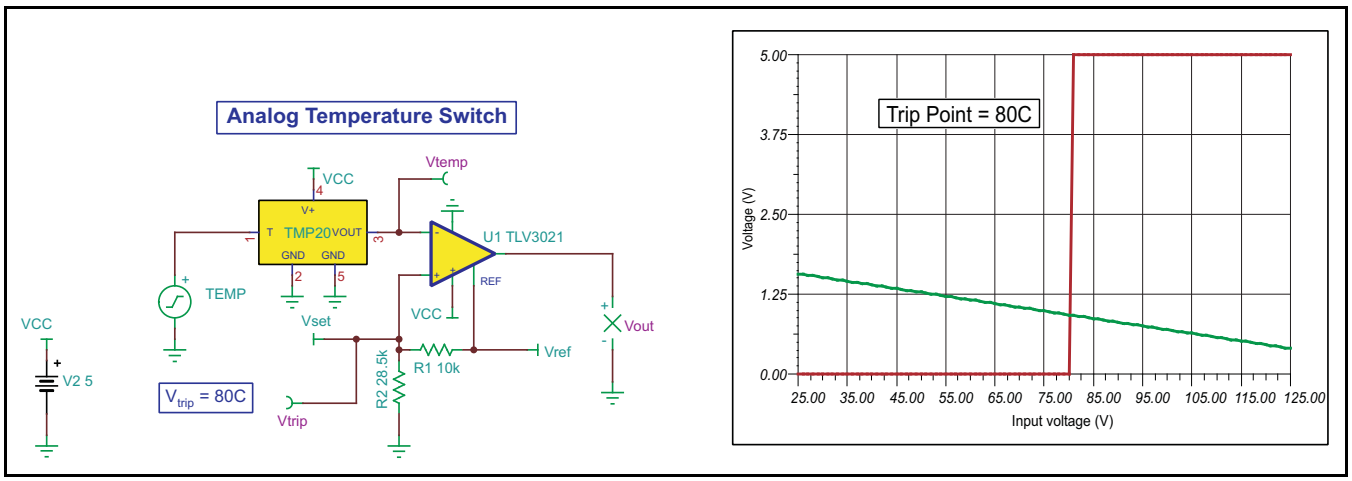
TINA is a simple, powerful, and easy-to-use circuit simulation program based on a SPICE engine. TINA-TI is a free, fully functional version of the TINA software, preloaded with a library of macromodels in addition to a range of both passive and active models. It provides all the conventional dc, transient, and frequency domain analysis of SPICE as well as additional design capabilities.

Available as a free download from the Analog eLab Design Center, TINA-TI offers extensive post-processing capability that allows users to format results in a variety of ways.

Virtual instruments offer users the ability to select input waveforms and probe circuit nodes, voltages, and waveforms, creating a dynamic quick-start tool.

Figure 12 and Figure 13 show example TINA-TI circuits for the TMP20 that can be used to develop, modify, and assess the circuit design for specific applications. Links to download these simulation files are given below.

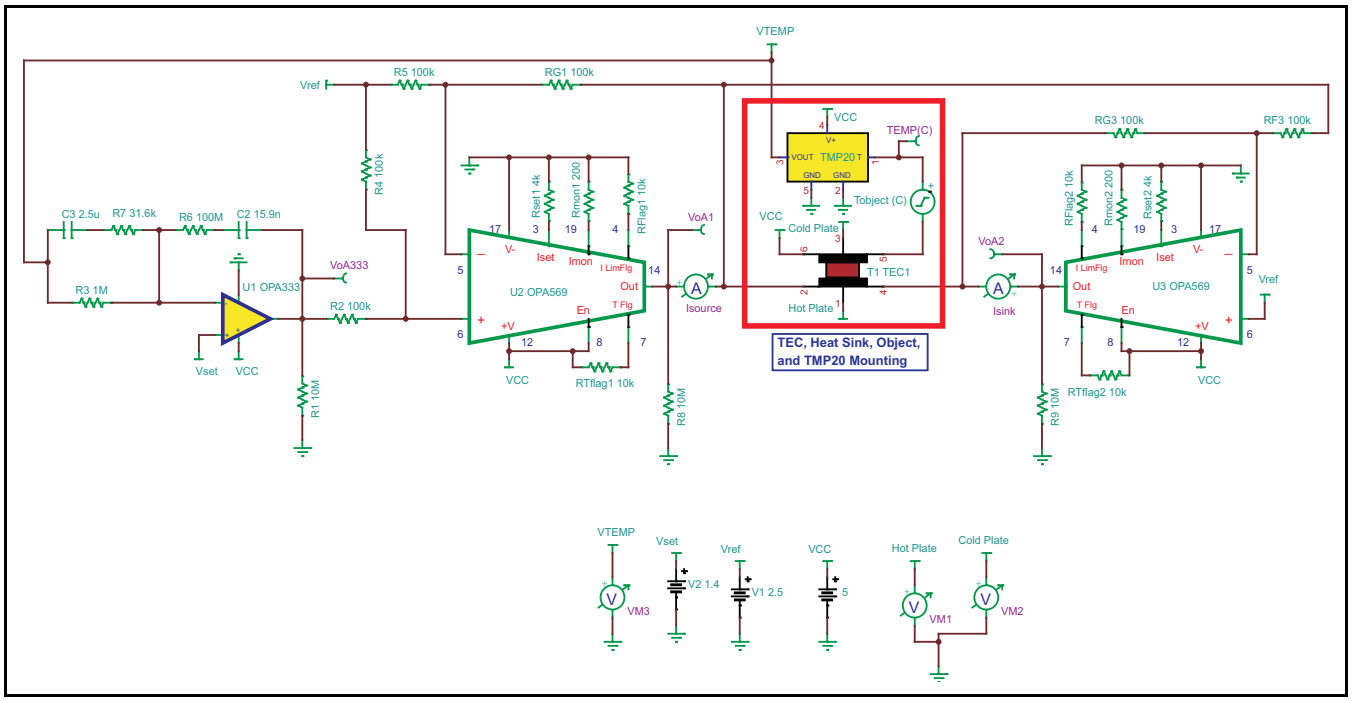
NOTE: These files require that either the TINA software (from DesignSoft) or TINA-TI software be installed. Download the free TINA-TI software from the TINA-TI folder.



Note: The TMP20 TINA model is preliminary only.

Figure 12. Analog Temperature Switch

To download a compressed file that contains the TINA-TI simulation file for this circuit, click the following link: Analog Temperature Switch.



(1) The TMP20 TINA model is preliminary only.

(2) Parameters and definitions:

a. T_{object} = Temperature of object to be cooled (in °C)

b. V_{set} = Voltage that corresponds to desired output temperature from TMP20

c. V_{temp} = Voltage output of TMP20

d. Hotplate = TEC plate on opposite side of object

e. Coldplate = TEC plate in contact with object

(3) In this configuration, the TEC driver is capable of cooling to –7°C and heating to +41°C; the V_{set} range is 1.38V to 1.95V. The OPA569 device outputs = ±1.65A, ±0.5V to ±4.5V. The 10MΩ resistors are for TINA convergence.

(4) For convergence in TINA software: In **Analysis/Set Analysis Parameters** menu, set *shunt conductance* = 1p.

Figure 13. Thermoelectric Cooler

To download a compressed file that contains the TINA-TI simulation file for this circuit, click the following link: Thermoelectric Cooler.

LAYOUT INFORMATION

The substrate on the TMP20AIDCK package is directly connected via conductive epoxy to the flag which connects pin 2 (GND) on the lead frame. Consequently, pin 2 (GND) is the best lead for a conductive thermal connection to the TMP20 die. In addition, the optimal electrical connection for this pin is ground (GND).

Do NOT attempt to connect pin 2 to any electrical potential other than ground.

If it is not possible to connect pin 2 to ground, it is also possible to electrically isolate this pin (that is, leave it floating); however, be very cautious in doing this because any noise or electromagnetic interference or radio frequency interference (EMI/RFI) spikes that couple in through this pin can cause erroneous temperature results.

Figure 14 shows a proper layout of the TMP20 with correct electrical and thermal connections of pin 2.

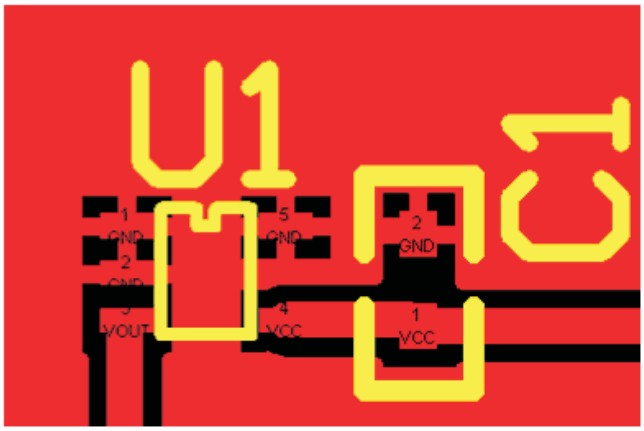


Figure 14. TMP20 Layout with Proper Electrical and Thermal Connections for Pin 2

Figure 15 illustrates a layout of the TMP20 with proper electrical connections and poor thermal connections to ground.

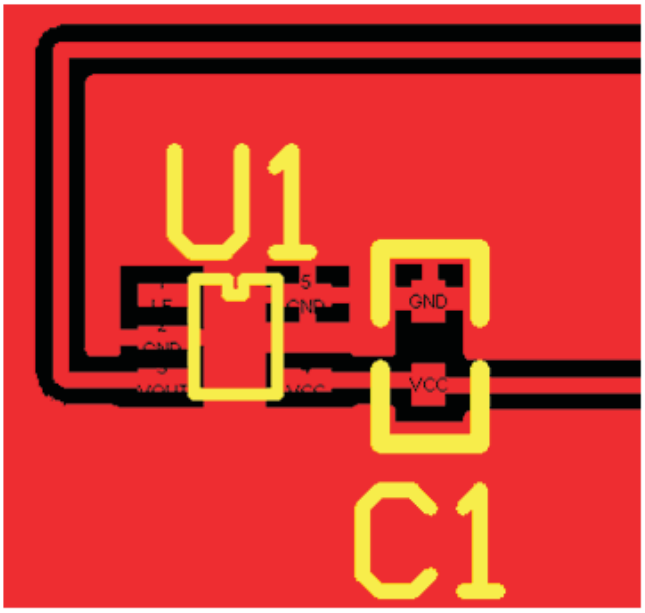


Figure 15. TMP20 Layout with Proper Electrical and Poor Thermal Connections to Ground

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TMP20AIDCKR	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU | CU NIPDAUAG	Level-1-260C-UNLIM		ODB	Samples
TMP20AIDCKT	ACTIVE	SC70	DCK	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU | CU NIPDAUAG	Level-1-260C-UNLIM		ODB	Samples
TMP20AIDRLR	ACTIVE	SOT	DRL	6	4000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		ODA	Samples
TMP20AIDRLT	ACTIVE	SOT	DRL	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		ODA	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

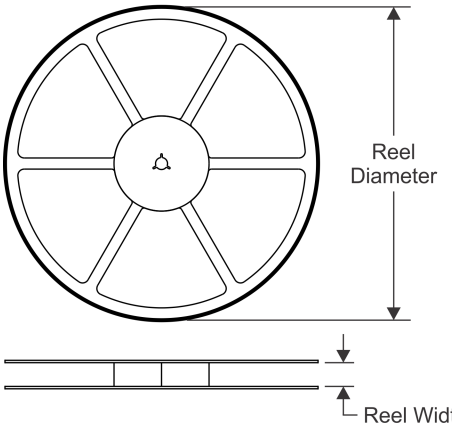
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

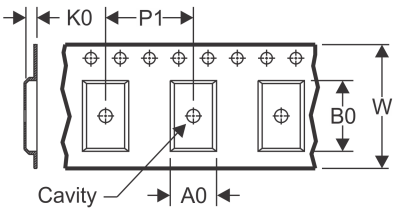
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

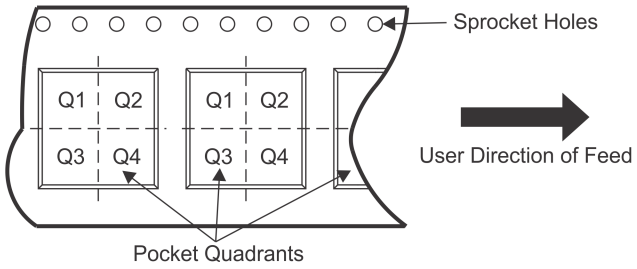


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

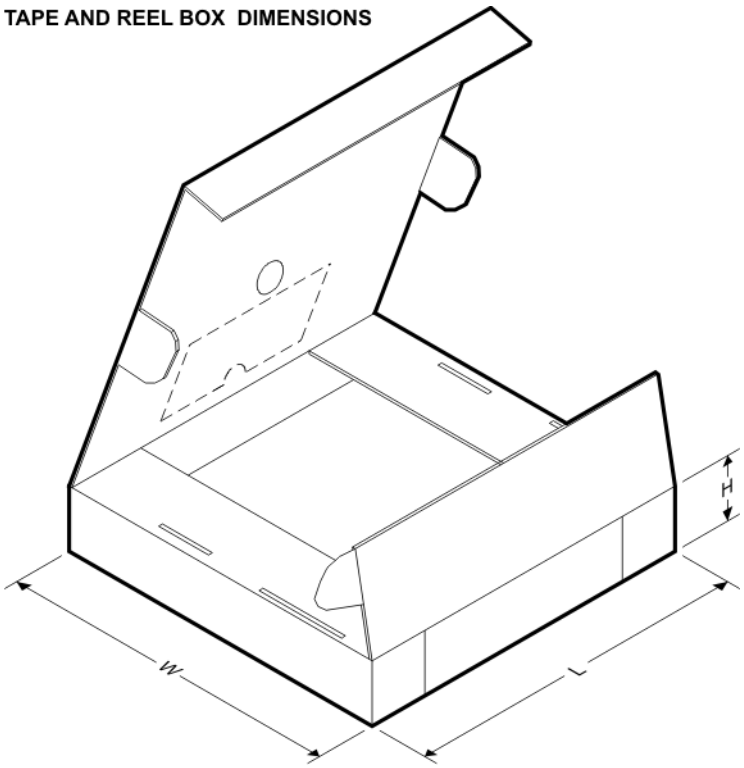
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TMP20AIDCKR	SC70	DCK	5	3000	180.0	8.4	2.47	2.3	1.25	4.0	8.0	Q3
TMP20AIDCKR	SC70	DCK	5	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
TMP20AIDCKT	SC70	DCK	5	250	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
TMP20AIDCKT	SC70	DCK	5	250	180.0	8.4	2.47	2.3	1.25	4.0	8.0	Q3
TMP20AIDRLR	SOT	DRL	6	4000	180.0	9.5	1.78	1.78	0.69	4.0	8.0	Q3
TMP20AIDRLR	SOT	DRL	6	4000	180.0	8.4	1.98	1.78	0.69	4.0	8.0	Q3
TMP20AIDRLT	SOT	DRL	6	250	180.0	8.4	1.98	1.78	0.69	4.0	8.0	Q3

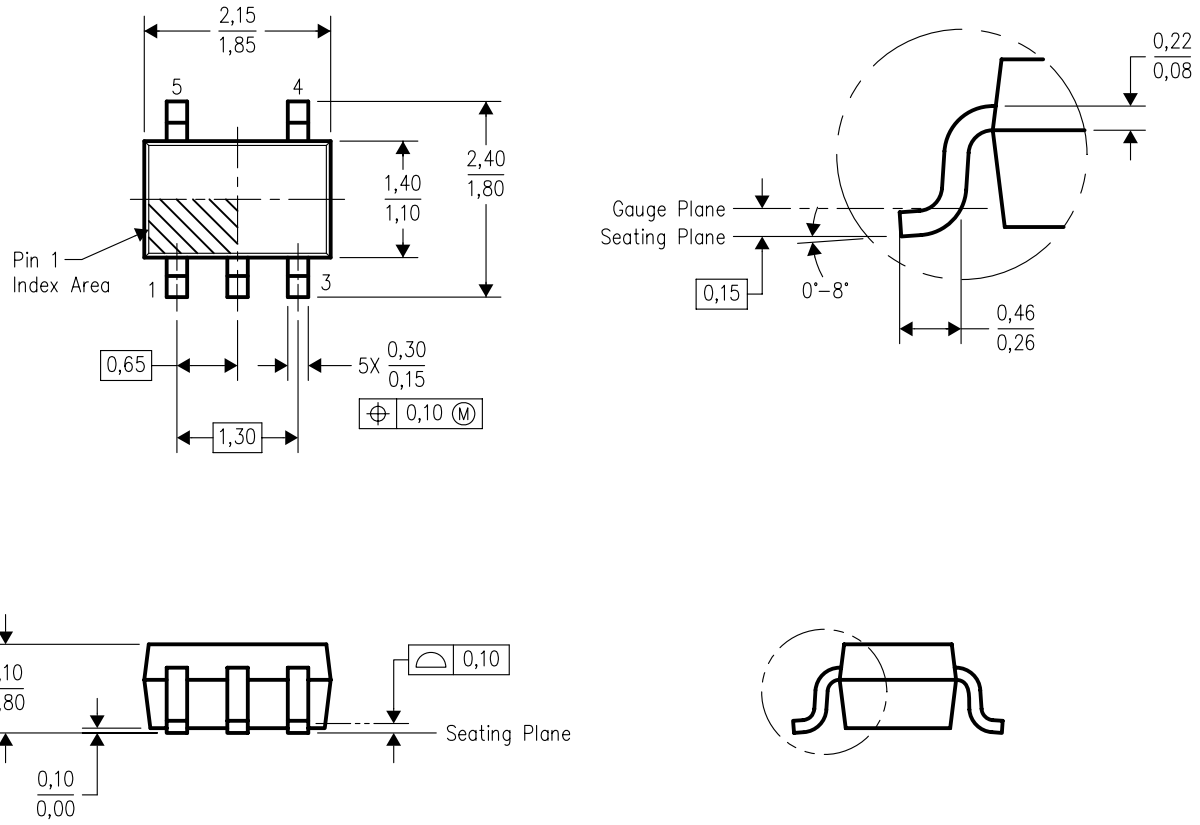
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TMP20AIDCKR	SC70	DCK	5	3000	202.0	201.0	28.0
TMP20AIDCKR	SC70	DCK	5	3000	180.0	180.0	18.0
TMP20AIDCKT	SC70	DCK	5	250	180.0	180.0	18.0
TMP20AIDCKT	SC70	DCK	5	250	202.0	201.0	28.0
TMP20AIDRLR	SOT	DRL	6	4000	184.0	184.0	19.0
TMP20AIDRLR	SOT	DRL	6	4000	202.0	201.0	28.0
TMP20AIDRLT	SOT	DRL	6	250	202.0	201.0	28.0

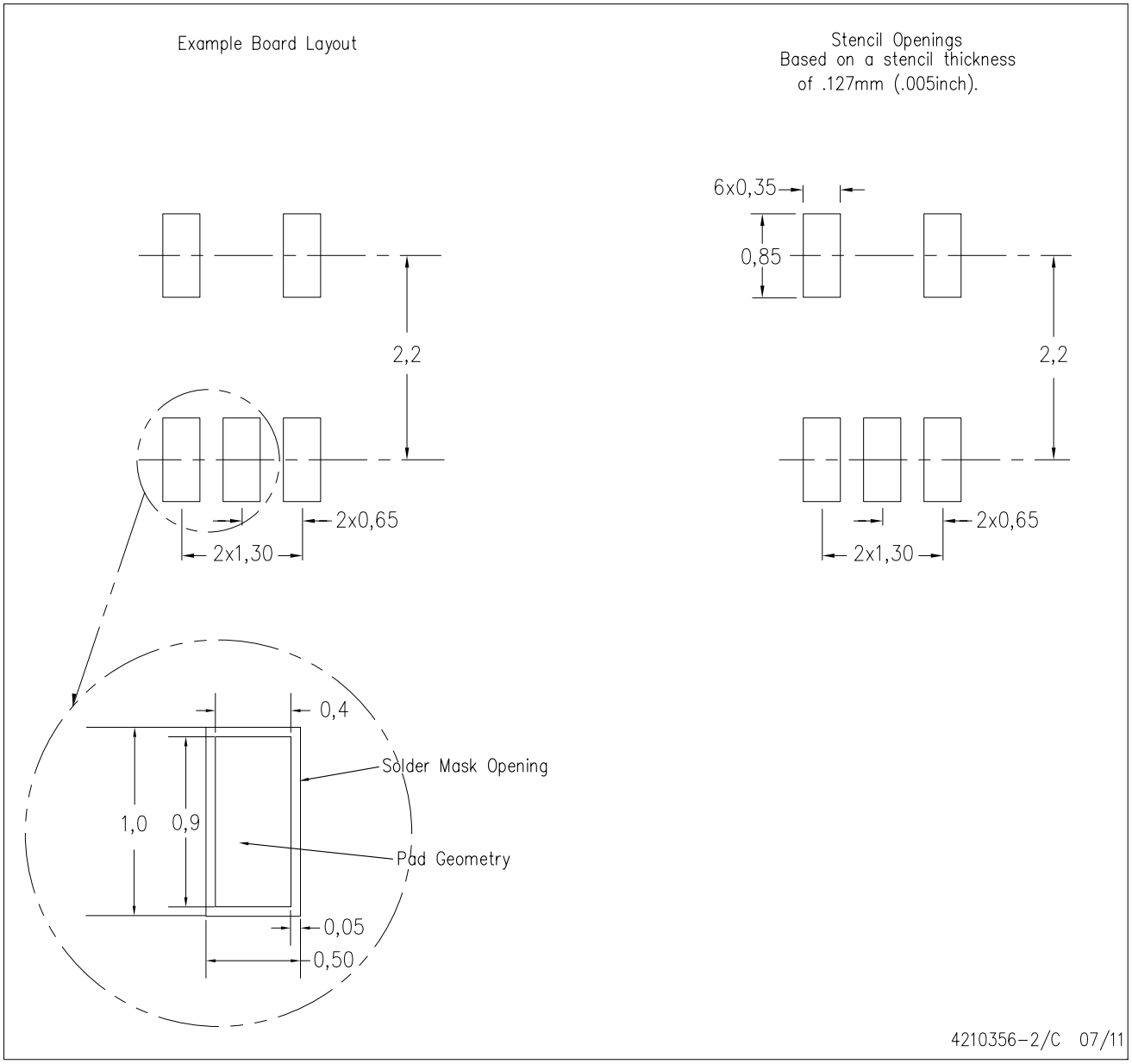
DCK (R–PDSO–G5) PLASTIC SMALL–OUTLINE PACKAGE



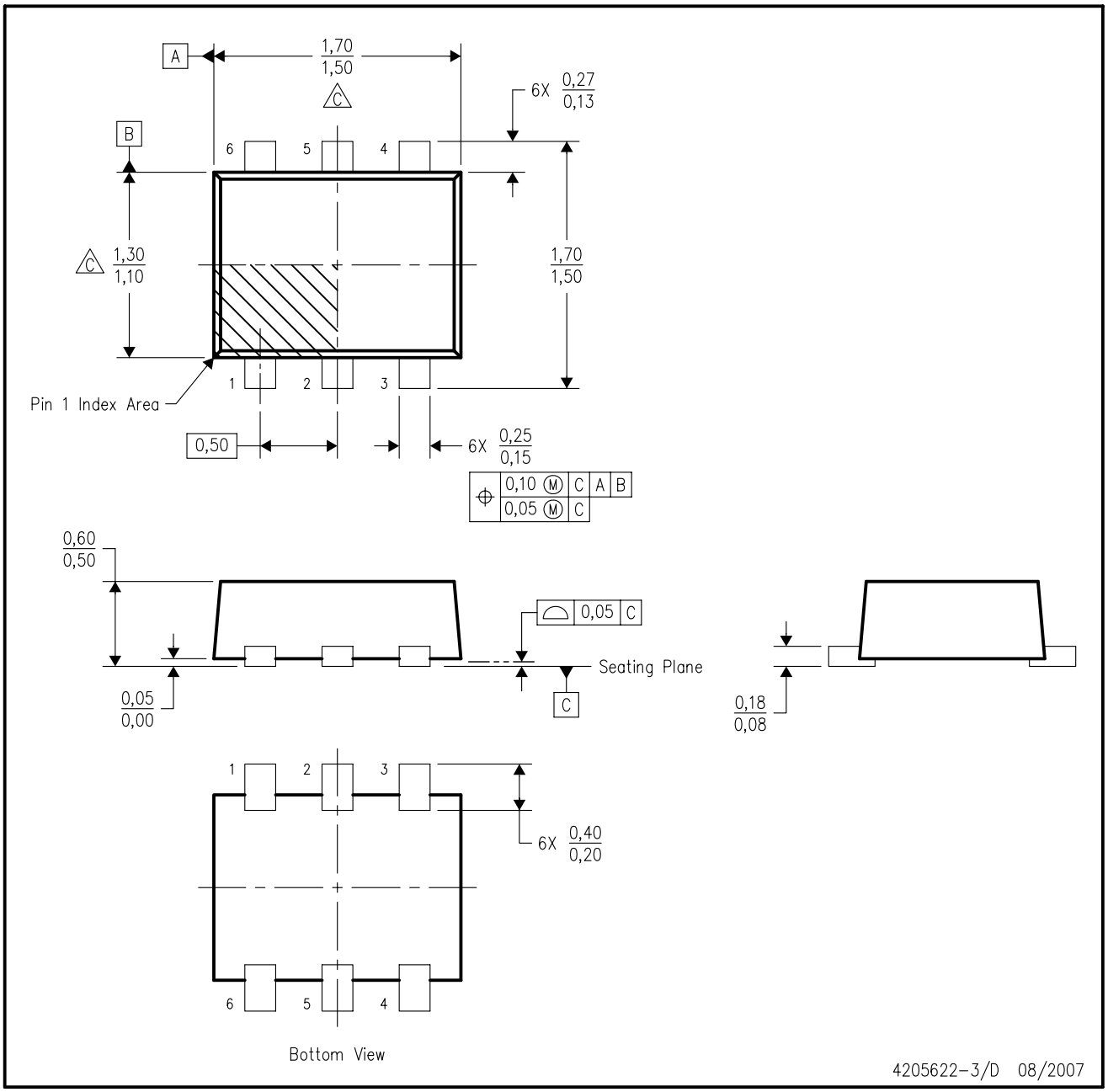
4093553–3/G 01/2007

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO–203 variation AA.

DCK (R–PDSO–G5) PLASTIC SMALL OUTLINE

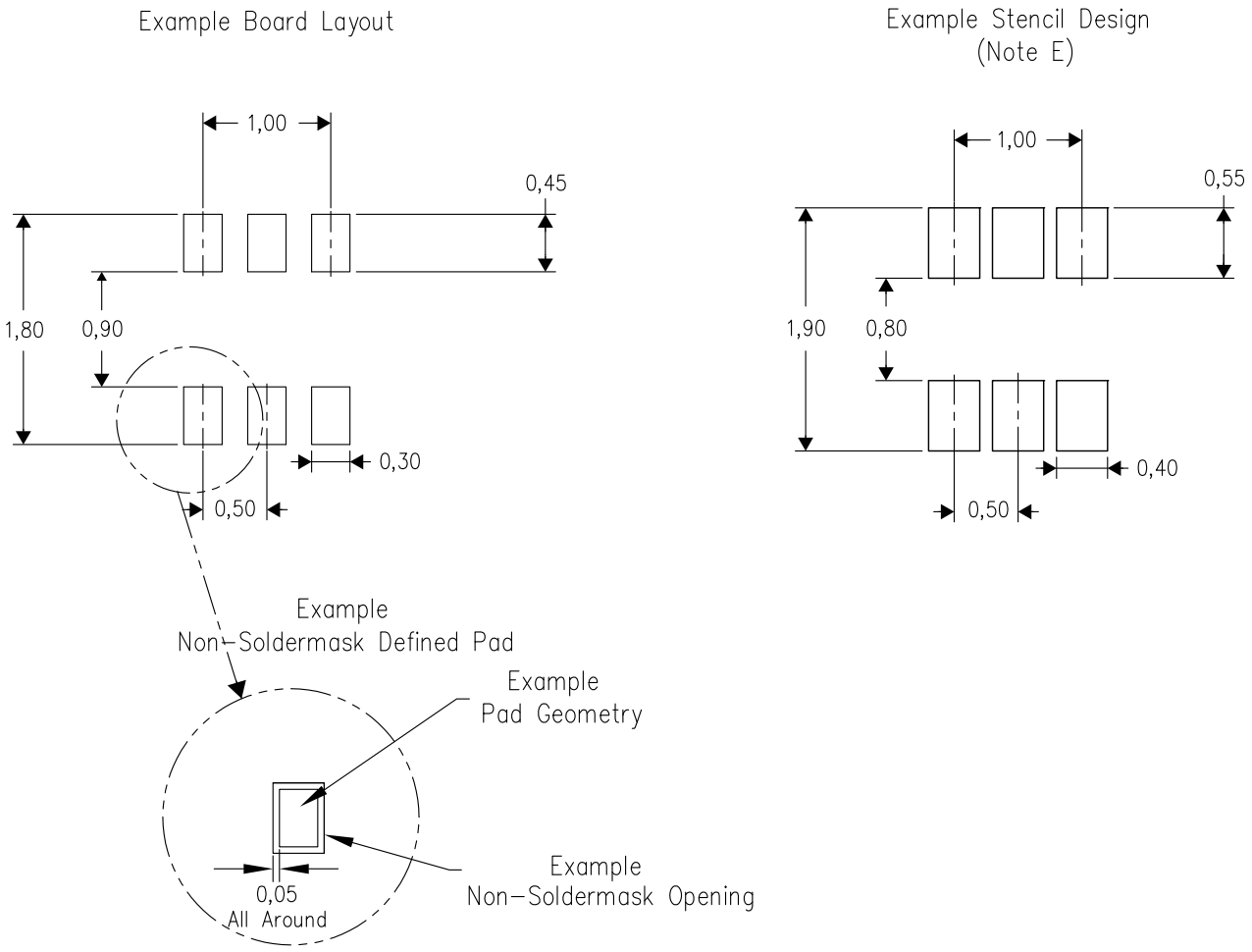


NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash, interlead flash, protrusions, or gate burrs. Mold flash, interlead flash, protrusions, or gate burrs shall not exceed 0,15 per end or side.
D. JEDEC package registration is pending.

DRL (R–PDSO–N6) PLASTIC SMALL OUTLINE



4208207–3/E 06/12

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
E. Maximum stencil thickness 0,127 mm (5 mils). All linear dimensions are in millimeters.
F. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
G. Side aperture dimensions over–print land for acceptable area ratio > 0.66. Customer may reduce side aperture dimensions if stencil manufacturing process allows for sufficient release at smaller opening.

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