UM10751

OM13488 8-bit GPIO Daughter Card User Manual

Rev. 1.0 — 11 October 2013 **User manual**

Document information

Info	Content
Keywords	Fm+ Development Kit, OM13320, GPIO, OM13303
Abstract	Installation guide and User Manual for the OM13488 8-bit GPIO Daughter Card that connects to OM13320 Fm+ Development Kit. This board permits easy and simple evaluation of most of NXP's 8-bit I^2C GPIO portfolio of products.

Revision history

Rev	Date	Description
1.0	20131011	Initial Release

Contact information

For more information, please visit: http://www.nxp.com

For sales office addresses, please send an email to: salesaddresses@nxp.com

1. Introduction

The OM13488 8-bit I²C GPIO Daughter Card connects to the OM13320 Fm+ Development kit and permits easy evaluation of most of NXP's 8-bit I²C GPIO portfolio of products.

Table_1 lists the supported devices.

The OM13488 8-bit I²C GPIO Daughter Card is shipped with no GPIO device soldered to the board. The user must purchase the device he is interested in evaluating in a TSSOP16 package (the ordering part number suffix should be "PW" and the package designation should be SOT403-1). These leaded packages should be relatively easy to solder to the board with a low wattage, fine tipped soldering iron.

Table 1. Devices Supported by OM13488 8-bit I²C GPIO Daughter Card

Device	Description	Orderable Part Number
PCA6408A	Low-voltage, 8-bit I²C-bus and SMBus I/O expander with interrupt output, reset, and configuration registers	PCA6408APW
PCA8574A	Remote 8-bit I/O expander for I²C-bus with interrupt	PCA8574APW
PCA8574	Remote 8-bit I/O expander for I²C-bus with interrupt	PCA8574PW
PCA9534	8-bit I²C-bus and SMBus low power I/O port with interrupt	PCA9534PW
PCA9538A	Low-voltage 8-bit I²C-bus I/O port with interrupt and reset	PCA9538APW
PCA9538	8-bit I²C-bus and SMBus low power I/O port with interrupt and reset	PCA9538PW
PCA9554A	8-bit I²C-bus and SMBus I/O port with interrupt	PCA9554APW
PCA9554B	Low-voltage 8-bit I²C-bus and SMBus low power I/O port with interrupt, weak pull-up	PCA9554BPW
PCA9554C	Low-voltage 8-bit I²C-bus and SMBus low power I/O port with interrupt, weak pull-up	PCA9554CPW
PCA9554	8-bit I²C-bus and SMBus I/O port with interrupt	PCA9554PW
PCA9670	Remote 8-bit I/O expander for Fm+ I²C-bus with reset	PCA9670PW
PCA9672	Remote 8-bit I/O expander for Fm+ I²C-bus with interrupt and reset	PCA9672PW
PCA9674A	Remote 8-bit I/O expander for Fm+ I²C-bus with interrupt	PCA9674APW
PCA9674	Remote 8-bit I/O expander for Fm+ I²C-bus with interrupt	PCA9674PW
PCAL6408A	Low-voltage translating, 8-bit I²C-bus/SMBus I/O expander with interrupt output, reset,	PCAL6408APW

Device	Description	Orderable Part Number
	and configuration registers	
PCAL9538A	Low-voltage 8-bit I²C-bus and SMBus low power I/O port with interrupt, reset and Agile I/O	PCAL9538APW
PCAL9554B	Low-voltage 8-bit I²C-bus/SMBus low power I/O port with interrupt, weak pull-up and Agile I/O	PCAL9554BPW
PCAL9554C	Low-voltage 8-bit I²C-bus/SMBus low power I/O port with interrupt, weak pull-up and Agile I/O	PCAL9554CPW
PCF8574	Remote 8-bit I/O expander for I^2C-bus with interrupt	PCF8574PW
PCF8574A	Remote 8-bit I/O expander for I^2C-bus with interrupt	PCF8574APW

The pin configuration of these devices varies only a bit and the different pin selections are made via jumpers.

2. Features of the OM13488 8-bit GPIO Daughter Card

- Direct connection to OM13320 Fm+ Development kit
- Footprint for a TSSOP16 package, user solderable
- Jumper configuration accommodates most NXP 8-bit GPIO
- Flexible power supply configuration: 3.3V, 5V or external supply
- Direct connection to OM13303 GPIO Target board for I/O visualization
- Jumper configuration of device I^2C address
- LED indicators for power and $\overline{INT}$
- Scope ground connection loop

3. Pin Configuration of 8-bit GPIO Devices

The different 8-bit GPIO devices pin configurations differ only slightly between devices. See Fig 1 for a description of the different pinouts.

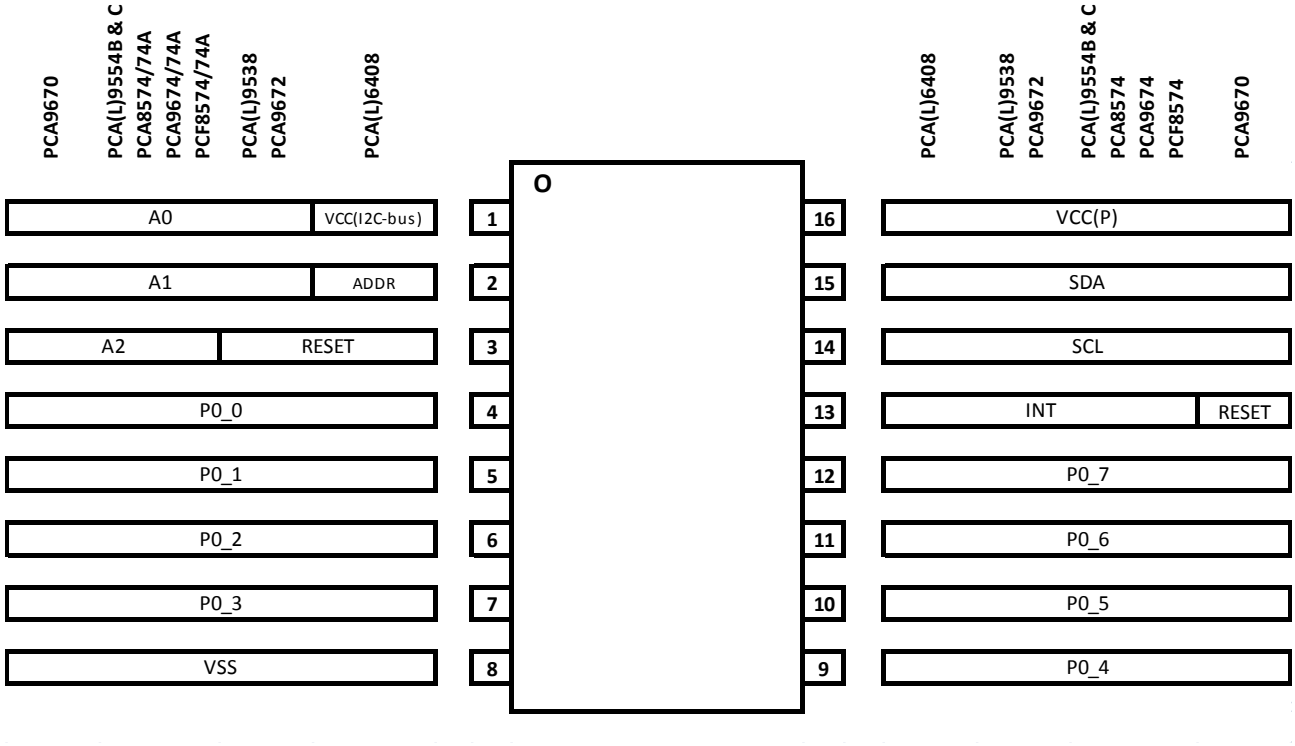


Fig 1. Pin Configuration 8-bit GPIO Devices

3.1 Power Supply Setup

Power supply voltages may be selected from the tester connector CN4 or the Fm+ board CN2. If one selects Fm+ CN2, either 3.3V or 5V can be chosen. Additionally, the PCA(L)6408 device implements two power supplies which are separately chosen, i.e. one can be 3.3V and the other 5V for voltage level translation evaluation. Both of these power supplies can be supplied externally by using TP1 and TP2 near the tester connector CN4. See the schematic section at the end of this document for more details.

The jumpers for power supply selection are JP2, JP3, and JP4

3.2 Reset, Interrupt, and Address pins selection

The Reset, Interrupt and Address pins are used in combinations on various devices. The selection matrix on the 8-bit GPIO board sends pins 2, 3, and 13 to determine if the pins are address or function on JP9, JP10, and JP11. Then, if they are determined address pins, JP1, JP7 and JP8 tie them to logic high or low. If they are determined to be function pins, the other position of JP9, JP10 and JP11 tie them to the correct connector function pins. See the schematic section at the end of this document for more details.

The logic high level for the address pins is VDDP.

4. Board Jumper Set Up

4.1 Power Supply Jumpers

The power supply selections for the OM13488 is very flexible and allows for detailed analysis and evaluation of all the NXP 8-bit GPIO devices. JP3 labeled PWR selects between 5V supplied from the tester connector CN4 (jumper between pin 2 and 3 labeled TSTR) and the Fm+ board connector CN2 (jumper between pin 1 and 2). If 3.3V or external power operation is desired, no jumper is required.

JP2 selects between 5V and 3.3V for a second power supply needed for PCA(L)6408A. If the device under test is not PCA(L)6408A, leave this jumper open.

JP4 selects between 5V and 3.3V for the main power supply on pin 16 of the device under test. Add a jumper between pins 2 & 3 for 3.3V or 1 & 2 for 5V.

For external power supply operation, do not jumper JP2, JP3 and JP4 and connect a voltage source to TP2 for the main power supply connected to pin 16 of the device under test. Connect another external voltage source to TP1 if the device under test is PCA(L)6408A.

See the schematic section at the end of this document for more details.

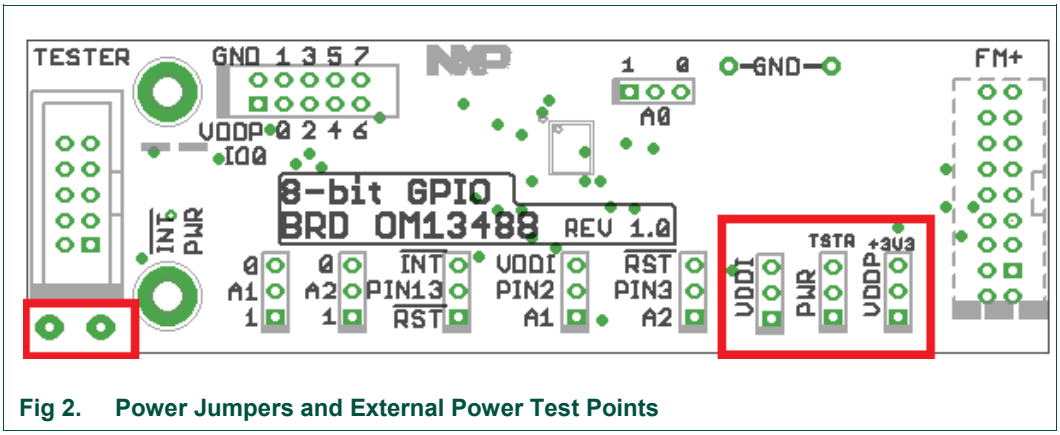


Fig 2. Power Jumpers and External Power Test Points

4.2 PCA8574, PCA8574A, PCA9534, PCA9554A, PCA9554B, PCA9554C, PCA9554, PCA9674A, PCA9674, PCAL9554B, PCAL9554C, PCF8574, PCF8574A

The PCA8557/A, PCA9534, PCA(L)5554x, PCA9674/A implement three address pins and $\overline{\text{INT}}$. This configuration ignores the power supply setup, but normally, only JP4 with a jumper between pins 2 & 3 need be applied to power the device at 3.3V.

To configure the function pins, apply jumpers between pins 1 & 2 on JP10 and JP11 to configure device pin 2 and pin 3 as addresses. Apply a jumper between pins 2 & 3 on JP9 to configure device pin 13 as $\overline{\text{INT}}$.

Then, apply jumpers to JP1, JP7 and JP8 to configure the desired I^2C address. Logic high or logic low is labeled on the board.

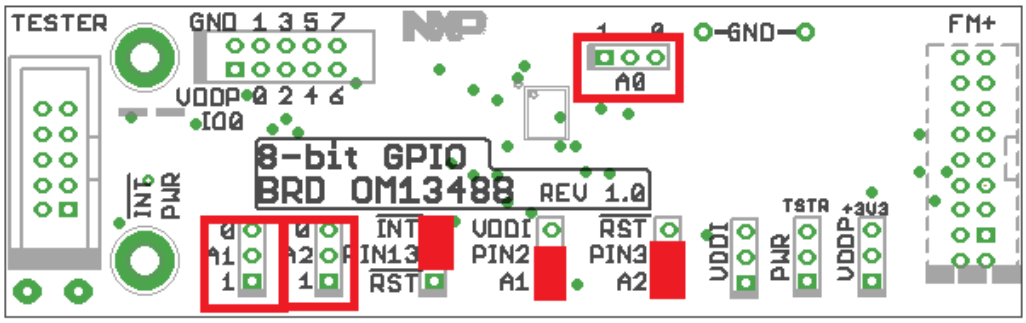


Fig 3. Jumper configuration for PCA8574, PCA8574A, PCA9534, PCA9554A, PCA9554B, PCA9554C, PCA9554, PCA9674A, PCA9674, PCAL9554B, PCAL9554C, PCF8574, PCF8574A

4.3 PCA9670

The PCA9670 implements three address pins and $\overline{\text{RST}}$. This configuration ignores the power supply setup, but normally, only JP4 with a jumper between pins 2 & 3 need be applied to power the device at 3.3V.

To configure the function pins, apply jumpers between pins 1 & 2 on JP9, JP10 and JP11 to configure pin 2 and pin 3 as addresses and pin 13 as $\overline{\text{RST}}$.

Then, apply jumpers to JP1, JP7 and JP8 to configure the desired I^2C address. Logic high or logic low is labeled on the board.

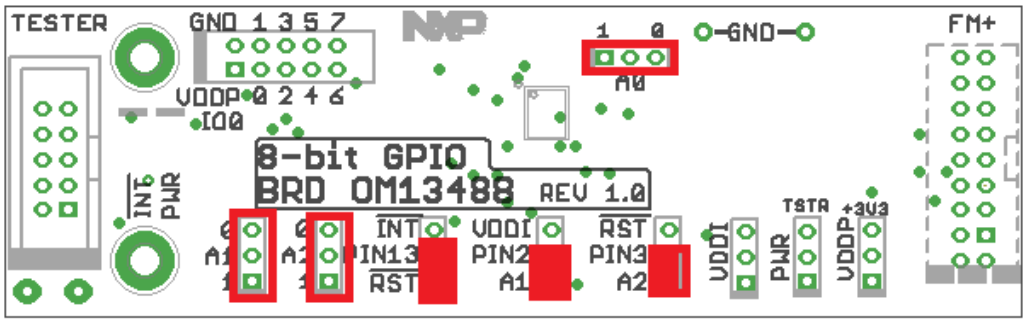


Fig 4. Jumper Configuration for PCA9670

4.4 PCA9672, PCAL9538A, PCA9538A, PCA9538

The PCA9672 and PCA9538 series implement two address pins, $\overline{\text{RST}}$ and $\overline{\text{INT}}$. This configuration ignores the power supply setup, but normally, only JP4 with a jumper between pins 2 & 3 need be applied to power the device at 3.3V.

To configure the function pins, apply jumpers between pins 2 & 3 on JP9 and JP11 to configure device pin 3 as $\overline{RST}$ and pin 13 as $\overline{INT}$. Apply a jumper between pins 1 & 2 on JP10 to configure device pin 2 as an address.

Then, apply jumpers to JP1 and JP7 to configure the desired I^2C address. Logic high or logic low are labeled on the board. Leave JP8 open.

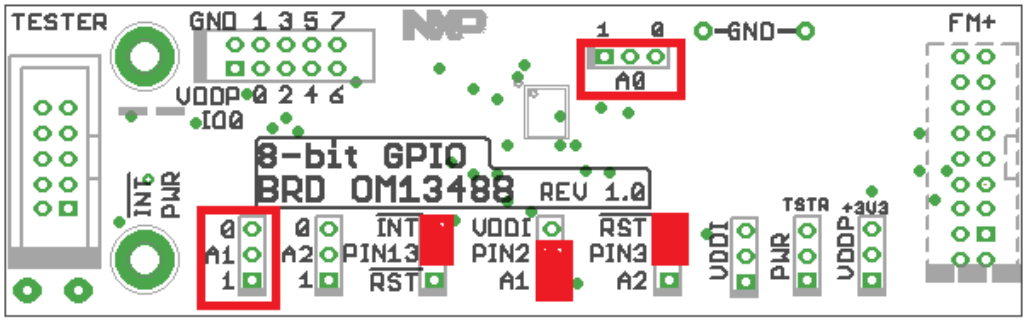


Fig 5. Jumper Configuration for PCA9672, PCAL9538A, PCA9538A, PCA9538

4.5 PCAL6408A, PCA6408A

The PCA(L)6408A devices are level translating, Agile I/0 Expanders with two power supplies, one address pin, $\overline{RST}$ and $\overline{INT}$. The two power supplies may operate at different voltages to translate from the I^2C-bus voltage domain to a higher or lower I/O voltage. JP2 and JP4 may be set to the same or different voltages, or left open and external voltage sources connected to TP1 and TP2. Unfortunately, there is a slight labeling issue on this board. Device pin 1 is the VDDI power supply and is permanently connected to JP2 which selects between VDDP and ground. Use a wire to jumper between pin 2 of JP1 to pin 3 of JP10 which is the board VDDI. See the datasheet for more details on voltage level translation.

Note that the 10K pull up resistors SDA and SCL, R5 and R6, are connected to VDDP which may cause incorrect current readings if two different supplies are used.

To configure the function pins, apply jumpers between pins 2 & 3 on JP9 and JP11 to configure device pin 3 as $\overline{RST}$ and device pin 13 as $\overline{INT}$.

There is a slight labeling issue on this board. Device pin 2 is the only address pin and JP10 should jumper pins 1 and 2 to route the address to JP7 (A1 instead of A0).Then, apply a jumper to JP7 to configure the desired I^2C address. Logic high or logic low are labeled on the board. Leave JP8 open.

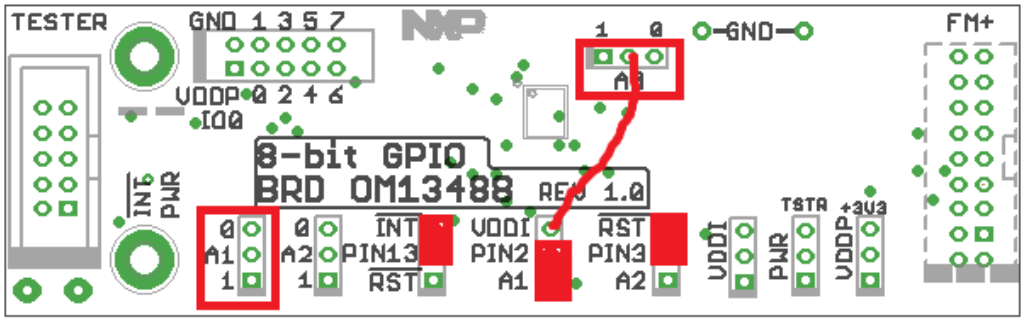


Fig 6. Jumper Configuration for PCA(L)6408

5. Connector Pinouts

5.1 CN1 GPIO Target Board Connector

The OM13303 GPIO Target Board consists of eight LEDs and eight switches and connects directly to the 8-bit GPIO board through CN1. The switches and LEDs permit easy exercise of the I/O functionality of the device under test. The LEDs light red when the voltage on that channel is below VCC x 0.3V and lights green when the voltage is above VCC x 0.7V. The LEDs remain off when the voltage is between those two levels.

Table 2. CN1 GPIO Target Board Connector Pinout

CN1 Pin Number	Function	Board Connection
1	VDD	VDDP
2	Ground	GND
3	IO0	U1 pin 4
4	IO1	U1 pin 5
5	IO2	U1 pin 6
6	IO3	U1 pin 7
7	IO4	U1 pin 9
8	IO5	U1 pin 10
9	IO6	U1 pin 11
10	IO7	U1 pin 12

5.2 CN2 Fm+ Development Board Connector

The OM13488 can connect directly to the OM13320 Fm+ Development kit via CN2. This connector provides power, I^2C signals and other ancillary signals.

Note: The connector on the Fm+ board is a male, shrouded 14 pin type, while the connector on the GPIO board is female, 18 pin.. The reason lies with the shroud around the 14 pin connector. To ensure correct mating of the female with the male, two pin positions on both of the female sides are unused.

Table 3. CN2 Fm+ Board Connector

CN2 Pin Number	Function	Board Connection
1	—	No connect
2	—	No connect
3	SCL	SCL Bus 1 to U1 pin 14
4	SDA2	SDA Bus 2 not used
5	INT	Interrupt to INT LED and JP9 pin 3
6	RESET	JP9 pin 1, JP11 pin 3
7	+5V	JP3 pin 1
8	+3.3V	JP2 pin 3 and JP4 pin 3
9	GND	
10	GND	
11	+3.3V	JP2 pin 3 and JP4 pin 3
12	+5V	JP3 pin 1
13	RESET	JP9 pin 1, JP11 pin 3
14	INT	Interrupt to INT LED and JP9 pin 3
15	SDA	SDA Bus 1 to U1 pin 15
16	SCL2	SCL Bus 2 not used
17	—	No connect
18	—	No connect

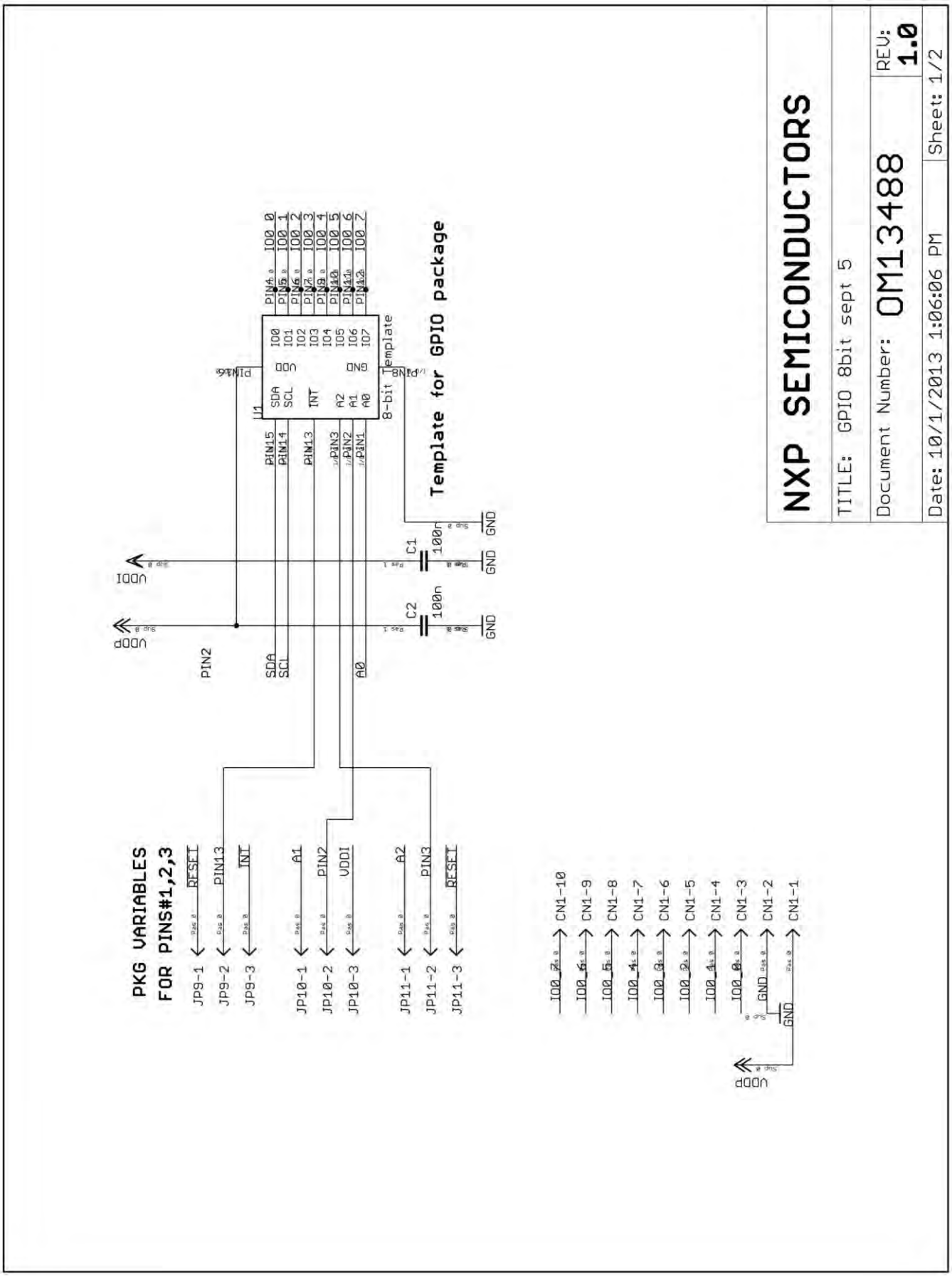
5.3 CN4 Tester Connector

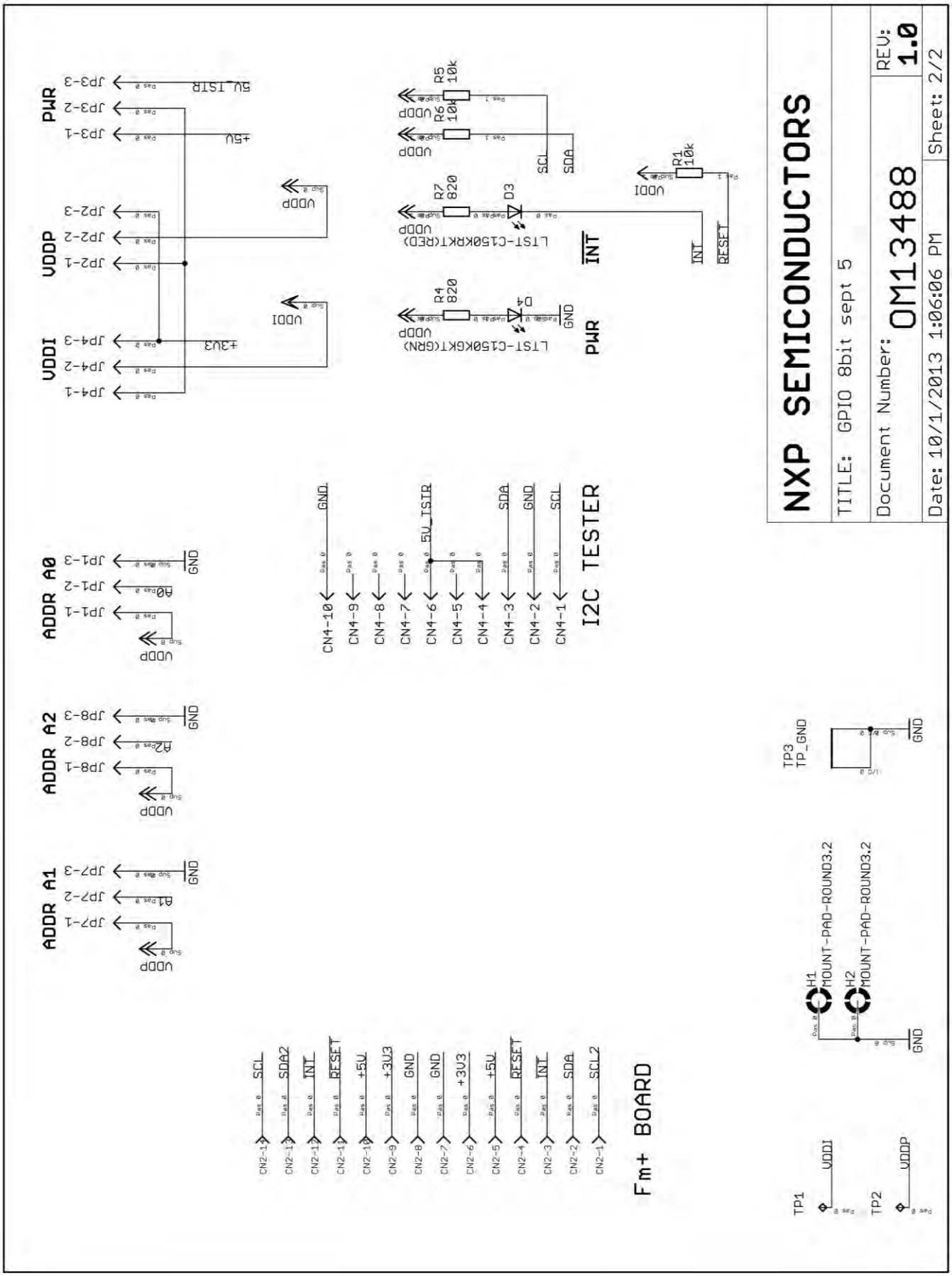
Generation, inspection and logging of I^2C-Bus data is easily achieved with third party development tools from Total Phase (www.totalphase.com) There are two tools called Aardvark and Beagle that direct connect to this board through CN4.

Note: Since SDA and SCL are both connected to the device under test, the Aardvark and the Fm+ Development board cannot be used simultaneously. The Beagle, a bus sniffer, does not have any issues.

Table 4. CN4 Tester Connector

CN4 Pin Number	Function	Board Connection
1	SCL	U1 pin 14
2	Ground	
3	SDA	U1 pin 15
4	+5V	JP3 pin 3
5	+5V	JP3 pin 3
6	+5V	JP3 pin 3
7	—	
8	—	
9	—	
10	Ground	





6. Legal information

6.1 Definitions

Draft — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

6.2 Disclaimers

Limited warranty and liability — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information.

In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the Terms and conditions of commercial sale of NXP Semiconductors.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors accepts no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

Evaluation products — This product is provided on an "as is" and "with all faults" basis for evaluation purposes only. NXP Semiconductors, its affiliates and their suppliers expressly disclaim all warranties, whether express, implied or statutory, including but not limited to the implied warranties of non-infringement, merchantability and fitness for a particular purpose. The entire risk as to the quality, or arising out of the use or performance, of this product remains with customer.

In no event shall NXP Semiconductors, its affiliates or their suppliers be liable to customer for any special, indirect, consequential, punitive or incidental damages (including without limitation damages for loss of business, business interruption, loss of use, loss of data or information, and the like) arising out the use of or inability to use the product, whether or not based on tort (including negligence), strict liability, breach of contract, breach of warranty or any other theory, even if advised of the possibility of such damages.

Notwithstanding any damages that customer might incur for any reason whatsoever (including without limitation, all damages referenced above and all direct or general damages), the entire liability of NXP Semiconductors, its affiliates and their suppliers and customer's exclusive remedy for all of the foregoing shall be limited to actual damages incurred by customer based on reasonable reliance up to the greater of the amount actually paid by customer for the product or five dollars (US$5.00). The foregoing limitations, exclusions and disclaimers shall apply to the maximum extent permitted by applicable law, even if any remedy fails of its essential purpose.

7. List of figures

8. List of tables

9. Contents

For more information, please visit: http://www.nxp.com
For sales office addresses, please send an email to: salesaddresses@nxp.com

Date of release: 11 October 2013
Document identifier: UM10751

Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

NXP:

OM13488UL

Общество с ограниченной ответственностью «МосЧип» ИНН 7719860671 / КПП 771901001
Адрес: 105318, г.Москва, ул.Щербаковская д.3, офис 1107

Данный компонент на территории Российской Федерации

Вы можете приобрести в компании MosChip.

Для оперативного оформления запроса Вам необходимо перейти по данной ссылке:

http://moschip.ru/get-element

Вы можете разместить у нас заказ для любого Вашего проекта, будь то серийное производство или разработка единичного прибора.

В нашем ассортименте представлены ведущие мировые производители активных и пассивных электронных компонентов.

Нашей специализацией является поставка электронной компонентной базы двойного назначения, продукции таких производителей как XILINX, Intel (ex.ALTERA), Vicor, Microchip, Texas Instruments, Analog Devices, Mini-Circuits, Amphenol, Glenair.

Сотрудничество с глобальными дистрибьюторами электронных компонентов, предоставляет возможность заказывать и получать с международных складов практически любой перечень компонентов в оптимальные для Вас сроки.

На всех этапах разработки и производства наши партнеры могут получить квалифицированную поддержку опытных инженеров.

Система менеджмента качества компании отвечает требованиям в соответствии с ГОСТ Р ИСО 9001, ГОСТ РВ 0015-002 и ЭС РД 009

Офис по работе с юридическими лицами:

105318, г.Москва, ул.Щербаковская д.3, офис 1107, 1118, ДЦ «Щербаковский»

Телефон: +7 495 668-12-70 (многоканальный)

Факс: +7 495 668-12-70 (доб.304)

E-mail: info@moschip.ru

Skype отдела продаж:
moschip.ru
moschip.ru_4
moschip.ru_6
moschip.ru_9