

General Description

The MAX4737/MAX4738/MAX4739 low-voltage, low on-resistance (R_{ON}), quad single-pole/single throw (SPST) analog switches operate from a single +1.8V to +5.5V supply. These devices are designed for USB 1.1 and audio switching applications.

The MAX4737/MAX4738/MAX4739 feature 4.5Ω R_{ON} (max) with 1.2Ω flatness and 0.4Ω matching between channels. These new switches feature guaranteed operation from +1.8V to +5.5V and are fully specified at 3V and 5V. These switches offer break-before-make switching (1ns) with $t_{ON} < 80ns$ and $t_{OFF} < 40ns$ at +2.7V. The digital logic inputs are +1.8V logic compatible with a +2.7V to +3.6V supply.

These switches are packaged in a chip-scale package (UCSP™), significantly reducing the required PC board area. The chip occupies only a 2mm x 2mm area and has a 4 x 4 bump array with a bump pitch of 0.5mm. These switches are also available in a 14-pin TSSOP and a 16-pin thin QFN (4mm x 4mm) package.

Applications

- Battery-Operated Equipment
- Audio/Video-Signal Routing
- Low-Voltage Data-Acquisition Systems
- Sample-and-Hold Circuits
- Data-Acquisition Systems
- Communications Circuits

UCSP is a trademark of Maxim Integrated Products, Inc.

Benefits and Features

- USB 1.1 Signal Switching
- 2ns (max) Differential Skew
- -3dB Bandwidth: >300MHz
- Low 20pF On-Channel Capacitance
- Low R_{ON}
 - 4.5Ω (max) (+3V Supply)
 - 3Ω (max) (+5V Supply)
- 0.4Ω (max) R_{ON} Match (+3V Supply)
- 1.2Ω (max) R_{ON} Flatness (+3V Supply)
- <0.5nA Leakage Current at +25°C
- High Off-Isolation: -55dB (10MHz)
- Low Crosstalk: -80dB (10MHz)
- Low Distortion: 0.03%
- +1.8V CMOS-Logic Compatible
- Single-Supply Operation from +1.8V to +5.5V
- Rail-to-Rail Signal Handling

MAX4737/MAX4738/ MAX4739

4.5Ω Quad SPST Analog Switches in UCSP

Absolute Maximum Ratings

(All Voltages Referenced to GND)

V+, IN_	-0.3V to +6.0V
COM_, NO_, NC_ (Note 1)	-0.3V to (V+ + 0.3V)
Continuous Current COM_, NO_, NC_	±100mA
Peak Current COM_, NO_, NC_ (pulsed at 1ms, 10% duty cycle)	±200mA
Continuous Power Dissipation (T _A = +70°C)	
14-Pin TSSOP (derate 6.3mW/°C above +70°C)	500mW
16-Bump UCSP (derate 8.3mW/°C above +70°C)	659mW
16-Pin Thin QFN (derate 25mW/°C above +70°C)	2000mW

ESD Method 3015.7	>2kV
Operating Temperature Range	-40°C to +85°C
Junction Temperature	+150°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (soldering, 10s)	+300°C
Bump Temperature (soldering)	
Infrared (15s)	+220°C
Vapor Phase (60s)	+215°C

Note 1: Signals on COM_, NO_, or NC_ exceeding V+ or GND are clamped by internal diodes. Limit forward-diode current to maximum current rating.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Electrical Characteristics—Single +3V Supply

(V+ = +2.7V to +3.6V, V_{IH} = +1.4V, V_{IL} = +0.5V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V+ = +3.0V, T_A = +25°C, unless otherwise noted.) (Notes 3, 4)

PARAMETER	SYMBOL	CONDITIONS	T _A	MIN	TYP	MAX	UNITS
Analog Signal Range	V _{COM_} , V _{NO_} , V _{NC_}			0		V+	V
ANALOG SWITCH							
On-Resistance (Note 5)	R _{ON}	V+ = 2.7V, I _{COM_} = 10mA; V _{NO_} or V _{NC_} = 1.5V	+25°C		3.0	4.5	Ω
			T _{MIN} to T _{MAX}			5	
On-Resistance Match Between Channels (Notes 5, 6)	ΔR _{ON}	V+ = 2.7V, I _{COM_} = 10mA; V _{NO_} or V _{NC_} = 1.5V	+25°C		0.1	0.4	Ω
			T _{MIN} to T _{MAX}			0.5	
On-Resistance Flatness (Note 7)	R _{FLAT(ON)}	V+ = 2.7V, I _{COM_} = 10mA; V _{NO_} or V _{NC_} = 1.0V, 1.5V, 2.0V	+25°C		0.6	1.2	Ω
			T _{MIN} to T _{MAX}			1.5	
NO_, NC_ Off-Leakage Current (Note 8)	I _{NO_(OFF)} , I _{NC_(OFF)}	V+ = 3.6V, V _{COM_} = 0.3V, 3.3V; V _{NO_} or V _{NC_} = 3.3V, 0.3V	+25°C	-0.5	+0.01	+0.5	nA
			T _{MIN} to T _{MAX}	-1		+1	
COM_ Off-Leakage Current (Note 8)	I _{COM_(OFF)}	V+ = 3.6V, V _{COM_} = 0.3V, 3.3V; V _{NO_} or V _{NC_} = 3.3V, 0.3V	+25°C	-0.5	+0.01	+0.5	nA
			T _{MIN} to T _{MAX}	-1		+1	
COM_ On-Leakage Current (Note 8)	I _{COM_(ON)}	V+ = 3.6V, V _{COM_} = 0.3V, 3.3V; V _{NO_} or V _{NC_} = 0.3V, 3.3V, or floating	+25°C	-1	+0.01	+1	nA
			T _{MIN} to T _{MAX}	-2		+2	

Electrical Characteristics—Single +3V Supply (continued)

(V+ = +2.7V to +3.6V, V_{IH} = +1.4V, V_{IL} = +0.5V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V+ = +3.0V, T_A = +25°C, unless otherwise noted.) (Notes 3, 4)

PARAMETER	SYMBOL	CONDITIONS	T _A	MIN	TYP	MAX	UNITS
DYNAMIC CHARACTERISTICS							
Turn-On Time	t _{ON}	V _{NO_} , V _{NC_} = 1.5V; R _L = 300Ω, C _L = 35pF, Figure 1	+25°C	40	80	ns	
			T _{MIN} to T _{MAX}	100			
Turn-Off Time	t _{OFF}	V _{NO_} , V _{NC_} = 1.5V; R _L = 300Ω, C _L = 35pF, Figure 1	+25°C	20	40	ns	
			T _{MIN} to T _{MAX}	50			
Break-Before-Make Time Delay (MAX4739 Only) (Note 8)	t _{BBM}	V _{NO_} , V _{NC_} = 1.5V; R _L = 300Ω, C _L = 35pF, Figure 2	+25°C	8		ns	
			T _{MIN} to T _{MAX}	1			
Skew (Note 8)	t _{SKEW}	R _S = 39Ω, C _L = 50pF, Figure 3	T _{MIN} to T _{MAX}	0.15	2	ns	
Charge Injection	Q	V _{GEN} = 2V, R _{GEN} = 0Ω, C _L = 1.0nF, Figure 4	+25°C	5		pC	
Off-Isolation (Note 9)	V _{ISO}	f = 10MHz; V _{NO_} , V _{NC_} = 1V _{P-P} ; R _L = 50Ω, C _L = 5pF, Figure 5a	+25°C	-55		dB	
		f = 1MHz; V _{NO_} , V _{NC_} = 1V _{P-P} ; R _L = 50Ω, C _L = 5pF, Figure 5a		-80			
Crosstalk (Note 10)	V _{CT}	f = 10MHz; V _{NO_} , V _{NC_} = 1V _{P-P} ; R _L = 50Ω, C _L = 5pF, Figure 5b	+25°C	-80		dB	
		f = 1MHz; V _{NO_} , V _{NC_} = 1V _{P-P} ; R _L = 50Ω, C _L = 5pF, Figure 5b		-110			
On-Channel -3dB Bandwidth	BW	Signal = 0dBm, C _L = 5pF, 50Ω in and out, Figure 5a	+25°C	300		MHz	
Total Harmonic Distortion	THD	R _L = 600Ω	+25°C	0.03		%	
NO_, NC_ Off-Capacitance	C _{NO_(OFF)} , C _{NC_(OFF)}	f = 1MHz, Figure 6	+25°C	9		pF	
Switch On-Capacitance	C _{ON}	f = 1MHz, Figure 6	+25°C	15		pF	
DIGITAL I/O							
Input Logic High Voltage	V _{IH}		T _{MIN} to T _{MAX}	1.4		V	
Input Logic Low Voltage	V _{IL}		T _{MIN} to T _{MAX}	0.5		V	
Input Leakage Current	I _{IN}	V+ = 3.6V, V _{IN_} = 0 or 5.5V	T _{MIN} to T _{MAX}	-0.1	+0.1	μA	

Electrical Characteristics—Single +3V Supply (continued)

(V+ = +2.7V to +3.6V, V_{IH} = +1.4V, V_{IL} = +0.5V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V+ = +3.0V, T_A = +25°C, unless otherwise noted.) (Notes 3, 4)

PARAMETER	SYMBOL	CONDITIONS	T _A	MIN	TYP	MAX	UNITS
SUPPLY							
Supply Voltage Range	V+		T _{MIN} to T _{MAX}	1.8		5.5	V
Positive Supply Current	I+	V+ = 5.5V, V _{INL} = 0V or V+	T _{MIN} to T _{MAX}			1	μA

Electrical Characteristics—Single +5V Supply

(V+ = +4.2V to +5.5V, V_{IH} = +2.0V, V_{IL} = +0.8V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V+ = +5.0V, T_A = +25°C, unless otherwise noted.) (Notes 3, 4)

PARAMETER	SYMBOL	CONDITIONS	T _A	MIN	TYP	MAX	UNITS
Analog Signal Range	V _{COM_} , V _{NO_} , V _{NC_}		T _{MIN} to T _{MAX}	0		V+	V
ANALOG SWITCH							
On-Resistance (Note 5)	R _{ON}	V+ = 4.2V; I _{COM_} = 10mA; V _{NO_} or V _{NC_} = 3.5V	+25°C		1.7	3.0	Ω
			T _{MIN} to T _{MAX}			3.5	
On-Resistance Match Between Channels (Notes 5, 6)	ΔR _{ON}	V+ = 4.2V; I _{COM_} = 10mA; V _{NO_} or V _{NC_} = 3.5V	+25°C		0.1	0.3	Ω
			T _{MIN} to T _{MAX}			0.4	
On-Resistance Flatness (Note 7)	R _{FLAT(ON)}	V+ = 4.2V; I _{COM_} = 10mA; V _{NO_} or V _{NC_} = 1.0V, 2.0V, 3.5V	+25°C		0.4	1.2	Ω
			T _{MIN} to T _{MAX}			1.5	
NO_, NC_ Off-Leakage Current (Note 8)	I _{NO_(OFF)} , I _{NC_(OFF)}	V+ = 5.5V; V _{COM_} = 1.0V, 4.5V; V _{NO_} or V _{NC_} = 4.5V, 1.0V	+25°C	-0.5	0.01	+0.5	nA
			T _{MIN} to T _{MAX}	-1		+1	
COM_ Off-Leakage Current (Note 8)	I _{COM_(OFF)}	V+ = 5.5V; V _{COM_} = 1V, 4.5V; V _{NO_} or V _{NC_} = 4.5V, 1V	+25°C	-0.5	0.01	+0.5	nA
			T _{MIN} to T _{MAX}	-1		+1	
COM_ On-Leakage Current (Note 8)	I _{COM_(ON)}	V+ = 5.5V; V _{COM_} = 1.0V, 4.5V; V _{NO_} or V _{NC_} = 1.0V, 4.5V, or floating	+25°C	-1	0.01	+1	nA
			T _{MIN} to T _{MAX}	-2		+2	
DYNAMIC CHARACTERISTICS							
Turn-On Time	t _{ON}	V _{NO_} , V _{NC_} = 3.0V; R _L = 300Ω, C _L = 35pF, Figure 1	+25°C		30	80	ns
			T _{MIN} to T _{MAX}			100	
Turn-Off Time	t _{OFF}	V _{NO_} , V _{NC_} = 3.0V; R _L = 300Ω, C _L = 35pF, Figure 1	+25°C		20	40	ns
			T _{MIN} to T _{MAX}			50	

Electrical Characteristics—Single +5V Supply (continued)

(V+ = +4.2V to +5.5V, V_{IH} = +2.0V, V_{IL} = +0.8V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V+ = +5.0V, T_A = +25°C, unless otherwise noted.) (Notes 3, 4)

PARAMETER	SYMBOL	CONDITIONS	T _A	MIN	TYP	MAX	UNITS
Break-Before-Make Time Delay (MAX4739 Only) (Note 8)	t _{BBM}	V _{NO_} , V _{NC_} = 3.0V; R _L = 300Ω, C _L = 35pF, Figure 2	+25°C		8		ns
			T _{MIN} to T _{MAX}	1			
Skew (Note 8)	t _{SKEW}	R _S = 39Ω, C _L = 50pF, Figure 3	T _{MIN} to T _{MAX}		0.15	2	ns
DIGITAL I/O							
Input Logic High Voltage	V _{IH}		T _{MIN} to T _{MAX}	2.0			V
Input Logic Low Voltage	V _{IL}		T _{MIN} to T _{MAX}			0.8	V
Input Leakage Current	I _{IN}	V+ = 5.5V, V _{IN_} = 0V or V+	T _{MIN} to T _{MAX}	-0.1		+0.1	μA
POWER SUPPLY							
Power-Supply Range	V+		T _{MIN} to T _{MAX}	1.8		5.5	V
Positive Supply Current	I+	V+ = 5.5V, V _{IN_} = 0V or V+	T _{MIN} to T _{MAX}			1	μA

Note 3: UCSP parts are 100% tested at +25°C only, and guaranteed by design over the specified temperature range. TSSOP and thin QFN parts are 100% tested at T_{MAX} and guaranteed by design over the specified temperature range.

Note 4: The algebraic convention used in this data sheet is where the most negative value is a minimum and the most positive value is a maximum.

Note 5: Guaranteed by design for UCSP and thin QFN parts.

Note 6: ΔR_{ON} = R_{ON(MAX)} - R_{ON(MIN)}.

Note 7: Flatness is defined as the difference between the maximum and minimum value of on-resistance as measured over the specified analog signal ranges.

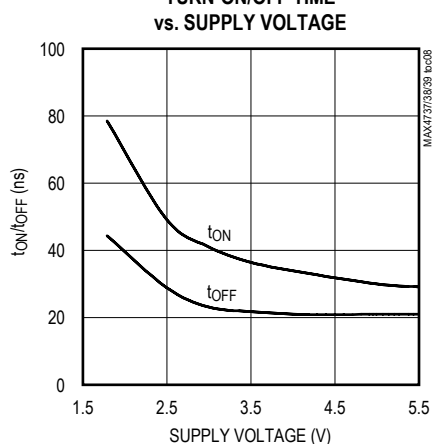
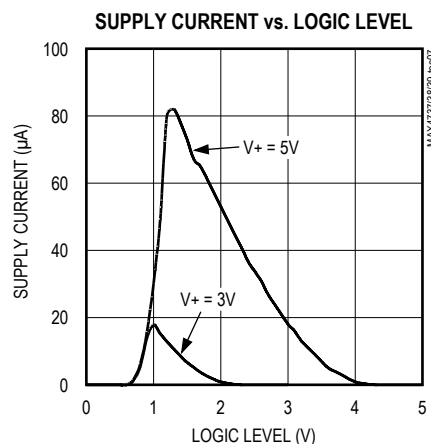
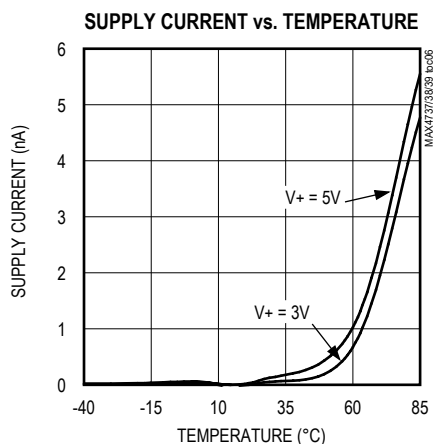
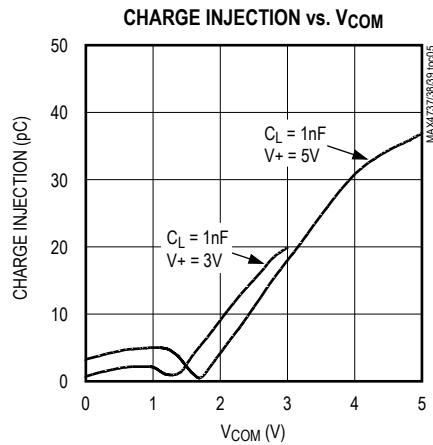
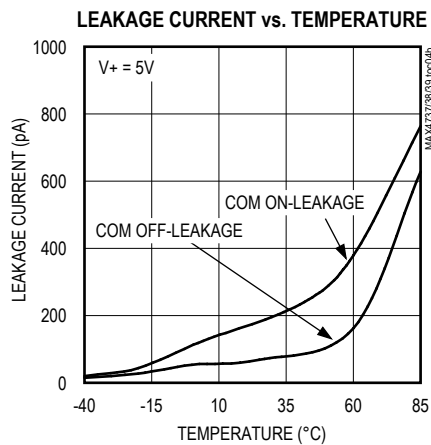
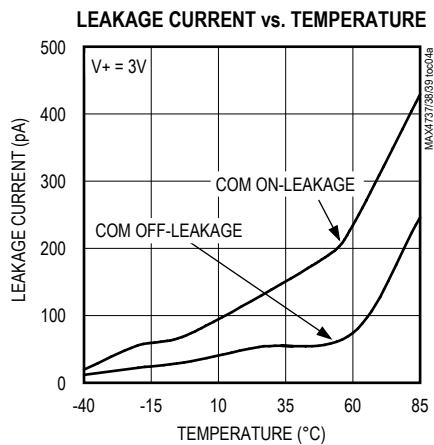
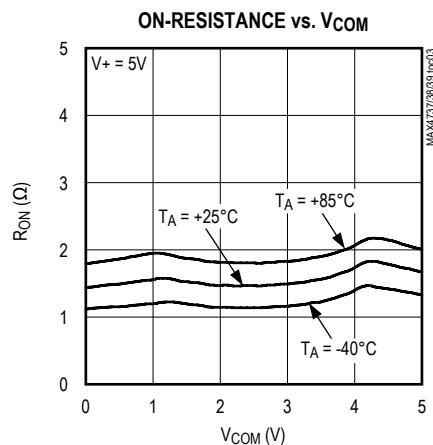
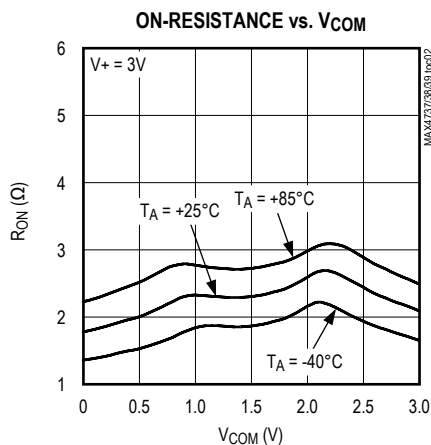
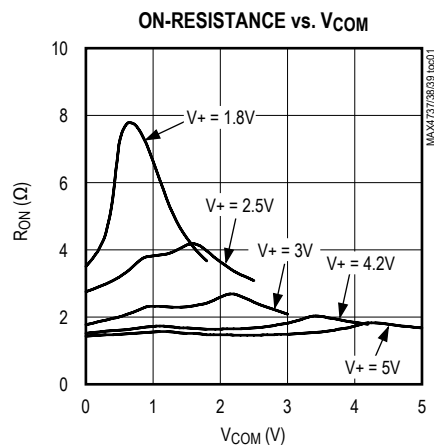
Note 8: Guaranteed by design.

Note 9: Off-Isolation = 20log₁₀ (V_{COM} / V_{NO}). V_{COM} = output, V_{NO} = input to off switch.

Note 10: Between any two switches.

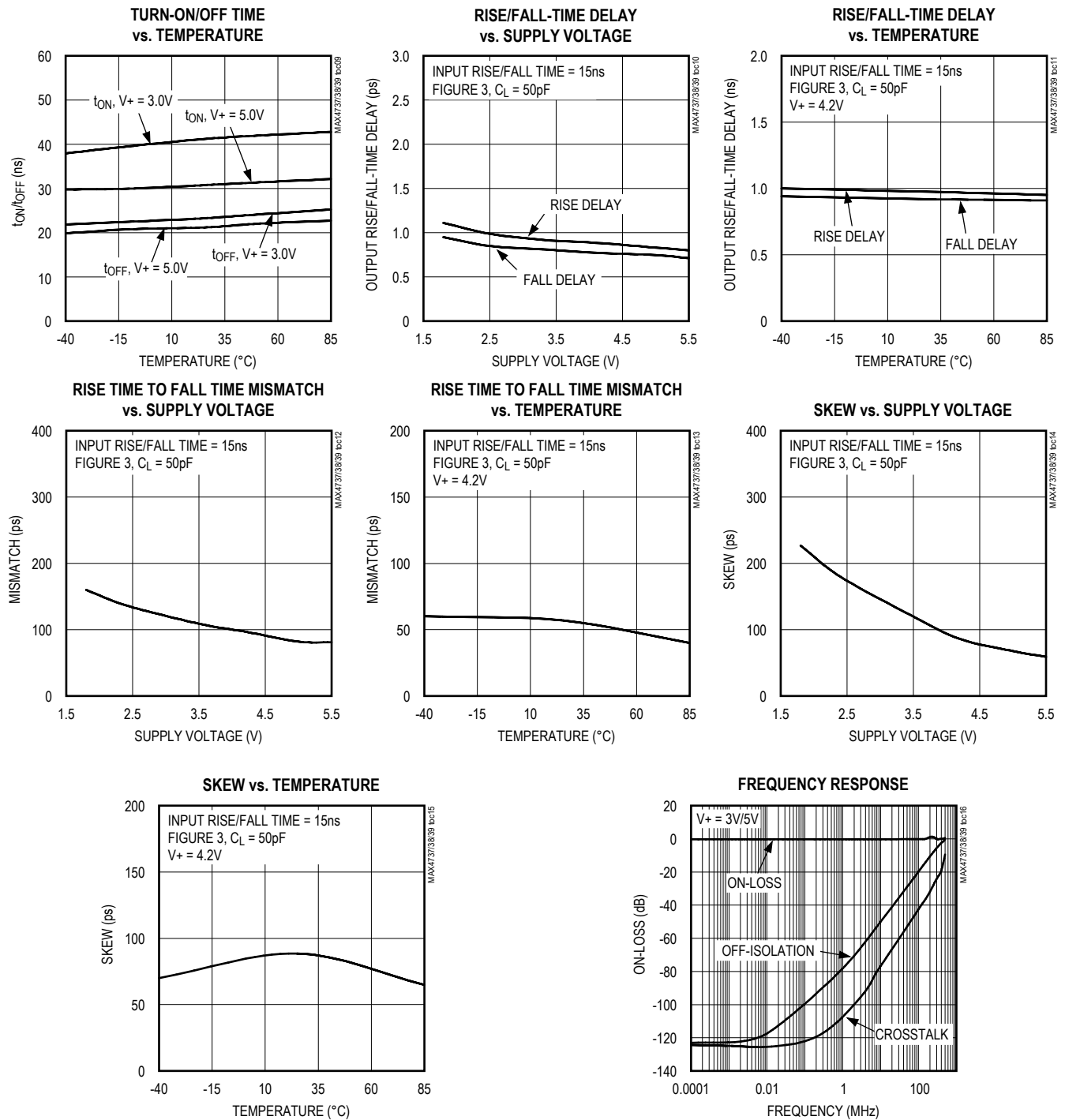
Typical Operating Characteristics

($T_A = +25^\circ\text{C}$, unless otherwise noted.)



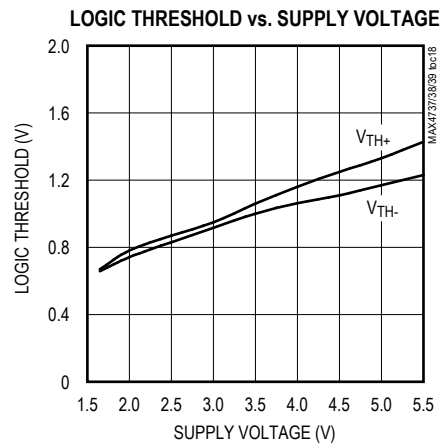
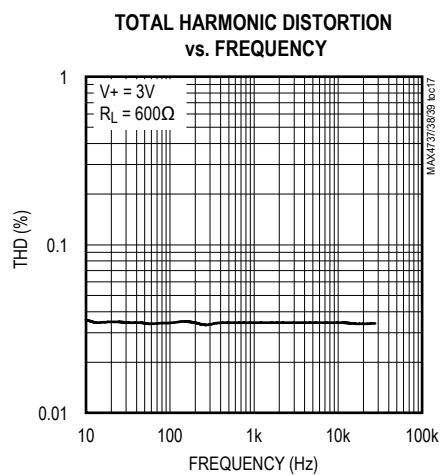
Typical Operating Characteristics (continued)

($T_A = +25^\circ\text{C}$, unless otherwise noted.)



Typical Operating Characteristics (continued)

($T_A = +25^\circ\text{C}$, unless otherwise noted.)



MAX4737/MAX4738/
MAX4739

4.5Ω Quad SPST Analog Switches in UCSP

Pin Configurations/Functional Diagrams/Truth Tables

TOP VIEW
(BUMPS SIDE DOWN)

MAX4737

1

2

3

4

A

B

C

D

IN2

IN3

NO3

COM3

COM2

GND

COM4

NO4

COM1

NO1

IN1

IN4

UCSP

MAX4738

1

2

3

4

A

B

C

D

IN2

IN3

NC3

COM3

COM2

GND

COM4

NC4

COM1

NC1

IN1

IN4

UCSP

MAX4739

1

2

3

4

A

B

C

D

IN2

IN3

NO3

COM3

COM2

GND

COM4

NC4

COM1

NO1

IN1

IN4

UCSP

IN ₋	NO ₋	NC ₋
LOW	OFF	ON
HIGH	ON	OFF

MAX4737

NO1

COM1

NO2

COM2

IN2

IN3

GND

1

2

3

4

5

6

7

+

14

13

12

11

10

9

8

V+

IN1

IN4

NO4

COM4

COM3

NO3

TSSOP

INPUT	SWITCH STATE
LOW	OFF
HIGH	ON

MAX4738

NC1

COM1

NC2

COM2

IN2

IN3

GND

1

2

3

4

5

6

7

+

14

13

12

11

10

9

8

V+

IN1

IN4

NC4

COM4

COM3

NC3

TSSOP

INPUT	SWITCH STATE
LOW	ON
HIGH	OFF

MAX4739

NO1

COM1

NC2

COM2

IN2

IN3

GND

1

2

3

4

5

6

7

+

14

13

12

11

10

9

8

V+

IN1

IN4

NC4

COM4

COM3

NO3

TSSOP

INPUT	NO1, NO3	NC2, NC4
LOW	OFF	ON
HIGH	ON	OFF

MAX4737

COM1

NO2

COM2

IN2

IN3

GND

NO3

N.C.

1

2

3

4

5

6

7

8

+

16

15

14

13

12

11

10

9

V+

IN1

IN4

NO4

COM4

COM3

N.C.

QFN

INPUT	SWITCH STATE
LOW	OFF
HIGH	ON

MAX4738

COM1

NC2

COM2

IN2

IN3

GND

NC3

N.C.

1

2

3

4

5

6

7

8

+

16

15

14

13

12

11

10

9

V+

IN1

IN4

NC4

COM4

COM3

N.C.

QFN

INPUT	SWITCH STATE
LOW	ON
HIGH	OFF

MAX4739

COM1

NC2

COM2

IN2

IN3

GND

NO3

N.C.

1

2

3

4

5

6

7

8

+

16

15

14

13

12

11

10

9

V+

IN1

IN4

NC4

COM4

COM3

N.C.

QFN

INPUT	NO1, NO3	NC2, NC4
LOW	OFF	ON
HIGH	ON	OFF

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Pin Descriptions

PIN									NAME	FUNCTION
MAX4737			MAX4738			MAX4739				
UCSP	TSSOP	THIN QFN	UCSP	TSSOP	THIN QFN	UCSP	TSSOP	THIN QFN		
D2	1	15	—	—	—	D2	1	15	NO1	Analog-Switch Normally Open Terminal
—	—	—	D2	1	15	—	—	—	NC1	Analog-Switch Normally Closed Terminal
D1	2	1	D1	2	1	D1	2	1	COM1	Analog-Switch Common Terminal
C1	3	2	—	—	—	—	—	—	NO2	Analog-Switch Normally Open Terminal
—	—	—	C1	3	2	C1	3	2	NC2	Analog-Switch Normally Closed Terminal
B1	4	3	B1	4	3	B1	4	3	COM2	Analog-Switch Common Terminal
A1	5	4	A1	5	4	A1	5	4	IN2	Logic-Control Digital Input
A2	6	5	A2	6	5	A2	6	5	IN3	Logic-Control Digital Input
B3	7	6	B3	7	6	B3	7	6	GND	Ground. Connect to digital ground.
A3	8	7	—	—	—	A3	8	7	NO3	Analog-Switch Normally Open Terminal
—	—	—	A3	8	7	—	—	—	NC3	Analog-Switch Normally Closed Terminal
A4	9	9	A4	9	9	A4	9	9	COM3	Analog-Switch Common Terminal
B4	10	10	B4	10	10	B4	10	10	COM4	Analog-Switch Common Terminal

Detailed Description

The MAX4737/MAX4738/MAX4739 quad SPST analog switches operate from a single +1.8V to +5.5V supply. The MAX4737/MAX4738/MAX4739 offer excellent AC characteristics, <0.5nA leakage current, less than 1ns differential skew, and 15pF on-channel capacitance. All of these devices are CMOS-logic compatible with V+ to GND signal handling capability.

The MAX4737/MAX4738/MAX4739 are USB-complaint switches that provide 4.5Ω (max) on-resistance and 15pF on-channel capacitance to maintain signal integrity. At 12Mbps (USB full-speed data rate specification), the MAX4737/MAX4738/MAX4739 introduce less than 2ns propagation delay between input and output signals and less than 0.5ns change in skew for the output signals (see Figure 4).

The MAX4737 has four normally open (NO) switches, the MAX4738 has four normally closed (NC) switches, and the MAX4739 has two NO switches and two NC switches.

Applications Information

Digital Control Inputs

The MAX4737/MAX4738/MAX4739 logic inputs accept up to +5.5V regardless of supply voltage. For example, with a +3.3V supply, IN₋ can be driven low to GND and high to +5.5V allowing for mixing of logic levels in a system. Driving the control logic inputs rail-to-rail minimizes power consumption. For a +1.8V supply voltage, the logic thresholds are 0.5V (low) and 1.4V (high); for a +5V supply voltage, the logic thresholds are 0.8V (low) and 2.0V (high).

Analog Signal Levels

Analog signals that range over the entire supply voltage (V+ to GND) are passed with very little change in on-resistance (see *Typical Operating Characteristics*). The switches are bidirectional, so the NO₋, NC₋, and COM₋ pins can be either inputs or outputs.

Power-Supply Bypassing

Power-supply bypassing improves noise margin and prevents switching noise from propagating from the V+ supply to other components. A 0.1μF capacitor connected from V+ to GND is adequate for most applications.

UCSP Applications Information

For the latest application details on UCSP construction, dimensions, tape carrier information, PC board techniques, bump-pad layout, and recommended reflow temperature profile, as well as the latest information on reliability testing results, refer to the Application Note: *UCSP—A Wafer-Level Chip-Scale Package* on Maxim's web site at www.maximintegrated.com/ucsp.

Test Circuits/Timing Diagrams

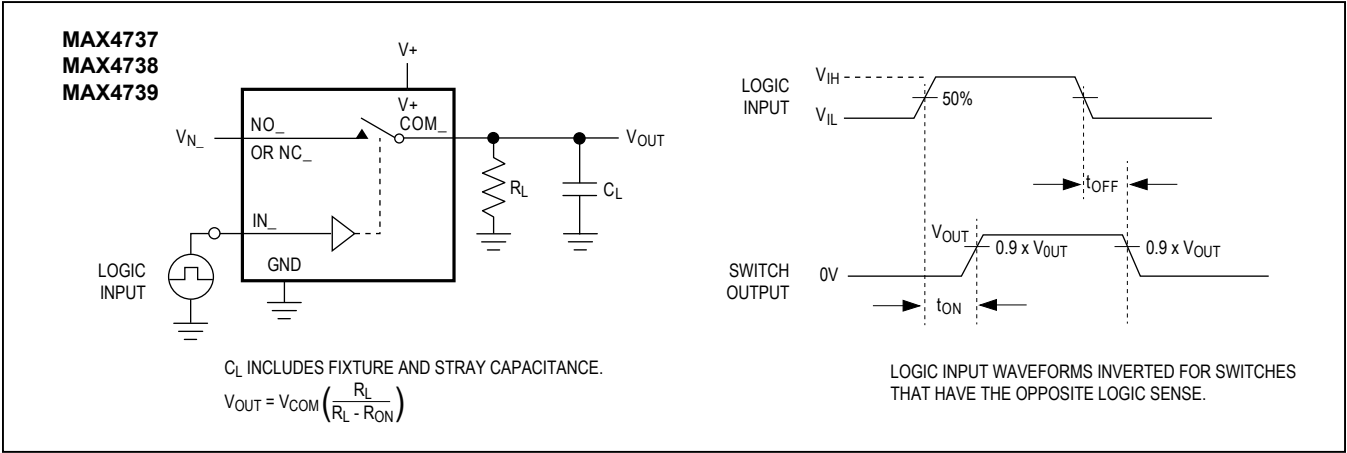


Figure 1. Switching Time

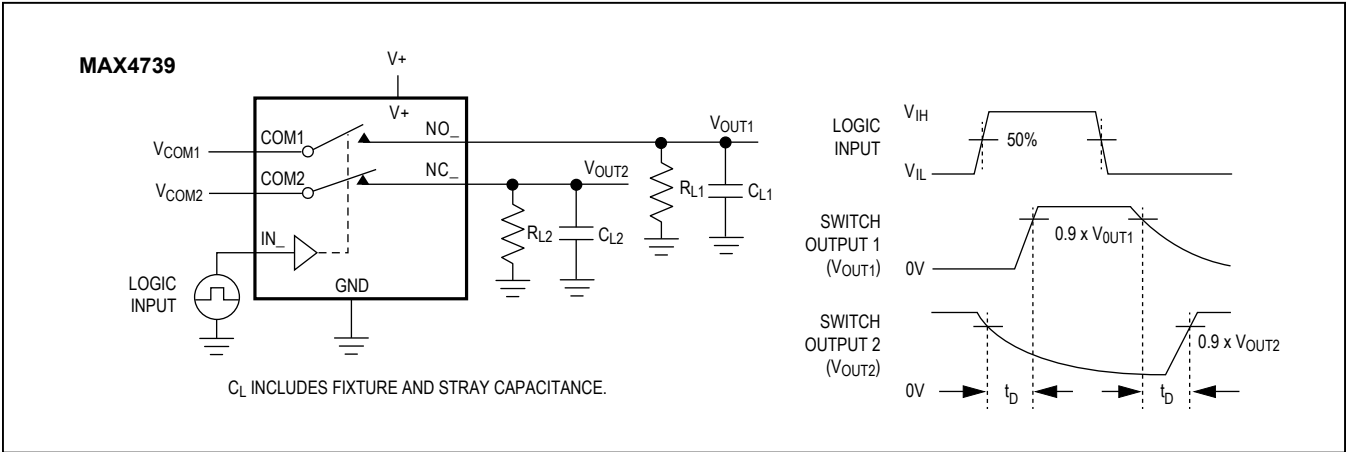


Figure 2. Break-Before-Make Interval

The diagrams illustrate the timing characteristics of a switch in a signal path. The top diagram shows a rising input signal (INPUT A) and a rising output signal (OUTPUT B). The bottom diagram shows a falling input signal (INPUT A-) and a falling output signal (OUTPUT B-). Both diagrams include a circuit schematic with a buffer, a resistor R_S , and a switch connecting to a load capacitor C_L . The timing parameters shown are t_{ri} , t_{ri0} , t_{skew_i} , t_{ri1} , t_{ro} , t_{ro0} , t_{skew_o} , and t_{ri2} .

Test Circuits/Timing Diagrams (continued)

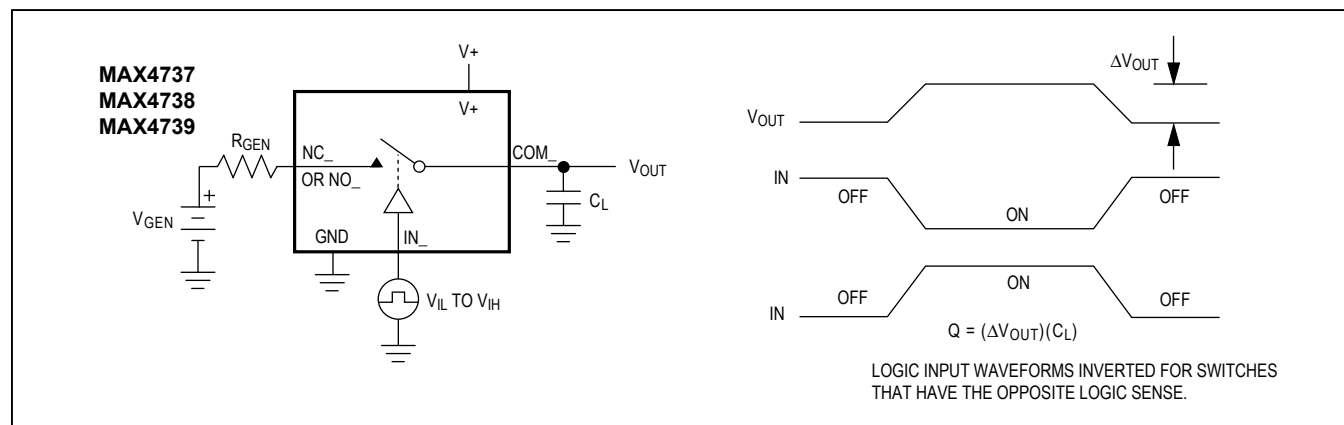


Figure 4. Charge Injection

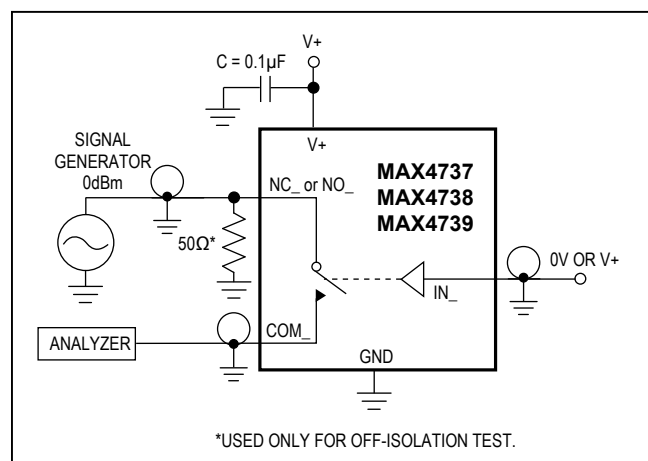


Figure 5a. On-Loss and Off-Isolation

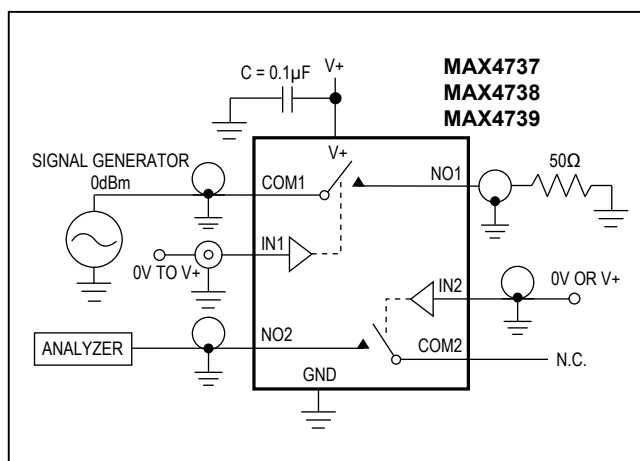


Figure 5b. Crosstalk Test Circuit

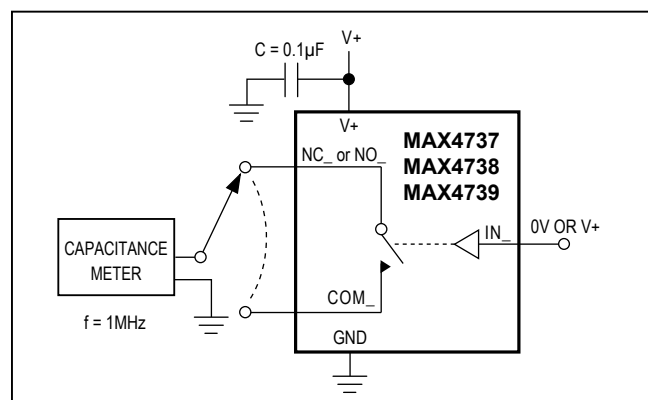


Figure 6. Channel Off-/On-Capacitance

MAX4737/MAX4738/ MAX4739

4.5Ω Quad SPST Analog Switches in UCSP

Ordering Information

PART	TEMP RANGE	PIN/BUMP- PACKAGE	TOP MARK
MAX4737 EUD	-40°C to +85°C	14 TSSOP	—
MAX4737ETE	-40°C to +85°C	16 Thin QFN	—
MAX4737EBE+T	-40°C to +85°C	16 UCSP-16	4737
MAX4738 EUD	-40°C to +85°C	14 TSSOP	—
MAX4738ETE	-40°C to +85°C	16 Thin QFN	—
MAX4738EBE+T	-40°C to +85°C	16 UCSP-16	4738
MAX4739 EUD	-40°C to +85°C	14 TSSOP	—
MAX4739ETE	-40°C to +85°C	16 Thin QFN	—
MAX4739EBE+T	-40°C to +85°C	16 UCSP-16	4739

+Denotes a lead(Pb)-free/RoHS-compliant package.

Package Information

For the latest package outline information and land patterns (footprints), go to www.maximintegrated.com/packages. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
14 TSSOP	U14+1	21-0066	90-0113
16 QFN	T1644+4	21-0139	90-0070
16 UCSP	B16+4	21-0101	—

Chip Information

TRANSISTOR COUNT: 361

PROCESS: CMOS

MAX4737/MAX4738/
MAX4739

4.5Ω Quad SPST Analog Switches in UCSP

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
2	1/16	Pb-free part numbers updated	1

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