## General Description

The MAX3956 is an 11.3Gbps, highly-integrated, low-power transceiver with digital diagnostics monitoring (DDM) designed for next-generation Ethernet transmission systems. The receiver incorporates a limiting amplifier and loss-of-signal (LOS) circuit. The limiting amplifier features dual-path architecture optimizing the performance for signals up to 4.25Gbps and up to 11.3Gbps, respectively. The transmitter incorporates Maxim's proprietary DC-coupled laser driver interface and closed-loop control of laser average power. This part is optimized to enable 0.8W maximum power dissipation target of SFP+ MSA based modules.

The MAX3956 supports differential AC-coupled signaling with 50Ω termination at Rx input, Rx output, and Tx input. The Tx output is a DC-coupled 25Ω laser diode interface with dedicated pins for the laser anode (TOUTA) and the laser cathode (TOUTC).

An integrated 12-bit analog-to-digital converter (ADC) is utilized to provide digital monitors of internal/external temperature, $V_{CC}$, and received signal strength indication (RSSI). The MAX3956's digital monitors and the use of a 2-wire or 3-wire slave interface enables configuration through a digital-only microcontroller (µC).

The MAX3956 operates from a single +3.3V supply and over a -40°C to +95°C temperature range and is available in a standard 5mm x 5mm, 32-pin TQFN-EP package.

## Applications

- 10GBASE-LR SFP+ Optical Transceivers

## Benefits and Features

Low Power Consumption
- Enables < 0.8W Total SFP+ Module Power Dissipation
- 380mW Typical IC Power Dissipation at 3.3V ($I_{LD\_MOD}$ = 45mA, $I_{BIAS}$ = 45mA)

Flexibility
- Multirate up to 11.3Gbps (NRZ) Operation with Rate Select for 1.25Gbps to 4.25Gbps Operation
- Programmable Laser-Diode Modulation Current from 10mA to 85mA
- Programmable Tx Input Equalization and Rx Output Deemphasis

Safety and Monitoring
- Integrated Eye Safety Features with Maskable Fault and Interrupt Signal Generation
- Analog Monitors with Integrated 12-Bit ADC, Fully Supporting SFF-8472 DDM

Accurate Analog Measurements
- High-Accuracy Temperature, $V_{CC}$, and RSSI Sensors
- Enables Use of Simple Digital-Only µC

## Simplified Block Diagram
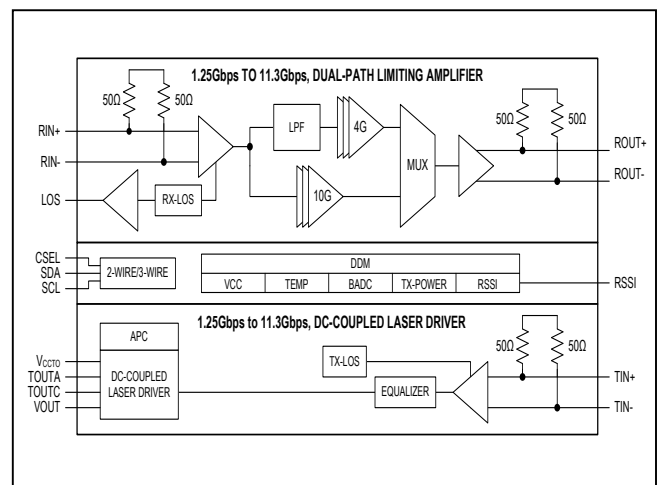
## Absolute Maximum Ratings

Voltage at $V_{CCX}$, $V_{CCRO}$, $V_{CCT}$, $V_{CCTO}$ ...............-0.3V to 4.0V
Voltage at REGFILT ..............................................-0.3V to 2.0V
Current into $V_{CCTO}$ .......................................-15mA to +180mA
Current into REGFILT .......................................-15mA to +15mA
Current into TOUTA and TOUTC .................................+150mA
Current into VOUT ...........................................-2mA to +90mA
Current into TIN+, TIN-, RIN+, and RIN- .........-15mA to +15mA
Current into ROUT+ and ROUT- ....................-30mA to +30mA
Voltage at TIN+, TIN-, RIN+, RIN-, LOS,
    DISABLE, FAULT, MDIN,
    RSSI, SCL, SDA, INTRPT, and CSEL -0.3V to ($V_{CCX}$ + 0.3V)

Voltage at TSNS, TGND .......................................-0.3V to 1.2V
Voltage at BADC, I.C. ..........................................-0.3V to 2V
Voltage at TOUTA ...............($V_{CCTO}$ - 1.3V) to ($V_{CCTO}$ + 1.3V)
Voltage at TOUTC and VOUT ..............0.3V to ($V_{CCTO}$ - 0.4V)
Continuous Power Dissipation ($T_A$ = +70°C)
    TQFN (derate 34.5mW/°C above +70°C).................2759mW
Junction Temperature......................................................+150°C
Storage Temperature Range........................... -55°C to +150°C
Lead Temperature (soldering, 10s) ...............................+300°C
Soldering Temperature (reflow)......................................+260°C

*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

## Package Thermal Characteristics (Note 1)

TQFN
    Junction-to-Ambient Thermal Resistance ($\theta_{JA}$) ..........29°C/W
    Junction-to-Case Thermal Resistance ($\theta_{JC}$)..............1.7°C/W

**Note 1:** Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

## Electrical Characteristics

($V_{CCX}$ = $V_{CCRO}$ = $V_{CCT}$ = 2.85V to 3.47V, $V_{CCTO}$ = 2.97V to 3.47V, $V_{GND}$ = 0V, $T_A$ = -40°C to +95°C. Typical values are at $V_{CCX}$ = $V_{CCRO}$ = $V_{CCT}$ = $V_{CCTO}$ = 3.3V, 14Ω single-ended load for TOUTC/TOUTA, and $T_A$ = +25°C, unless otherwise noted. See Figure 1 for electrical setup.) (Note 2)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| Power-Supply Current | $I_{CC}$ | Excludes current through TOUTC and TOUTA; $I_{LD\_MOD}$ = 60mA, $I_{LD\_DC}$ = 40mA, and SET_CML[4:0] = 3d | | 105 | 130 | mA |
| Power-On-Reset (Enable Part) | $V_{POR\_DE}$ | | | 2.5 | | V |
| Power-On-Reset (Disable Part) | $V_{POR\_AS}$ | | | 2.4 | | V |
| **RX INPUT SPECIFICATION** | | | | | | |
| Input Sensitivity for BER < $10^{-12}$ | $V_{RIN\_MIN}$ | $2^{31}$-1 PRBS at 11.3Gbps | | 3 | | $mV_{P-P}$ |
| Differential Input Resistance | $R_{RIN}$ | | | 100 | | Ω |
| **RX OUTPUT SPECIFICATION (SET_RXDE[2:0] = 0xx)** | | | | | | |
| Differential Output Voltage Programming Range | $V_{ROUT}$ | See Table 7 for more information | 450 | | 800 | $mV_{P-P}$ |
| Differential Output Voltage when Squelched | $V_{ROUT}$ | SQ_EN = 1 | | 5 | | $mV_{P-P}$ |
| Differential Output Resistance | $R_{ROUT}$ | | | 100 | | Ω |

## Electrical Characteristics (continued)

($V_{CCX}$ = $V_{CCRO}$ = $V_{CCT}$ = 2.85V to 3.47V, $V_{CCTO}$ = 2.97V to 3.47V, $V_{GND}$ = 0V, $T_A$ = -40°C to +95°C. Typical values are at $V_{CCX}$ = $V_{CCRO}$ = $V_{CCT}$ = $V_{CCTO}$ = 3.3V, 14Ω single-ended load for TOUTC/TOUTA, and $T_A$ = +25°C, unless otherwise noted. See Figure 1 for electrical setup.) (Note 2)

| PARAMETER | SYMBOL | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| Deterministic Jitter | DJ | 10.3Gbps (Notes 3, 4, and 5) | | | 4.6 | 10 | ps$_{P-P}$ |
| | | 11.3Gbps (Notes 3, 4, and 5) | | | 5.6 | 11 | |
| Random Jitter | RJ | $V_{RIN}$ = 60mV$_{P-P}$ at 10.3Gbps, 11111 00000 pattern, SET_CML[4:0] = 10d (Note 3) | | | 0.25 | 0.4 | ps$_{RMS}$ |
| ROUT Rise/Fall Time | $t_R/t_F$ | 20% to 80%, RSEL = high, (Notes 3 and 5) 11111 00000 pattern | | | 27 | 35 | ps |
| **RX OMA BASED LOSS-OF-SIGNAL (LOS) SPECIFICATION (Notes 3 and 7)** | | | | | | | |
| Assert/Deassert Time | | (Note 6) | | 2.3 | | 80 | µs |
| LOS Low Level Setting | | SET_LOS[6:0] = 8d | Assert level | 6 | 10 | 16 | mV$_{P-P}$ |
| | | | Deassert level | 12 | 16.7 | 23 | |
| LOS Medium Level Setting | | SET_LOS[6:0] = 38d | Assert level | | 48 | | mV$_{P-P}$ |
| | | | Deassert level | | 78 | | |
| LOS High Level Setting | | SET_LOS[6:0] = 101d | Assert level | | 121 | | mV$_{P-P}$ |
| | | | Deassert level | | 197 | | |
| LOS Output Masking Time Range | | LOS_MASKTIME = 0d | | | 0 | | ms |
| | | LOS_MASKTIME = 127d | | | 4.6 | | |
| LOS Output Masking Time Setting Resolution | | (Note 8) | | | 36 | | µs |
| **TX INPUT SPECIFICATION** | | | | | | | |
| Differential Input Resistance | $R_{TIN}$ | | | | 100 | | Ω |
| **LASER DC CURRENT GENERATOR (Note 9)** | | | | | | | |
| Maximum DC-ON Current | $I_{DC\_MAX}$ | Current into VOUT pin | | 57 | | | mA |
| Minimum DC-ON Current | $I_{DC\_MIN}$ | Current into VOUT pin | | | 0.7 | 1 | mA |
| Maximum DC-OFF Current | $I_{DC\_OFF}$ | Laser current into VOUT pin when Tx output disabled | | | | 0.1 | mA |
| **LASER MODULATOR OUTPUT (TX_EQ[1:0] = 00) (Note 10)** | | | | | | | |
| Maximum Modulation ON-Current | $I_{LD\_MOD\_MAX}$ | Current into TOUTC, external 10Ω differential load | | 85 | | | mA |
| Minimum Modulation ON-Current | $I_{LD\_MOD\_MIN}$ | Current into TOUTC, external 10Ω differential load | | | | 10 | mA |
| Modulation Output Termination | $R_{TOUT}$ | Single-ended resistance | | | 25 | | Ω |
| Maximum Modulation OFF-Current | $I_{LD\_MOD\_OFF}$ | Current into TOUTC pin when Tx output disabled | | | | 0.1 | mA |
| Modulation Current DAC Stability | | 10mA < $I_{LD\_MOD}$ < 85mA (Notes 3 and 11) | | | 1.5 | 4 | % |

## Electrical Characteristics (continued)

($V_{CCX}$ = $V_{CCRO}$ = $V_{CCT}$ = 2.85V to 3.47V, $V_{CCTO}$ = 2.97V to 3.47V, $V_{GND}$ = 0V, $T_A$ = -40°C to +95°C. Typical values are at $V_{CCX}$ = $V_{CCRO}$ = $V_{CCT}$ = $V_{CCTO}$ = 3.3V, 14Ω single-ended load for TOUTC/TOUTA, and $T_A$ = +25°C, unless otherwise noted. See Figure 1 for electrical setup.) (Note 2)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| **LASER MODULATOR OUTPUT (TX_EQ[1:0] = 00, 10mA < $I_{LD\_MOD}$ < 85mA, $V_{TIN}$ = 150 to 1000mV$_{P-P}$ differential amplitude) (Notes 3 and 4)** | | | | | | |
| Modulation Current Rise/Fall Time | $t_R$/$t_F$ | 20% to 80%, 11111 00000 pattern | | 24 | 35 | ps |
| Deterministic Jitter | DJ | 10.3Gbps | | 5 | 11 | ps$_{P-P}$ |
| | | 11.3Gbps | | 5 | 11 | |
| Random Jitter | RJ | 11111 00000 pattern | | 0.23 | 0.55 | ps$_{RMS}$ |
| **APC LOOP OPERATION SPECIFICATION** | | | | | | |
| MD Average Current Range | $I_{MDIN\_AVG}$ | Average current sunk from MDIN pin | 50 | | 2000 | µA |
| Initialization Time | t_init | $I_{DC}$ = 40mA, $I_{MOD}$ = 60mA, $I_{DC\_init}$ = 0mA, ER = 9dB, time from restart to $I_{DC}$ and $I_{MOD}$ at 90% of steady state | | 0.1 | | ms |
| **TIMING REQUIREMENTS (Note 3)** | | | | | | |
| DISABLE Assert Time | t_off | Time from rising edge of DISABLE input signal to 10% of $I_{DC}$ and $I_{MOD}$ | | 1.5 | 10 | µs |
| DISABLE Negate Time | t_on | Time from falling edge of DISABLE to $I_{DC}$ and $I_{LD\_MOD}$ at 90% of steady state when FAULT = low before reset | | 8 | | µs |
| FAULT Reset Time | t_recovery | Time from negation of latched fault using DISABLE to $I_{LD\_MOD}$ + $I_{DC}$ at 90% of steady state | | 8 | | µs |
| FAULT Assert Time | t_fault | Time from fault to TX_FAULT = high, $C_{FAULT}$ ≤ 20pF, $R_{FAULT}$ = 4.7kΩ | | 1 | 3 | µs |
| DISABLE to Reset Time | | Time DISABLE must be held high to reset fault | 4 | | | µs |
| **SAFETY FEATURES** | | | | | | |
| Fault Assert Threshold at VOUT | | FAULT always occurs for VOUT < $V_{CCTO}$ - 2.8V | | $V_{CCTO}$ - 2.8V | | V |
| Fault Deassert Threshold at VOUT | | FAULT never occurs for VOUT ≥ $V_{CCTO}$ - 2.0V | | $V_{CCTO}$ - 2.0V | | V |
| Fault Assert Threshold at TOUTC | | FAULT always occurs for $V_{TOUTC}$ < 0.24V | | 0.24 | | V |
| Fault Deassert Threshold at TOUTC | | FAULT never occurs for $V_{TOUTC}$ ≥ 0.58V | | 0.58 | | V |
| Fault Threshold at TOUTA | | FAULT always occurs for $V_{TOUTA}$ < $V_{CCTO}$ - 1.85V | | $V_{CCTO}$ - 1.85V | | V |

## Electrical Characteristics (continued)

($V_{CCX}$ = $V_{CCRO}$ = $V_{CCT}$ = 2.85V to 3.47V, $V_{CCTO}$ = 2.97V to 3.47V, $V_{GND}$ = 0V, $T_A$ = -40°C to +95°C. Typical values are at $V_{CCX}$ = $V_{CCRO}$ = $V_{CCT}$ = $V_{CCTO}$ = 3.3V, 14Ω single-ended load for TOUTC/TOUTA, and $T_A$ = +25°C, unless otherwise noted. See Figure 1 for electrical setup.) (Note 2)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| Fault Deassert Threshold at TOUTA | | FAULT never occurs for $V_{TOUTA}$ ≥ $V_{CCTO}$ - 1.34V | | $V_{CCTO}$ - 1.34V | | V |
| **RSSI MONITOR** | | | | | | |
| ADC Resolution | | | | 16 | | bits |
| LSb Size | | | | 35.5 | | nA |
| RSSI Input Current Range | | | 1 | | 2000 | µA |
| RSSI Offset Current | | | | 50 | | nA |
| RSSI Offset Current Stability | | (Notes 3 and 12) | -120 | | +150 | nA |
| RSSI Gain Error | | (Note 3) | -4 | | +4 | % |
| **TX POWER MONITOR** | | | | | | |
| Tx Power Monitor Accuracy | | Average current into MDIN pin 50µA < $I_{MDIN\_AVG}$ < 2mA, excluding tracking error (Note 3) | -25 | | +25 | % |
| **BADC MONITOR** | | | | | | |
| Gain Error | | | -2 | | +2 | % |
| ADC Full Scale | | | | 1.164 | | V |
| ADC Resolution | | | | 12 | | bits |
| ADC LSB Size | | | | 284 | | µV |
| **SUPPLY VOLTAGE MONITOR ($V_{CCX}$, $V_{CCRO}$, and $V_{CCT}$)** | | | | | | |
| Supply Voltage Monitor Accuracy | | $V_{CCX}$ = $V_{CCRO}$ = $V_{CCT}$ > $V_{POR\_DE}$ | -2 | | +2 | % |
| ADC Resolution | | | | 12 | | bits |
| ADC LSb Size | | | | 1.137 | | mV |
| **TEMPERATURE SENSOR** | | | | | | |
| External Temperature Sensor Accuracy | | Measured with a single PNP device (Note 3) | -2 | | +2 | °C |
| **DIGITAL INPUTS (SDA, SCL, CSEL, DISABLE, RSEL)** | | | | | | |
| Minimum Input Voltage High | $V_{IH}$ | | | 1.6 | | V |
| Maximum Input Voltage High | $V_{IH}$ | | | $V_{CC}$ | | V |
| Minimum Input Voltage Low | $V_{IL}$ | | | 0 | | V |

## Electrical Characteristics (continued)

($V_{CCX}$ = $V_{CCRO}$ = $V_{CCT}$ = 2.85V to 3.47V, $V_{CCTO}$ = 2.97V to 3.47V, $V_{GND}$ = 0V, $T_A$ = -40°C to +95°C. Typical values are at $V_{CCX}$ = $V_{CCRO}$ = $V_{CCT}$ = $V_{CCTO}$ = 3.3V, 14Ω single-ended load for TOUTC/TOUTA, and $T_A$ = +25°C, unless otherwise noted. See Figure 1 for electrical setup.) (Note 2)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| Maximum Input Voltage Low | $V_{IL}$ | | | 0.8 | | V |
| Input Hysteresis | $V_{HYS}$ | | | 80 | | mV |
| Input Leakage Current High (SDA, DISABLE) | $I_{IH}$ | Input connected to $V_{CCRO}$ | -10 | | +10 | µA |
| Input Leakage Current High (SCL, CSEL, RSEL) | $I_{IH}$ | Input connected to $V_{CCRO}$, internal 75kΩ pulldown | 20 | 44 | 100 | µA |
| Input Leakage Current Low (SCL, CSEL, RSEL) | $I_{IL}$ | Input connected to GND | -10 | | +10 | µA |
| Input Leakage Current Low (SDA) | $I_{IL}$ | Input connected to GND, internal 75kΩ pullup | 20 | 44 | 100 | µA |
| Input Leakage Current Low (DISABLE) | $I_{IL}$ | Input connected to GND, internal 7.5kΩ pullup | 200 | 450 | 800 | µA |
| **DIGITAL OPEN-DRAIN OUTPUT (SDA, LOS, and FAULT) (Note 14)** | | | | | | |
| Output Low Voltage | $V_{OL}$ | External pullup is between 4.7kΩ and 10kΩ to $V_{CCRO}$ | | | 0.4 | V |
| Output High Voltage | $V_{OH}$ | External pullup is between 4.7kΩ and 10kΩ to $V_{CCRO}$ | $V_{CCRO}$ - 0.4 | $V_{CCRO}$ | | V |
| **DIGITAL CMOS OUTPUT (INTRPT, LOS, and FAULT) (Note 14)** | | | | | | |
| Output Low Voltage | $V_{OL}$ | $I_{OL}$ = 1mA | | | 0.4 | V |
| Output High Voltage | $V_{OH}$ | $I_{OH}$ = 1mA | $V_{CCRO}$ - 0.4 | | | V |
| **3-WIRE TIMING SPECIFICATIONS (Figure 3)** | | | | | | |
| Maximum SCL Clock Frequency | $f_{SCL}$ | | | 1000 | | kHz |
| Minimum SCL Pulse Width High | $t_{CH}$ | | | 500 | | ns |
| Minimum SCL Pulse Width Low | $t_{CL}$ | | | 500 | | ns |
| SDA Setup Time | $t_{DS}$ | | | 100 | | ns |
| SDA Hold Time | $t_{DH}$ | | | 100 | | ns |
| SCL Rise to SDA Propagation Time | $t_D$ | | | 12 | | ns |
| Minimum CSEL Pulse Width Low | $t_{CSW}$ | | | 500 | | ns |
| CSEL Leading Time Before the First SCL Edge | $t_L$ | | | 500 | | ns |
| CSEL Trailing Time After the Last SCL Edge | $t_T$ | | | 500 | | ns |

## Electrical Characteristics (continued)

($V_{CCX}$ = $V_{CCRO}$ = $V_{CCT}$ = 2.85V to 3.47V, $V_{CCTO}$ = 2.97V to 3.47V, $V_{GND}$ = 0V, $T_A$ = -40°C to +95°C. Typical values are at $V_{CCX}$ = $V_{CCRO}$ = $V_{CCT}$ = $V_{CCTO}$ = 3.3V, 14Ω single-ended load for TOUTC/TOUTA, and $T_A$ = +25°C, unless otherwise noted. See Figure 1 for electrical setup.) (Note 2)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| Maximum Capacitive Load SDA, SCL | $C_b$ | Total bus capacitance on one line with 4.7kΩ pullup from SDA to $V_{CC}$ | | 20 | | pF |
| **2-WIRE TIMING SPECIFICATIONS (Figure 5)** | | | | | | |
| Maximum SCL Clock Frequency | $f_{SCL}$ | | | 400 | | kHz |
| Minimum SCL Pulse Width High | $t_{CH}$ | | | 1.3 | | µs |
| Minimum SCL Pulse Width Low | $t_{CL}$ | | | 0.6 | | µs |
| Minimum Bus Free Time Between STOP and START Condition | $t_{BUF}$ | | | 1.3 | | µs |
| Minimum STOP Setup Time | $t_{SU\_STO}$ | | | 600 | | ns |
| Minimum START Setup Time | $t_{SU\_STA}$ | | | 600 | | ns |
| Minimum START Hold Time | $t_{HD\_STA}$ | | | 600 | | ns |
| Minimum SDA Setup Time | $t_{HD\_DAT}$ | | | 100 | | ns |
| Minimum SDA Hold Time | $t_{HD\_DAT}$ | Receive | | 0 | | ns |
| | | Transmit | | 300 | | |
| Minimum SCL and SDA Rise and Fall Time | $t_R$, $t_F$ | (Note 15) | | 20 + 0.1$C_b$ | | ns |
| Maximum Spike Pulse Width Suppressed by Input Filter | $t_{SP}$ | | | 50 | | ns |
| Maximum Capacitive Load SDA, SCL | $C_b$ | Total bus capacitance on one line | | 20 | | pF |

**Note 2:** Limits are 100% tested at $T_A$ = +25°C (and/or $T_A$ = +95°C). Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization.

**Note 3:** Guaranteed by design and characterization.

**Note 4:** A repeating $2^7$ PRBS + 72 zeros and $2^7$ PRBS (inverted) + 72 ones pattern is used. Deterministic jitter is defined as the arithmetic sum of pulse-width distortion (PWD) and pattern-dependent jitter (PDJ). Source DJ is removed from the measurement.

**Note 5:** $V_{RIN}$ is 30m$V_{P-P}$ to 1.2$V_{P-P}$ differential amplitude, SET_CML = 10d. Input data transition time 21ps (20% to 80%).

**Note 6:** LOS must not assert if the input data is invalid for less than 2.3µs. The LOS must assert, if the data is invalid for more than 80µs. The signal at the input will be switched between two amplitudes Signal_ON, and Signal_OFF.
1) Receiver operates at sensitivity level plus 1dB power penalty
       A) Signal_OFF = 0; Signal_ON = (+8dB) + 10log(min_assert_level)
       B) Signal_ON = (+1dB) + 10log(max_deassert_level); Signal_OFF = 0
2) Receiver operates at overload
       Signal_OFF = 0; Signal_ON = 1.2$V_{P-P}$.

**Note 7:** LOS hysteresis (10 × Log($V_{LOS-DEASSERT}$/$V_{LOS-ASSERT}$)dB) is designed to be > 1.25dB for SET_LOS[6:0] DAC code from 8d to 101d. LOS is characterized with a $2^{23}$-1 PRBS pattern for 11.3Gbps and a K28.5 pattern for 1.25Gbps operation

**Note 8:** Output of a TIA in case of loss of light, see Figure 7.

**Note 9:** $I_{LD\_DC}$ = $I_{DC}$ + 0.5 × $I_{MOD}$ × R/(50 + R), where $I_{LD\_DC}$ is the effective laser DC current, $I_{DC}$ is the DC DAC current, $I_{MOD}$ is the modulation DAC current, and R is the differential laser load resistance. Example: For R = 5Ω, $I_{LD\_DC}$ = $I_{DC}$ + 0.045 × $I_{MOD}$. The required compliance range for VOUT, while Tx output is enabled, is $V_{CCTO}$ - 1V to $V_{CCTO}$ - 2V.

## Electrical Characteristics (continued)

($V_{CCX}$ = $V_{CCRO}$ = $V_{CCT}$ = 2.85V to 3.47V, $V_{CCTO}$ = 2.97V to 3.47V, $V_{GND}$ = 0V, $T_A$ = -40°C to +95°C. Typical values are at $V_{CCX}$ = $V_{CCRO}$ = $V_{CCT}$ = $V_{CCTO}$ = 3.3V, 14Ω single-ended load for TOUTC/TOUTA, and $T_A$ = +25°C, unless otherwise noted. See Figure 1 for electrical setup.) (Note 2)

**Note 10:** $I_{LD\_MOD}$ = $I_{MOD}$ × 50/(50 + R), where $I_{LD\_MOD}$ is the effective laser modulation current, $I_{MOD}$ is the modulation DAC current, and R is the differential laser load resistance. Example: For R = 5Ω, $I_{LD\_MOD}$ = 0.91 × $I_{MOD}$.

**Note 11:** Stability is defined as [($I_{MEASURED}$) - ($I_{REFERENCE}$)]/($I_{REFERENCE}$) over the listed current/temperature range and $V_{CCT}$ = $V_{CCX}$ = $V_{CCRO}$ = $V_{CCREF}$ ±5%, $V_{CCREF}$ = 3.3V. Reference current measured at $V_{CCREF}$ and $T_{REF}$ = +25°C.

**Note 12:** Stability is defined as [($I_{MEASURED}$) - ($I_{REFERENCE}$)] over the listed temperature range and supply range. Reference current measured at $V_{CC}$ = 3.3V and $T_{REF}$ = +25°C.
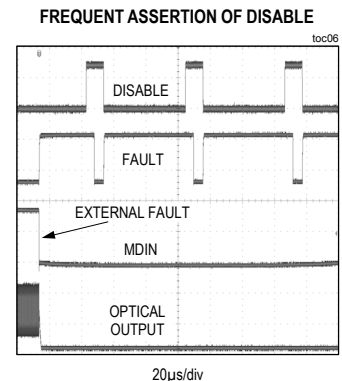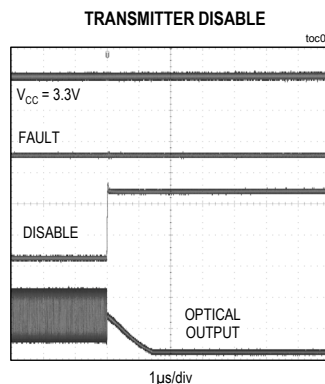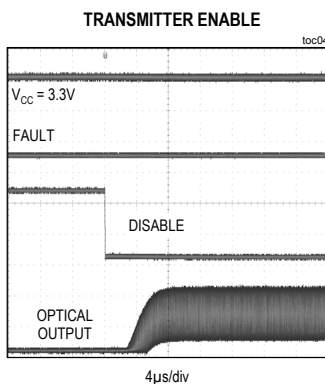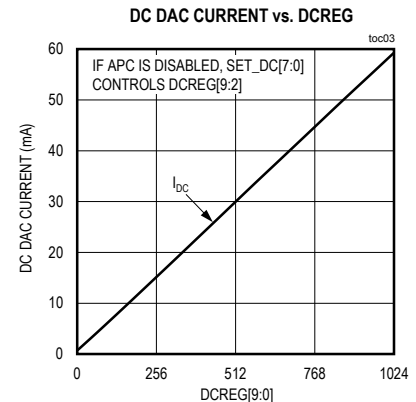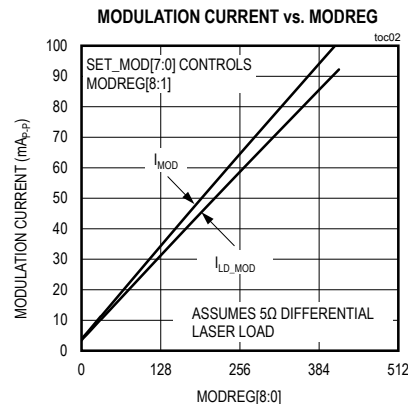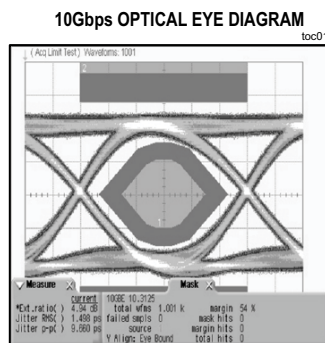
**Note 13:** Calibrated at room temperature by adjusting TSNS_INT_OFS[15:0] (TSNS_INT_SCL[15:0] unchanged from default value). In order to reduce the effect of self-heating the Rx and Tx circuitry are disabled. To minimize the reported error over the full temperature range, calibration is set such that the reported result is 2°C above ambient at room temperature. In the application, self-heating may introduce additional variation.

**Note 14:** For open-drain configuration FAULT_PU_EN = 0 and LOS_PU_EN = 0. For CMOS output configuration FAULT_PU_EN = 1 and LOS_PU_EN = 1.

**Note 15:** $C_b$ = total capacitance of one bus line in pF.
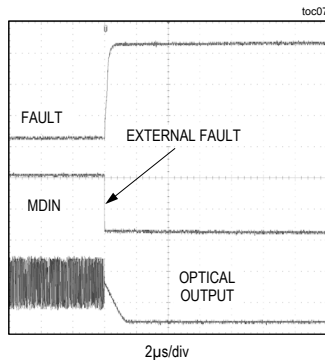
## Typical Operating Characteristics

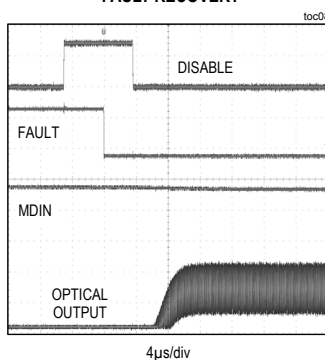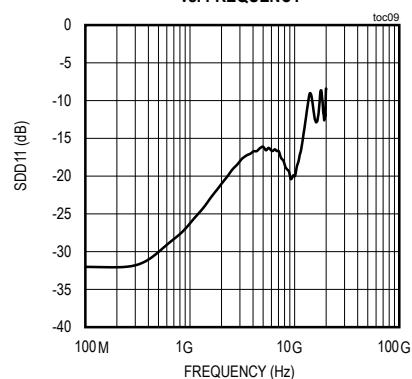($V_{CC}$ = 3.3V, $T_A$ = +25°C, data pattern $2^{31}$-1 PRBS, unless otherwise noted.)

**10Gbps OPTICAL EYE DIAGRAM**

**MODULATION CURRENT vs. MODREG**

**DC DAC CURRENT vs. DCREG**

**TRANSMITTER ENABLE**

**TRANSMITTER DISABLE**

**FREQUENT ASSERTION OF DISABLE**

## Typical Operating Characteristics (continued)

($V_{CC}$ = 3.3V, $T_A$ = +25°C, data pattern $2^{31}$-1 PRBS, unless otherwise noted.)

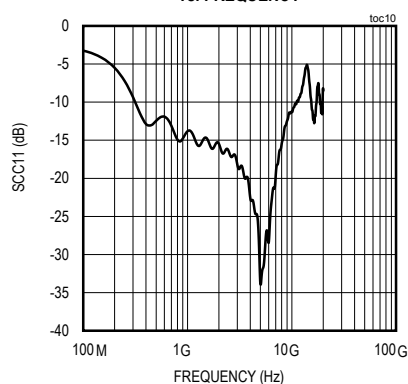**RESPONSE TO FAULT**

toc07

FAULT

EXTERNAL FAULT

MDIN

OPTICAL
OUTPUT

2µs/div

**FAULT RECOVERY**

toc08

DISABLE

FAULT

MDIN

OPTICAL
OUTPUT

4µs/div

**Tx INPUT DIFFERENTIAL RETURN LOSS
vs. FREQUENCY**

toc09

SDD11 (dB)

FREQUENCY (Hz)

**Tx INPUT COMMON-MODE RETURN LOSS
vs. FREQUENCY**

toc10

SCC11 (dB)

FREQUENCY (Hz)

**Tx OUTPUT DIFFERENTIAL RETURN LOSS
vs. FREQUENCY**

toc11

SDD22 (dB)

FREQUENCY (Hz)

**Tx OUTPUT COMMON-MODE RETURN LOSS
vs. FREQUENCY**

toc12

SCC22 (dB)

FREQUENCY (Hz)

**REPORTED $V_{CCTO}$, $V_{CCX}$, $V_{CCT}$ VOLTAGES
vs. FORCED SUPPLY VOLTAGE**

toc13

REPORTED VOLTAGES (V)

$V_{CCTO}$

$V_{CCX}$

$V_{CCT}$

FORCED SUPPLY VOLTAGE (V)

**REPORTED RSSI CURRENT
vs. FORCED RSSI INPUT CURRENT**

toc14

REPORTED RSSI CURRENT (mA)

FORCED RSSI INPUT CURRENT (mA)

**EXTERNAL TEMPERATURE SENSOR
ABSOLUTE ERROR**

toc15

BASED ON 30 PART CHARACTERIZATION

ABSOLUTE ERROR (°C)

3σ ERROR
BANDS

TEMPERATURE (°C)

# Typical Operating Characteristics (continued)

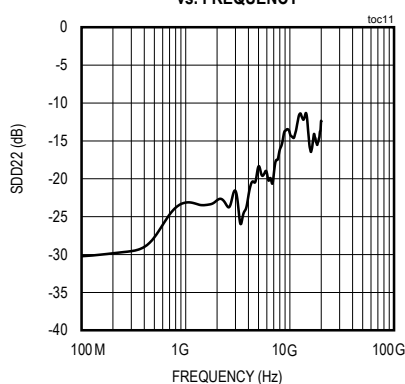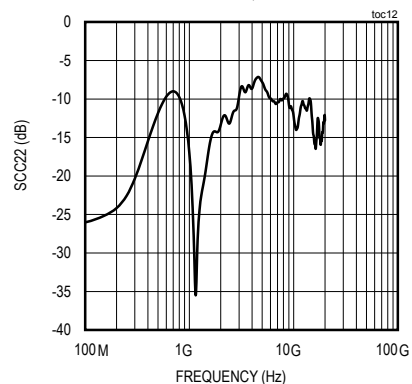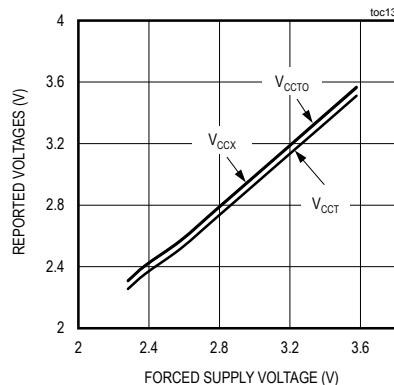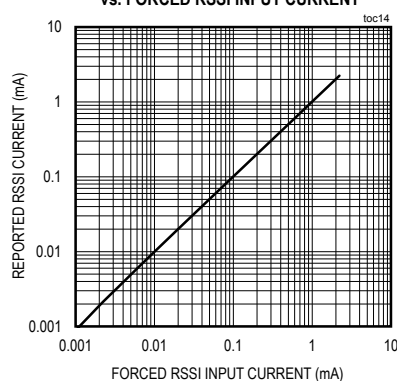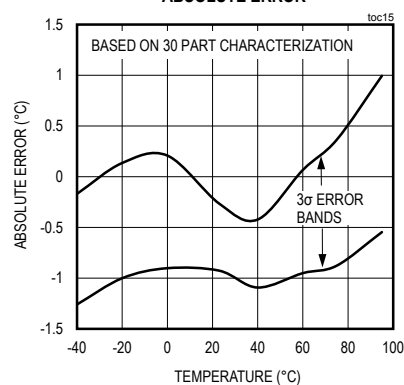($V_{CC}$ = 3.3V, $T_A$ = +25°C, data pattern $2^{31}$-1 PRBS, unless otherwise noted.)

**INTERNAL TEMPERATURE SENSOR ERROR (23°C CALIBRATION)**

toc16

3σ ERROR BANDS

ERROR (°C) vs TEMPERATURE (°C)

**REPORTED BADC VOLTAGE vs. FORCED BADC VOLTAGE**

toc17

REPORTED BADC VOLTAGE (V) vs FORCED BADC VOLTAGE (V)

**DIFFERENTIAL Rx OUTPUT AMPLITUDE vs. SET_CML DAC SETTING**

toc18

1111 0000 PATTERN

DE-EMPHASIS DISABLED

4dB DE-EMPHASIS
3dB DE-EMPHASIS
2dB DE-EMPHASIS
1dB DE-EMPHASIS

DIFFERENTIAL Rx OUTPUT AMPLITUDE (mV$_{P-P}$) vs SET_CML[4:0]

**Rx INPUT-BASED LOS THRESHOLD vs. SET_LOS**

toc19

DEASSERT

ASSERT

DIFFERENTIAL INPUT AMPLITUDE (mV$_{P-P}$) vs SET_LOS[6:0]

**RX BER vs. DIFFERENTIAL INPUT AMPLITUDE (10.3Gbps)**

toc20

BER vs INPUT AMPLITUDE (mV$_{P-P}$)

**Rx OUTPUT (INPUT: 1.0625Gbps, 30mV$_{P-P}$, $2^7$-1 PRBS)**

toc21

RATE_SEL + RSEL = 0, SET_RXBW = 00 (1GHz)

80mV/div

140ps/div

# Typical Operating Characteristics (continued)

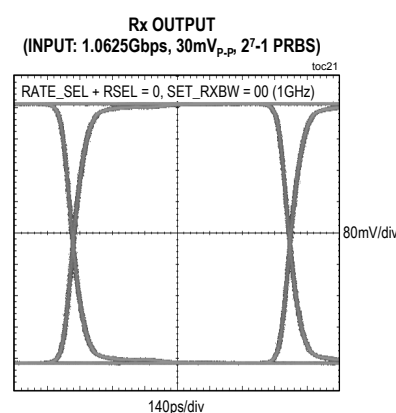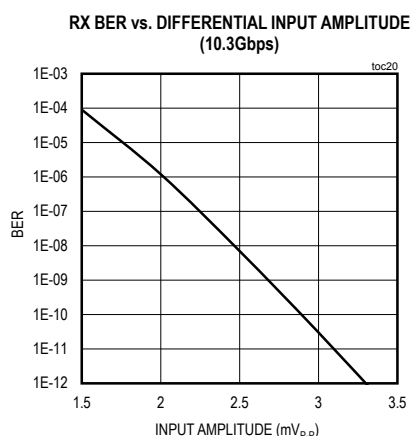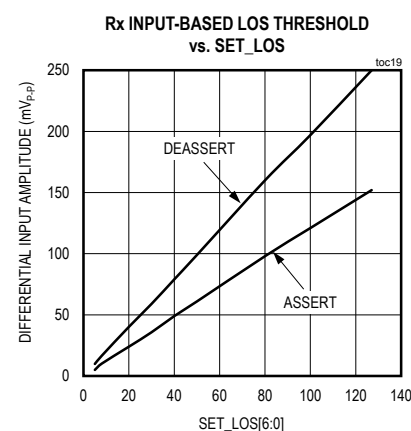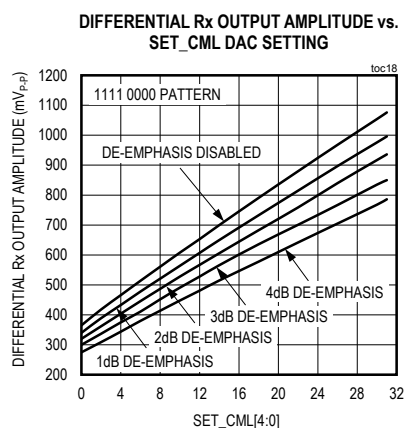($V_{CC}$ = 3.3V, $T_A$ = +25°C, data pattern $2^{31}$-1 PRBS, unless otherwise noted.)

**Rx OUTPUT**
**(INPUT: 4.25Gbps, 30mV$_{P-P}$, $2^7$-1 PRBS)**

toc22

RATE_SET + RSEL = 0, SET_RXBW = 11 (3GHz)

80mV/div

35ps/div

**Rx OUTPUT**
**(INPUT: 10.3Gbps, 30mV$_{P-P}$, $2^{31}$-1 PRBS)**

toc23

RATE_SET + RSEL = 1, SET_RXBW = 01 (10GHz)

80mV/div

15ps/div

**Rx OUTPUT**
**(INPUT: 10.3Gbps, 1200mV$_{P-P}$, $2^{31}$-1 PRBS)**

toc24

RATE_SEL + RSEL = 1, SET_RXBW = 01 (10GHz)

80mV/div

15ps/div

**Rx OUTPUT THROUGH 4.6dB CHANNEL LOSS**
**AT 5GHz, 11.3Gbps, NO DEEMPHASIS**

toc25

80mV/div

13ps/div

**Rx OUTPUT THROUGH 4.6dB CHANNEL LOSS**
**AT 5GHz, 11.3Gbps, DEEMPHASIS = 4dB**

toc26

80mV/div

13ps/div

**POR (P3VFLAG) ASSERT/DE-ASSERT**
**vs. TEMPERATURE**

toc27

DE-ASSERT

ASSERT

$V_{CCX}$, $V_{CCT}$ (V)

TEMPERATURE (°C)

# 11.3Gbps Transceiver with DDM and DC-Coupled Laser Interface

## Pin Configuration

TOP VIEW

MAX3956

TQFN
5mm x 5mm

Pins (top): 24 RSSI, 23 TSNS, 22 TGND, 21 VOUT, 20 TOUTC, 19 TOUTA, 18 V$_{CCTO}$, 17 MDIN

Pins (left): 25 BADC, 26 I.C., 27 V$_{CCX}$, 28 RIN-, 29 RIN+, 30 V$_{CCX}$, 31 RSEL, 32 LOS

Pins (right): 16 I.C., 15 V$_{CCT}$, 14 TIN-, 13 TIN+, 12 I.C., 11 REGFILT, 10 SDA, 9 SCL

Pins (bottom): 1 INTRPT, 2 FAULT, 3 DISABLE, 4 V$_{CCRO}$, 5 ROUT+, 6 ROUT-, 7 V$_{CCRO}$, 8 CSEL

## Pin Description

| PIN | NAME | FUNCTION | EQUIVALENT CIRCUIT |
|-----|------|----------|--------------------|
| 1 | INTRPT | Interrupt Output, CMOS. Programmable interrupt signal. | MAX3956 V$_{CCRO}$ — INTRPT — ESD PROTECTION |

## Pin Description (continued)

| PIN | NAME | FUNCTION | EQUIVALENT CIRCUIT |
|---|---|---|---|
| 2 | FAULT | Transmitter Fault, Open-Drain Output. A logic-high indicates a fault condition has been detected. It remains high even after the fault condition has been removed. A logic-low occurs when the fault condition has been removed and the fault latch has been cleared by the DISABLE signal. Connect FAULT to host $V_{CC}$ via a 4.7kΩ to 10kΩ resistor. FAULT can also be configured as a CMOS output requiring no external resistor by setting the FAULT_PU_EN bit high. | |
| 3 | DISABLE | Transmitter Disable, LVTTL/CMOS input. Set to logic-low for normal operation. Logic-high or open disables both the modulation and DC current. Internally pulled up by a 7.5kΩ resistor to $V_{CCRO}$. | |
| 4, 7 | $V_{CCRO}$ | Power Supply. Provides supply voltage to the transceiver digital core and the Rx output circuitry. | — |
| 5 | ROUT+ | Differential Receiver Data Output, CML. This output has 50Ω terminations to $V_{CCRO}$. Polarity is set by the RX_POL bit. | |
| 6 | ROUT- | | |

## Pin Description (continued)

| PIN | NAME | FUNCTION | EQUIVALENT CIRCUIT |
|-----|------|----------|--------------------|
| 8 | CSEL | Chip-Select Input, CMOS. Used for 3-Wire communication. Setting CSEL to logic-high starts a cycle. Setting CSEL to logic-low ends the cycle and resets the control state machine. Internally pulled to ground by a 75kΩ resistor. Set low if using 2-wire communication. |  |
| 9 | SCL | Serial-Clock Input, CMOS. Internally pulled to ground by a 75kΩ resistor. |  |
| 10 | SDA | Serial-Data Bidirectional I/O, CMOS. Open-drain output. This pin has a 75kΩ internal pullup, but it requires an external 4.7kΩ to 10kΩ pullup to meet 3-wire timing specifications. |  |

## Pin Description (continued)

| PIN | NAME | FUNCTION | EQUIVALENT CIRCUIT |
|---|---|---|---|
| 11 | REGFILT | Internal Filter Node. Requires 0.1µF decoupling capacitor to ground. | — |
| 12, 16, 26 | I.C. | Internal Connection. Leave unconnected. | — |
| 13 | TIN+ | Differential Transmitter Data Input. The polarity is set by the TX_POL bit. | |
| 14 | TIN- | | |
| 15 | $V_{CCT}$ | Power Supply. Provides supply voltage to the transmitter core. | — |
| 17 | MDIN | Monitor Diode Input. Connect this pin to the cathode of the monitor diode. For transmitter power monitoring MDIN needs to be connected even for open-loop operation. External filtering on this pin should be optimized for each TOSA configuration. The Thevenin equivalent input of this pin is 40Ω to $V_{CCT}$ - 1.25V. | — |

## Pin Description (continued)

| PIN | NAME | FUNCTION | EQUIVALENT CIRCUIT |
|-----|------|----------|--------------------|
| 18 | $V_{CCTO}$ | Power Supply. Provides power to the transmitter output and laser TOSA. | |
| 19 | TOUTA | Inverting Modulator Current Output with 25Ω back-termination. Connect to laser anode through 25Ω transmission line. | |
| 20 | TOUTC | Noninverting Modulator Current Output with 25Ω back-termination. Connect to laser cathode through 25Ω transmission line. | |
| 21 | $V_{OUT}$ | Combined laser cathode current return path and sinking laser DC current output. | |
| 22 | TGND | Connect to an external temperature sensor (cathode). | |
| 23 | TSNS | Connect to an external temperature sensor (anode). | |

## Pin Description (continued)

| PIN | NAME | FUNCTION | EQUIVALENT CIRCUIT |
|---|---|---|---|
| 24 | RSSI | Current input to main ADC for receive-signal-strength-indication (RSSI). The voltage at this pin is regulated internally to 1.62V. |  |
| 25 | BADC | Auxiliary ADC Input (≈ 1.16V full scale) | — |
| 27, 30 | V$_{CCX}$ | Power Supply. Provides supply voltage to the receiver core. | — |
| 28 | RIN- | Differential Receiver Data Input. Contains 50Ω terminations on-chip. Connect these inputs to the TIA outputs using coupling capacitors. |  |
| 29 | RIN+ | | |

## Pin Description (continued)

| PIN | NAME | FUNCTION | EQUIVALENT CIRCUIT |
|-----|------|----------|--------------------|
| 31 | RSEL | Rate Select, CMOS Input. Internally pulled to ground by a 75kΩ resistor. Pin is internally OR'ed with RATE_SEL bit. The output of the OR sets the Rx circuitry path to 10G for logic 1, 4G for logic 0. |  |
| 32 | LOS | Receiver Loss-of-Signal (LOS) Output, Open Drain. This output goes to a logic-high when the level of the input signal drops below the SET_LOS register threshold. Polarity is set by LOS_POL register. The LOS circuitry can be disabled by setting LOS_EN = 0. Pull this pin to Host $V_{CC}$ via a 4.7kΩ to 10kΩ resistor. LOS can also be configured as a CMOS output requiring no external resistor by setting the LOS_PU_EN bit high. |  |
| — | EP | Exposed Pad. Ground. This is the only electrical connection to ground and must be soldered to circuit board ground for proper thermal and electrical performance (see the *Exposed-Pad Package and Thermal Considerations* section). | — |
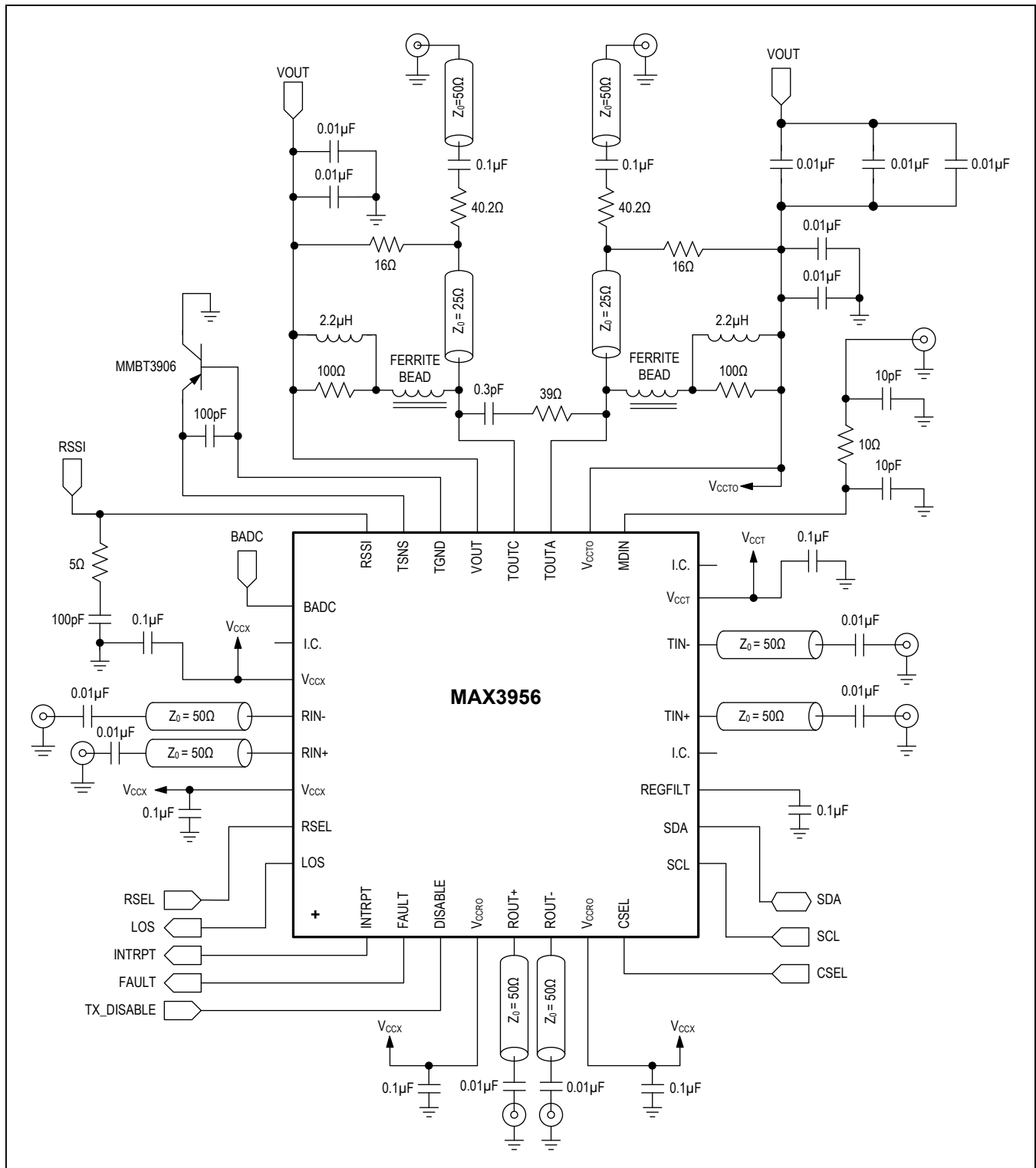
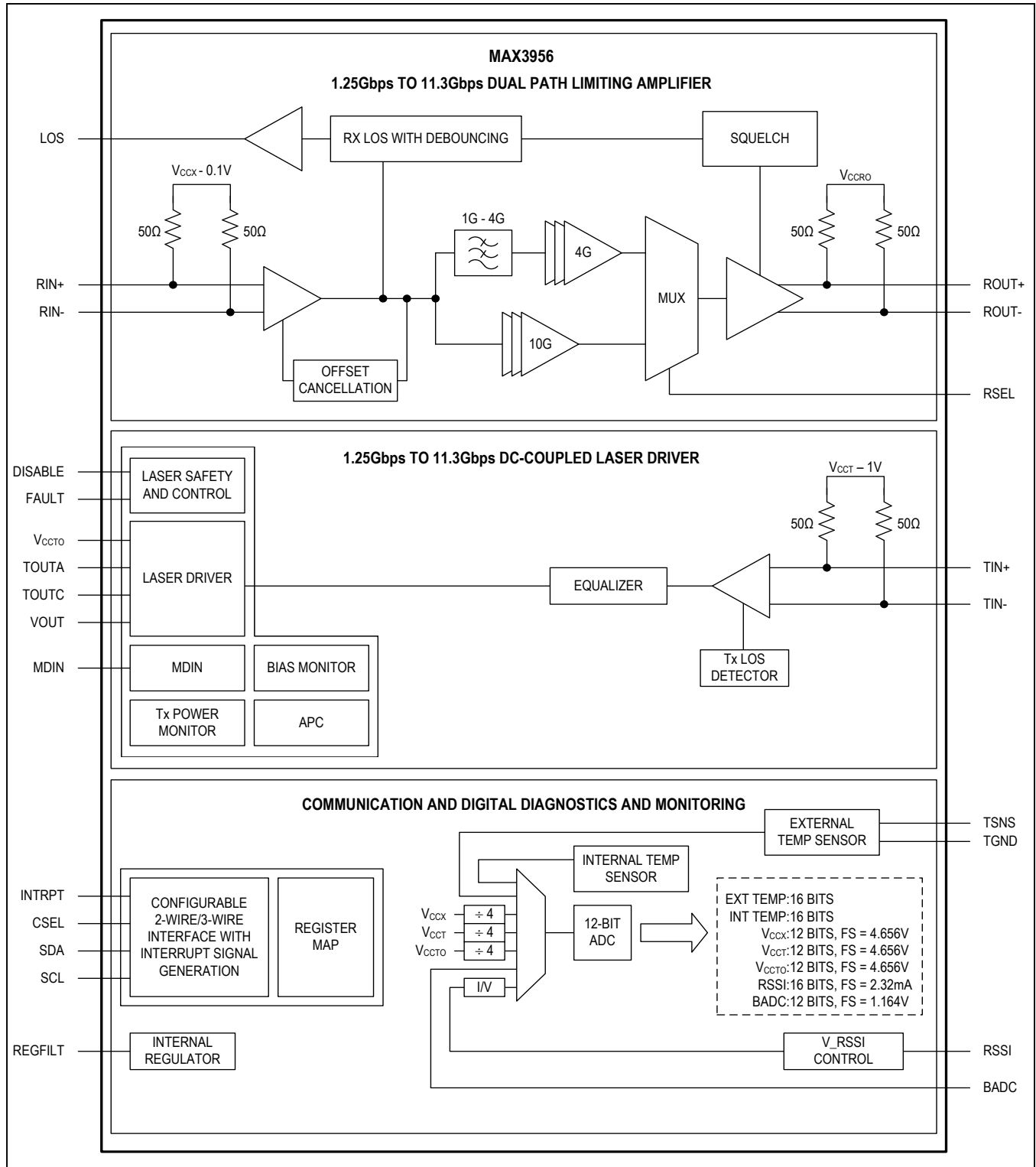*Figure 1. AC Electrical Test Schematic*

*Figure 2. Functional Diagram*

# Detailed Description

The MAX3956 combines a high-gain limiting amplifier, laser driver, and digital diagnostics monitoring (DDM). The limiting amplifier includes offset cancellation, programmable signal detect threshold, selectable bandwidth, and deemphasis. The laser driver includes automatic power-control (APC), laser current and power measurement capability, overcurrent limiting, and fault detection. A serial control interface enables an external controller to set all parameters necessary for operation and read all monitors and status indicators. The interface accepts either 2-wire or 3-wire protocol.

The features and performance are specifically designed to be compatible with low-cost microcontrollers to provide complete SFF-8472 functionality, including laser fault detection, diagnostics, and automatic power control. The MAX3956 includes all the logic required for laser protection, control loop operation, and monitor diode (MD) current measurement.

## 1.25Gbps to 11.3Gbps Limiting Amplifier Block Description

### Limiting Amplifier

The limiting amplifier consists of a multistage-multipath amplifier, offset-correction circuit, loss-of-signal circuit, and output buffer. Its low noise and high gain optimize optical performance. Configuration options (LOS threshold, LOS polarity, output amplitude, output deemphasis, and data polarity) enhance layout flexibility and ROSA compatibility.

### High-Speed Input Signal Path

The inputs, RIN±, have an internal 100Ω differential termination and should be AC-coupled to the transimpedance amplifier.

### Offset Cancellation

The offset cancellation loop compensates for pulse-width distortion at RIN± and internal offsets. The default small-signal low-frequency cutoff of the offset cancellation loop is 10kHz when AZ_BW[1:0] is set to 01.

### Loss-of-Signal Circuitry (LOS)

The loss-of-signal circuitry detects the amplitude of the incoming signal and compares it against a programmable threshold, which is controlled by SET_LOS[6:0]. The range of LOS assert is 10mV$_{P-P}$ to 121mV$_{P-P}$. Changing the LOS threshold during operation (i.e., without executing a reset) does not cause a glitch or incorrect LOS output. The detector has 2dB of hysteresis to control chatter

at the LOS output. The LOS output polarity is controlled by the LOS_POL bit. The entire LOS circuit block can be disabled by setting LOS_EN = 0.

### Output Drivers

The ROUT± outputs are terminated with 50Ω to V$_{CCRO}$. The differential output level can be programmed between 400mV$_{P-P}$ and 1000mV$_{P-P}$ by the SET_CML[4:0], and the output polarity can be inverted. The output can be disabled to its common-mode voltage either manually or automatically by an LOS condition (squelch through the SQ_EN bit).

Deemphasis may be enabled to compensate for FR4 losses with a 10Gbps signal. If enabled, settings of 1dB, 2dB, 3dB, and 4dB deemphasis are available.

## 1.25Gbps to 11.3Gbps Laser Driver Block Description

The laser driver consists of a high-speed differential input buffer, selectable input equalizer, polarity switch buffer, laser modulator and DC current generator, monitor diode input buffer with adjustable gain, APC loop circuitry, eye-safety monitors, and DISABLE pin.

### Differential High-Speed Input Buffer with Programmable Equalization

The TIN± inputs are internally biased and have a 100Ω differential termination. The first amplifier stage features a programmable equalizer, controlled by TX_EQ, to compensate for high-frequency losses including the SFP connector. The TX_POL bit controls the signal path polarity. An active AC input signal is indicated by TIN_LOS.

### Laser Modulator and DC Generator

The laser modulator provides DC-coupled current into the cathode of the laser diode at the TOUTC pin. The modulation current amplitude is set by MODREG[8:0]. The modulation current DAC guarantees modulation amplitudes up to 85mA. The instantaneous compliance voltage for TOUTC is 0.6V to V$_{CCTO}$ - 1V and for TOUTA is V$_{CCTO}$ ±1V.

The VOUT pin sinks DC current from the laser's cathode. The amplitude of the laser DC current is controlled by DCREG[9:0]. The laser DC current DAC guarantees values up to 57mA.

### Monitor Diode Current Input Buffer

The MDIN input stage has adjustable gain settings, allowing a large input signal range. The MDIN_GAIN[2:0] bits set the transimpedance gain from 156Ω to 2496Ω in one octave steps.

### Automatic Power Control Circuitry (APC)

The MAX3956 contains circuitry to maintain constant optical power using feedback from the monitor diode. The SET_APC register in conjuction with MDIN_GAIN controls the set point for average laser power when APC operation is enabled.

### DDM

Digital diagnostics and monitoring is provided on the MAX3956. This includes internal and external temperature monitoring, Tx DC current reporting, Tx average current reporting, Tx output power reporting, RSSI, and internal supply voltage monitoring. The MAX3956, when combined with a digital-only µC, will provide compliance with SFF-8472 (Diagnostic Monitoring Interface for Optical Transceivers).

### 3-Wire Interface

The MAX3956 implements a proprietary 3-wire digital slave interface. The 3-wire interface consists of an SDA bidirectional data line, an SCL clock signal input, and a CSEL chip-select input (active high). The external master initiates a data transfer by asserting the CSEL pin then generating a clock signal. All data transfers are most significant bit (MSb) first. See Figure 3 for more information.

### Protocol

Each single register operation consists of 16-bit transfers (15-bit address/data, 1-bit RWN). The bus master generates 16 clock cycles to SCL. All operations transfer 8 bits

to the MAX3956; the RWN bit determines if the cycle is read or write. See Table 1.

### Write Mode (RWN = 0)

Writing to a register requires two transactions: a write of 12h to the MODECTRL register to enter SETUP mode, followed by a write to the target address. For each transaction, the master generates 16 clock cycles at SCL. It outputs a total of 16 bits (MSb first) to the SDA line at the falling edge of the clock. The master closes the transmission by setting CSEL to 0. Figure 3 shows the 3-wire interface timing.

### Read Mode (RWN = 1)

The master generates 16 clock cycles at SCL in total. The master outputs a total of 8 bits (MSb first) to the SDA line at the falling edge of the clock. The SDA line is released after the RWN bit has been transmitted. The slave outputs 8 bits of data (MSb first) at the rising edge of the clock. The master closes the transmission by setting CSEL to 0. Figure 3 shows the 3-wire interface timing.

### Table 1. 3-Wire Digital Communication Word Structure

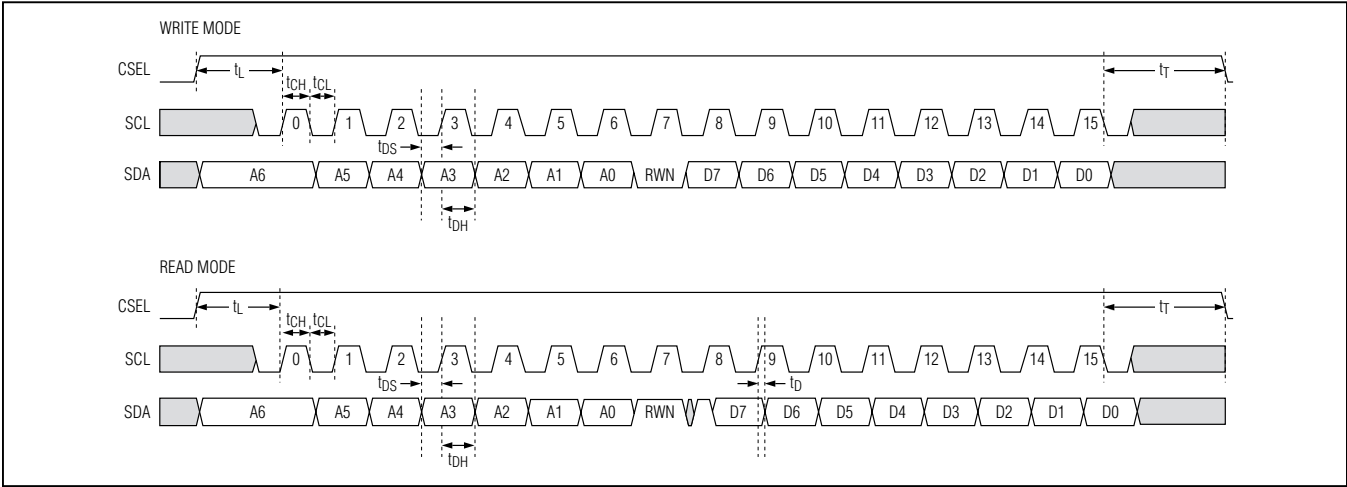| BIT | NAME | DESCRIPTION |
|------|------|-------------|
| 15:9 | Address | 7-Bit Internal Register Address |
| 8 | RWN | 0: Write; 1: Read |
| 7:0 | Data | 8-Bit Read or Write Data |



Figure 3. 3-Wire Digital Interface Timing Diagram

## Table 2. Block Write Examples

| BLOCK WRITE MODE 1 (STARTS AT ADDRESS H0x01) | BLOCK WRITE MODE 2 (STARTS AT ANY ADDRESS) |
|---|---|
| Master sets CSEL to 1 | Master sets CSEL to 1 |
| ADDR H0x00 + RWN = 0 | ADDR H0x00 + RWN = 0 |
| Data 81h (page 0 access) – or Data 55h (page 1 access) | Data 81h (page 0 access) – or Data 55h (page 1 access) |
| Master sets CSEL to 0 | Master sets CSEL to 0 |
| Master sets CSEL to 1 | Master sets CSEL to 1 |
| ADDR H0x00 + RWN = 0 | ADDR H0x00 + RWN = 0 |
| Data 12h (setup mode) | Data 12h (setup mode) |
| Data 1 (ADDR H0x01) | Master sets CSEL to 0 |
| Data 2 (ADDR H0x02) | Master sets CSEL to 1 |
| Data 3 (ADDR H0x03) | ADDR H0x0N + RWN = 0 |
| … | Data 1 (ADDR H0x0N) |
| Data j (ADDR H0xj) | Data 2 (ADDR H0x0N + 1) |
| Master sets CSEL to 0 | Data 3 (ADDR H0x0N + 2) |
| — | … |
| — | Data i (ADDR H0xN + i - 1) |
| — | Master sets CSEL to 0 |

## Table 3. MODECTRL Register Settings

| CODE (hex) | CONDITION |
|---|---|
| 00 | NORMAL mode |
| 12 | SETUP mode |
| 55 | SELECT PAGE 1 mode |
| 68 | FAULT CLEAR mode |
| 81 | SELECT PAGE 0 mode |

**Block Write Mode (RWN = 0)**

The two different block write modes of operation are described in Table 2.

**Block Read Mode (RWN = 1)**

The master initiates the block read mode by accessing any register address and setting the RWN bit to 1. The block read mode starts by stretching the CSEL interval beyond the 16 clock cycles, and it is exited automatically when the master has set CSEL to 0.
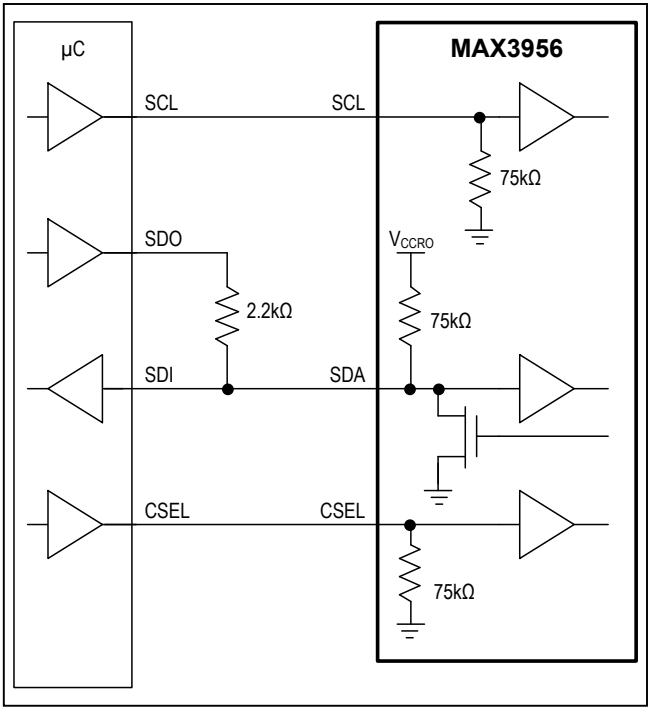


*Figure 4. Recommended 3-Wire Implementation Using a Generic Microcontroller*

**Mode Control**

The MAX3956 contains more than 128 registers, which exceeds the addressability of a 7-bit number. So it has two pages (Page 0 and Page 1) that contain all the registers. To write to or read from either page, the page must first be selected by writing to the MODECTRL register: 81h to access page 0, 55h to access page 1. Once a page has been selected any further writes or reads will access that page until the MODECTRL is written to the new page. The default page upon POR is page 1.

Setup mode allows the master to write data into any register except the status registers and read-only registers. To enter the setup mode, 12h is written to the MODECTRL register. The next operation is unrestricted to any writable register. The setup mode is automatically exited after the next operation is finished. This sequence must be repeated if further register writes are necessary.

To speed up the laser control by a factor of 2, the MODINC, DCINC, and APCINC registers can be updated without writing SETUP mode to MODECTRL.

Fault-clear mode allows the clearing of the fault latch, and restarts operation of the device. It is activated by writing 68h to the MODECTRL register.

## 2-Wire Communication

### 2-Wire Definition

The following terminology is commonly used to describe 2-Wire data transfers.

**Master Device:** The master device controls the slave devices on the bus. The master device generates SCL clock pulses and START and STOP conditions.

**Slave Devices:** Slave devices send and receive data at the master's request.

**Bus Idle or Not Busy**: Time between STOP and START conditions when both SDA and SCL are inactive and in their logic-high states.

**START Condition:** A START condition is generated by the master to initiate a new data transfer with a slave. Transitioning SDA from high to low, while SCL remains high, generates a START condition. See Figure 5 for applicable timing.

**STOP Condition:** A STOP condition is generated by the master to end a data transfer with a slave. Transitioning SDA from low to high, while SCL remains high, generates a STOP condition. See Figure 5 for applicable timing.

**Repeated START Condition:** The master can use a repeated START condition at the end of one data transfer to indicate that it will immediately initiate a new data transfer following the current one. Repeated STARTs are commonly used during read operations to identify a specific register address to begin a data transfer. A repeated START condition is issued identically to a normal START condition. See Figure 5 for applicable timing.

**Bit Write:** Transitions of SDA must occur during the low state of SCL. The data on SDA must remain valid and unchanged during the entire high pulse of SCL plus the setup and hold time requirements (Figure 5). Data is shifted into the device during the rising edge of the SCL.

**Bit Read:** At the end a write operation, the master must release the SDA bus line for the proper amount of setup time before the next rising edge of SCL during a bit read. The device shifts out each bit of data on SDA at the falling edge of the previous SCL pulse and the data bit is valid at the rising edge of the current SCL pulse. Remember that the master generates all SCL clock pulses, including when it is reading bits from the slave.

**Acknowledgement (ACK and NACK):** An acknowledgement (ACK) or not-acknowledge (NACK) is always the 9th bit transmitted during a byte transfer. The device receiving data (the master during a read or the slave during a write operation) performs an ACK by transmitting a zero during the 9th bit. A device performs a NACK by transmitting a one during the 9th bit. Timing for the ACK and NACK is identical to all other bit writes (Figure 5). An ACK is the acknowledgment that the device is properly receiving data. A NACK is used to terminate a read sequence or as an indication that the device is not receiving data.

**Byte Write:** A byte write consists of 8 bits of information transferred from the master to the slave (most significant bit first) plus a 1-bit acknowledgement from the slave to the master. The 8 bits transmitted by the master are done according to the bit write definition and the acknowledgement is read using the bit read definition.
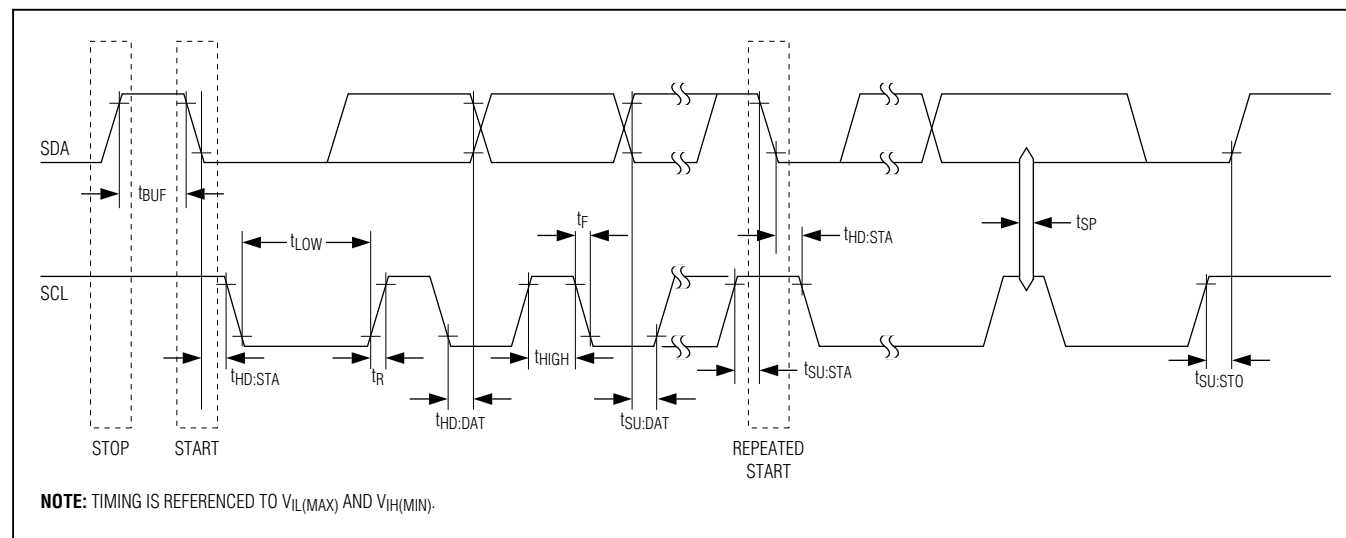


Figure 5. 2-Wire Timing Diagram

**Byte Read:** A byte read is an 8-bit information transfer from the slave to the master plus a 1-bit ACK or NACK from the master to the slave. The 8 bits of information that are transferred (most significant bit first) from the slave to the master are read by the master using the bit read definition, and the master transmits an ACK using the bit write definition to receive additional data bytes. The master must NACK the last byte read to terminate communication so the slave returns control of SDA to the master.

**Slave Address Byte:** Each slave on the 2-wire bus responds to a slave address byte sent immediately following a START condition. The slave address byte contains the slave address in the most significant 7 bits and the R/$\overline{W}$ bit in the least significant bit. The MAX3956 responds to the slave address 46h.

The part contains more than 128 registers, which exceeds the addressability of a 7-bit number. So it has two pages (page 0 and page 1) that contain the registers. To write to or read from either page, the page must first be selected by writing to the MODECTRL register: 81h to access page 0, 55h to access page 1. Once a page has been selected any further writes or reads will access that page until MODECTRL is written with a new page. The default page upon POR is page 1.

**2-Wire Protocol**

See Figure 6 for an example of 2-wire timing.

**Writing a Single Byte to the MAX3956:** The master must generate a START condition, write the slave address byte, write R/$\overline{W}$ = 0, write the MODECTRL address, write 12h (Setup), and generate a STOP condition. This prepares the MAX3956 for a write. Then the master must generate a START condition, write the slave address byte, write R/$\overline{W}$ = 0, write the register address, write the byte of data, and generate a STOP condition. Remember that the master must read the slave's acknowledgement during all byte write operations.
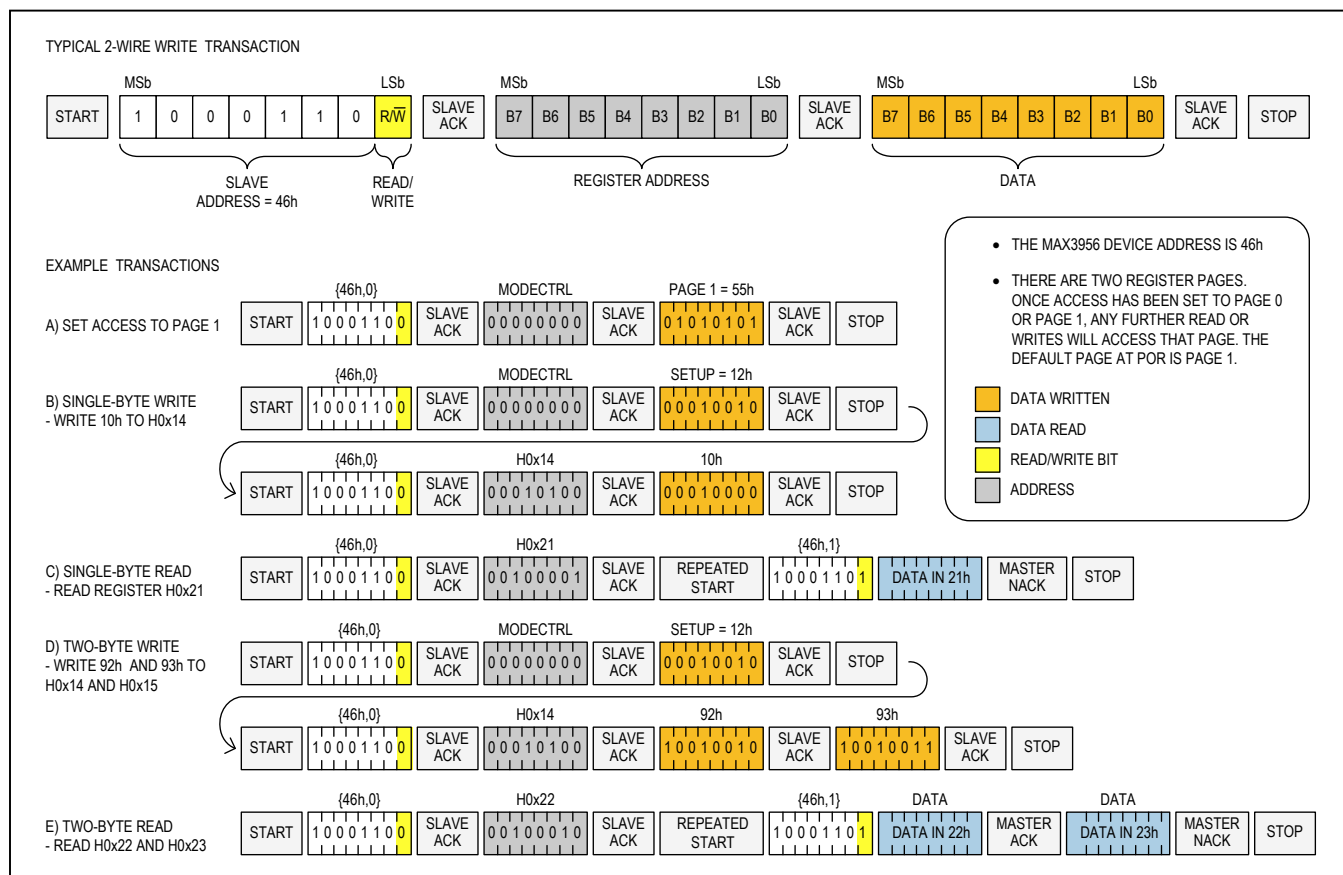


*Figure 6. Example 2-Wire Timing*

**Writing Multiple Bytes to the MAX3956:** To write multiple bytes to a slave, the master must generate a START condition, write the slave address byte, write R/$\overline{W}$ = 0, write the MODECTRL address, write 12h (Setup), and generate a STOP condition. Then the master must generate a START condition, write the slave address byte, write R/$\overline{W}$ = 0, write the register address, write multiple data bytes, and generate a STOP condition. The device writes multiple bytes with this second write transaction. This is internally controlled by an address counter that allows data to be written to consecutive addresses without transmitting a register address before each data byte is sent. The address counter limits the write to one page.

For example: A 3-byte write starts at address 06h and writes three data bytes (11h, 22h, and 33h) to three consecutive addresses. The result is that addresses H0x06, H0x07, H0x08 would contain 11h and 22h, and 33h respectively.

The APCINC, MODINC, and DCINC registers are the only registers in the device that do not require 12h (Setup) to be written to MODECTRL before writing to these registers. This allows quicker adjustments of these registers.

**Writing to the APCINC, MODINC, or DCINC register**: The master must generate a START condition, write the slave address byte, write R/$\overline{W}$ = 0, write the address, write the byte of data, and generate a STOP condi-

tion. Remember that the master must read the slave's acknowledgement during all byte write operations.

## Design Procedure

### Load Factory Calibration Constants

Upon power-up, after POR has deasserted, the microcontroller must load the individually programmed calibration constants into the calibration registers. This is accomplished by five write commands shown below:

WRITE: 55h to H0x00

WRITE: 34h to H0x00

WRITE: 01h to H0x7A

WRITE: 34h to H0x00

WRITE: 03h to H0x7A

### Power-On-Reset (POR)

A power-on-reset circuit provides proper startup sequencing and ensures that the laser is off while the supply voltage is ramping or below a specified threshold (≈ 2.55V). The serial interface can also be used to command a manual reset at any time by setting SOFT_RESET = 1, which is identical to a power-on reset. When using SOFT_RESET, the MAX3956 transmitter must first be disabled, either by the DISABLE pin, by setting TX_EN = 0, or by setting XCVR_EN = 0. Either power-on or SOFT_RESET requires approximately 150µs to complete. POR sets all
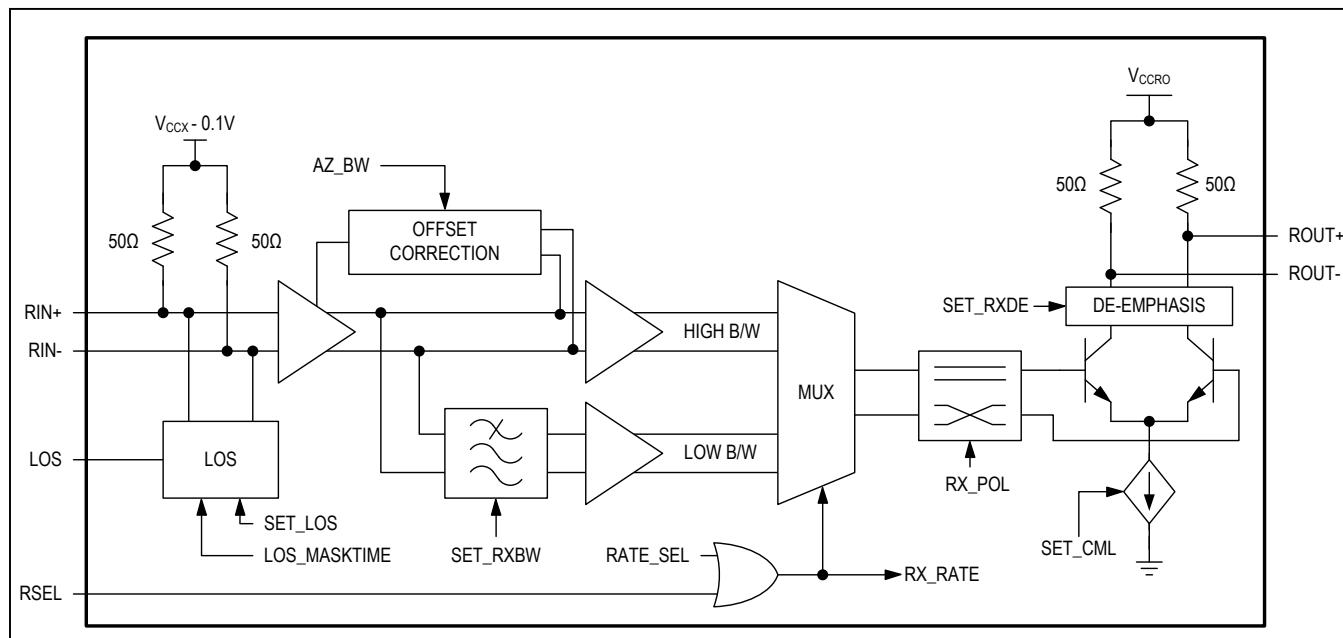


*Figure 7. Limiting Amplifier Block Diagram*

registers to their defaults. The recommended POR proce-
dure is as follows:

- Because the POR is routed to both the FAULT and
INTRPT pins, the µC should monitor one of these for
POR detection in the case of a power-supply brown-
out issue.

- If FAULT is used by the µC to detect a MAX3956
POR event, a pullup resistor should be used on this
pin. This is because FAULT defaults to open drain
upon POR.

- Upon POR event detection, the controller initiates
2-wire or 3-wire communication with MAX3956 by
repeatedly reading out the TOPSTAT register until
the 1-to-0 transition occurs for both PORD and
P3VFLAG.

- Once the POR flags have cleared, repeatedly read
the TXSTAT1 register until the Tx status flags have
cleared. Write a fault clear (68h) to the MODECTRL
register to clear any startup related faults.

- Controller writes commands to load calibration con-
stants into calibration registers then writes/initializes
all applicable registers.

## 1.25Gbps to 11.3Gbps Receiver Details

Figure 7 is a block diagram of the MAX3956 receiver cir-
cuitry. It includes the offset-correction block, LOS block,
high-bandwidth/low-bandwidth paths, input and output
stages, and output deemphasis.

### Offset-Correction Circuitry

The offset-correction circuitry is provided to remove PWD
at RIN± and offsets caused by intrinsic mismatch within
the amplifier stages. The bandwidth of the offset-correc-
tion loop is adjustable and is set by AZ_BW[1:0]. Table 4
shows the small-signal cutoff frequency for each setting.

### LOS Circuitry

The LOS block detects the differential amplitude of the
input signal and compares it against a preset threshold
controlled by the 7-bit SET_LOS register. The LOS assert
threshold is approximately $1.2mV_{P-P} \times$ SET_LOS[6:0].
The LOS deassert level is approximately 1.6 times the
assert level to avoid LOS chatter. The recommended
minimum setting is SET_LOS[6:0] = 8d.

### LOS Output Masking

The LOS output masking feature masks false input sig-
nals that can occur after a loss-of-light event in a fiberop-
tic link. These false input signals, caused by some tran-
simpedance amplifier implementations, can corrupt the
LOS output and cause system-level link diagnostic errors.

The LOS output masking time can be programmed from
0 to 4.6ms in 36µs steps using the LOS_MASKTIME[6:0]
register. The output mask timer is initiated on the first
"0" to "1" LOS signal transition and prevents any further
changes in the LOS output signal until the end of the
programmed LOS timing period. The LOS output mask-
ing time should be carefully chosen to extend beyond any
expected input glitch. See Figure 8.

## Table 4. Offset-Correction Loop Cutoff Frequency

| AZ_BW[1:0] | CUTOFF FREQUENCY (kHz) |
|---|---|
| 00 | 5 |
| 01 | 10 (default) |
| 10 | 20 |
| 11 | 40 |
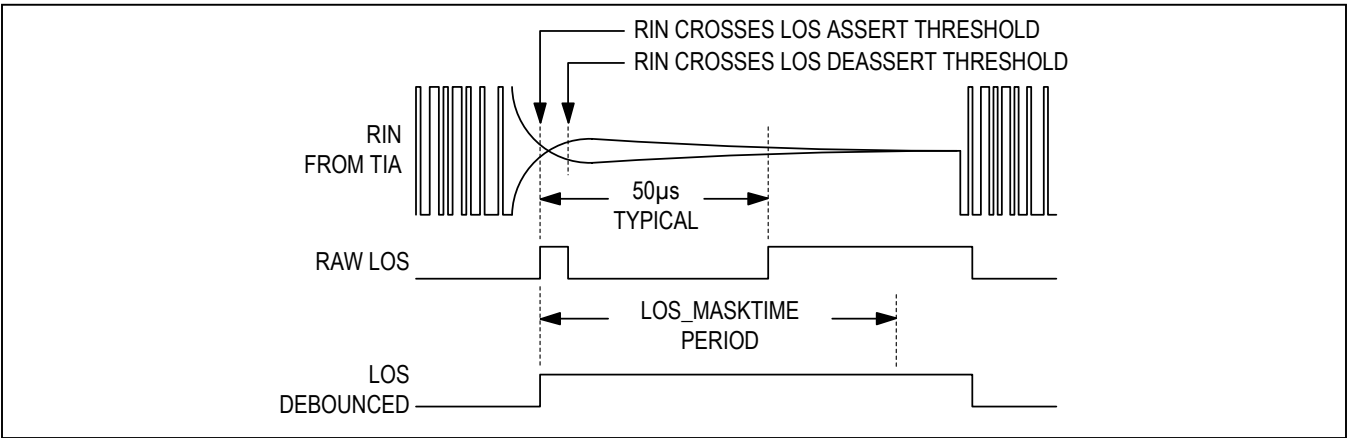


Figure 8. LOS Output Masking
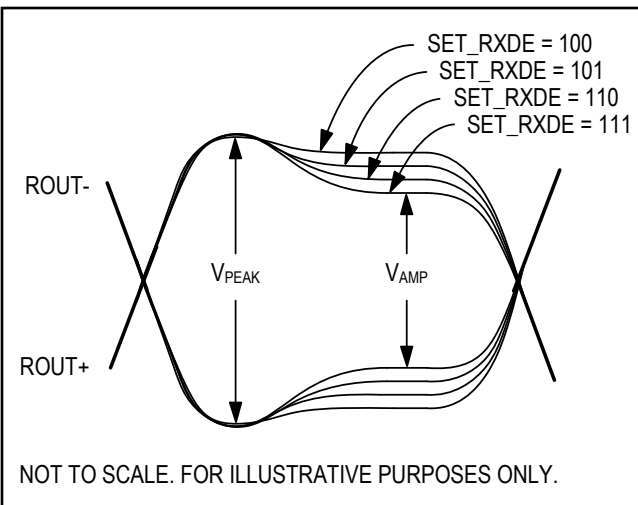
*Figure 9. Deemphasis Effect on ROUT Signal*

## Receiver Path Selection and Bandwidth Modes

Table 5 shows the settings for the receiver paths and bandwidth selection modes.

## Rx Output Stage

The CML output is optimized for a differential 100Ω load and can be squelched to its common-mode voltage manually or by the internal LOS status. Table 6 shows the output modes for various conditions/settings.

Deemphasis is included to compensate for FR4 loss at 10Gbps and is set by the SET_RXDE[2:0] bits. Figure 9 illustrates the effects of deemphasis on the output waveform.

## Table 5. Receiver Path Selection and -3dB Bandwidth Setting Modes

| RSEL + RATE_SEL | SET_RXBW[1:0] | OUTPUT OPERATION MODE DESCRIPTION |
|---|---|---|
| 0 | 00 | Low-bandwidth Rx path with small-signal bandwidth of ≈ 1GHz |
| 0 | 01 | Low-bandwidth Rx path with small-signal bandwidth of ≈ 2GHz |
| 0 | 10 | Low-bandwidth Rx path with small-signal bandwidth of ≈ 2.5GHz |
| 0 | 11 | Low-bandwidth Rx path with small-signal bandwidth of ≈ 3GHz |
| 1 | xx | High-bandwidth Rx path |

## Table 6. ROUT Enable/Disable Mode

| XCVR_EN | RX_EN | RX_OUT_EN | SQ_EN | OUTPUT OPERATION MODE DESCRIPTION |
|---|---|---|---|---|
| 0 | X | X | X | Disabled, to $V_{CCRO}$ |
| 1 | 0 | X | X | Disabled, to $V_{CCRO}$ |
| 1 | 1 | 0 | X | Output squelched, to common-mode |
| 1 | 1 | 1 | 0 | Enabled |
| 1 | 1 | 1 | 1 | Squelch mode controlled by LOS |

## Table 7. ROUT Amplitude Range and Resolution (Typical, RSEL + RATE_SEL = 1)

| SET_RXDE[2:0] | DIFFERENTIAL OUTPUT AMPLITUDE (mV$_{P-P}$), V$_{AMP}$ in Figure 9 | |
|---|---|---|
| | SET_CML[4:0] = 12d | SET_CML[4:0] = 31d |
| 0xx | 650 | 1080 |
| 100 | 610 | 1000 |
| 101 | 570 | 940 |
| 110 | 530 | 850 |
| 111 | 480 | 790 |

## 1.25Gbps to 11.3Gbps Laser Driver

The MAX3956 contains a DC-coupled laser driver designed to drive 5Ω to 10Ω TOSAs from 1.25Gbps to 11.3Gbps. It contains an input buffer with programmable equalization, DC current and modulation current DACs, output driver, and eye safety circuitry. A 2-wire or 3-wire digital interface is used to control these functions.

## Programmable Input Equalization

When operating at 10Gbps, connector and FR4 losses can be significant enough to increase jitter. To compensate for these losses the MAX3956 has adjustable input equalization as shown in Table 8. When TX_EQ ≠ 00, the equalizer has an optimized range of 190mV$_{P-P}$ to 700mV$_{P-P}$ differential at TIN±.

## Laser DC Current DAC

The DC current from the MAX3956 is optimized to provide up to 57mA of DC current into a 5Ω to 10Ω laser load with 58.5µA resolution. The current is controlled through the 2-wire or 3-wire interface using the APC loop or by open-loop control. While the transmitter is enabled, the compliance voltage at VOUT is $V_{CCTO}$ - 1V to $V_{CCTO}$ - 2V.

Effective DC current seen by the laser ($I_{BIAS}$) is actually the combination of the DC DAC current generated by the DCREG register ($I_{DC}$), MODREG register ($I_{MOD}$) and laser load (R). It is calculated by the formula:

$$I_{DC} \equiv DC\ DAC\ Current$$
$$I_{DC} = (DCREG[9:0] + 12) \times 58.5µA$$
$$I_{LD\_DC} = I_{DC} + 0.5 \times I_{MOD} \times R/(50 + R)$$
$$I_{BIAS} = I_{LD\_DC} + I_{LD\_MOD}/2$$

If the written value of DCREG[9:2] exceeds DCMAX[7:0], the DC_OVFL warning flag is set and DCREG[9:2] remains unchanged. If an attempt is made to set the DCREG to be less than 0, an underflow warning bit, DC_UDFL will flag.

## APC Operation

The automatic power control loop (APC) automatically adjusts DC laser current to maintain constant average current at the MDIN pin. The desired average current at the MDIN pin is set by the SET_APC register in conjunction with the MDIN_GAIN value. The MAX3956 measures the high peak and low peak of the MDIN current which represent the P1 and P0 levels of the optical power. These levels are held in the MD1REG and MD0REG registers respectively. The APC loop will increase/decrease DC laser current to make the following equation true:

$$SET\_APC[7:0] = MD1REG[15:8] + MD0REG[15:8]$$

When the APC loop is closed, the average MDIN current will be related to SET_APC and MDIN_GAIN by the following equation:

$$I_{MDIN\_AVG} = SET\_APC[7:0] \times 1.22mV/MDIN\_GAIN$$

The largest step size the APC circuitry can apply to DCREG[9:0] is determined by DCINC[4:0]. So if DCINC = 1 then the APC can only increase or decrease DCREG[9:0] by 1 LSb per loop calculation. If DCINC[4:0] = 0, then the APC loop is frozen.

## Flowchart for Setting Up APC Operation

Figure 10 explains the procedure for setting up APC operation on the MAX3956 and Figure 11 shows the optical power for each step in the flowchart process.

## Open Loop Control of DC Laser Current

To control the DC DAC current manually (not using the APC loop), the APC_EN bit must be set to 0. DCREG controls the DC DAC current. DCREG cannot be directly written to but can be adjusted by writing to DCINC or SET_DC (if IBUPDT_EN=1). Setting IBUPDT_EN = 1 allows writes to SET_DC[7:0] to automatically transfer to DCREG[9:2]. The 2 LSb (bits 1 and 0) of DCREG are initialized to zero after POR and can be updated using the DCINC register. The DCMAX register limits the maximum DCREG[9:2] DAC code.

After initialization, the value of the DCREG register should be updated using the DCINC register. This optimizes cycle time and enhances laser safety.  The DCINC[4:0] contains increment information in two's complement notation. Increment values range from -16 to +15 LSbs.

## Laser Modulation Current DAC

The modulation current from the MAX3956 is optimized to provide up to 85mA of modulation current into a 5Ω laser load with 234µA resolution. The modulation current is controlled through the 2-wire/3-wire digital interface using the SET_DC, MODMAX, and MODINC. Effective modulation current seen by the laser is actually the combination

## Table. 8 Tx Input Equalization Control

| TX_EQ | BOOST AT 5.1GHz (dB) |
|-------|----------------------|
| 00    | 1.5                  |
| 01    | 3                    |
| 10    | 4.5                  |
| 11    | 5.5                  |
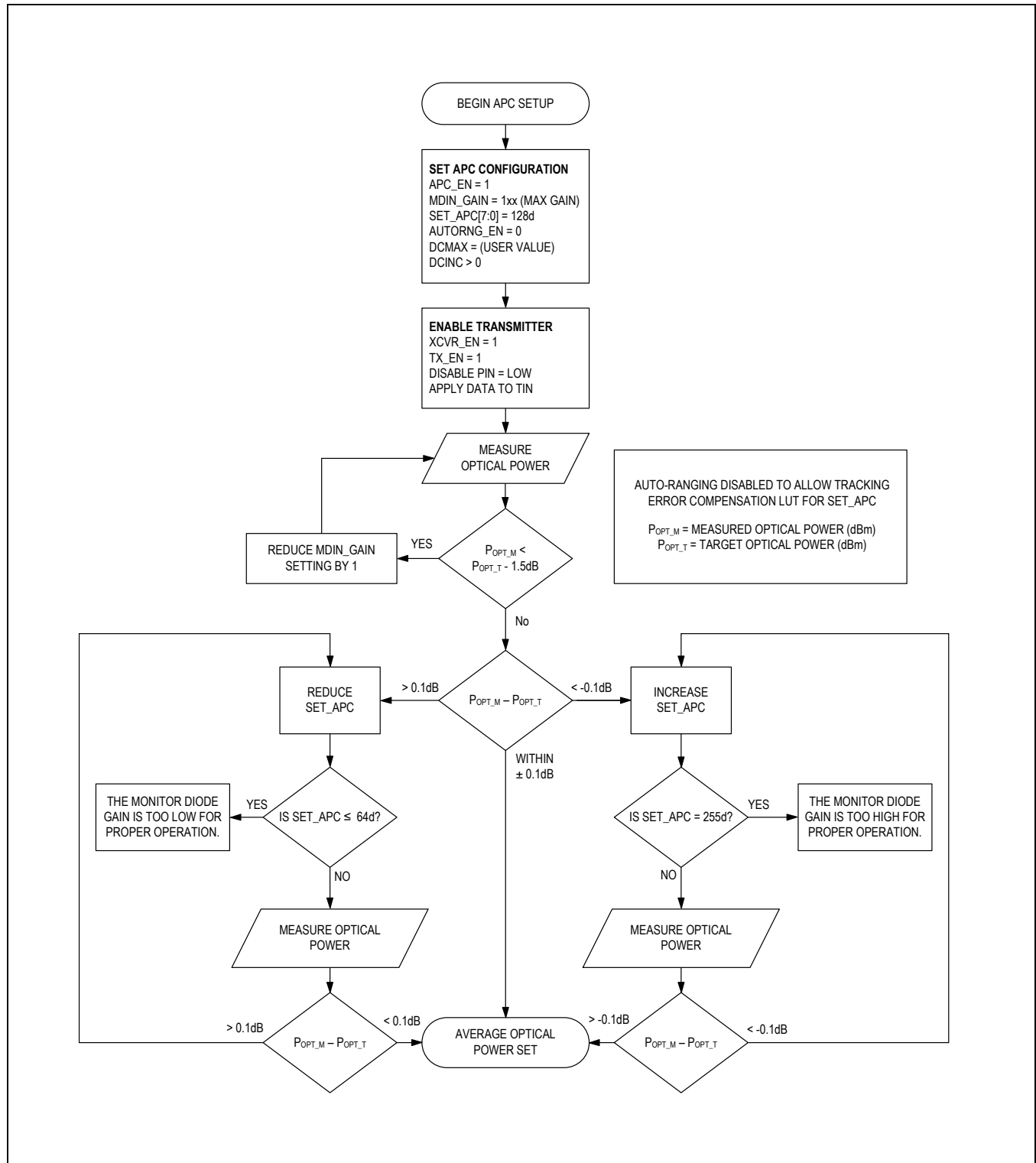
Figure 10. APC Setup Flowchart
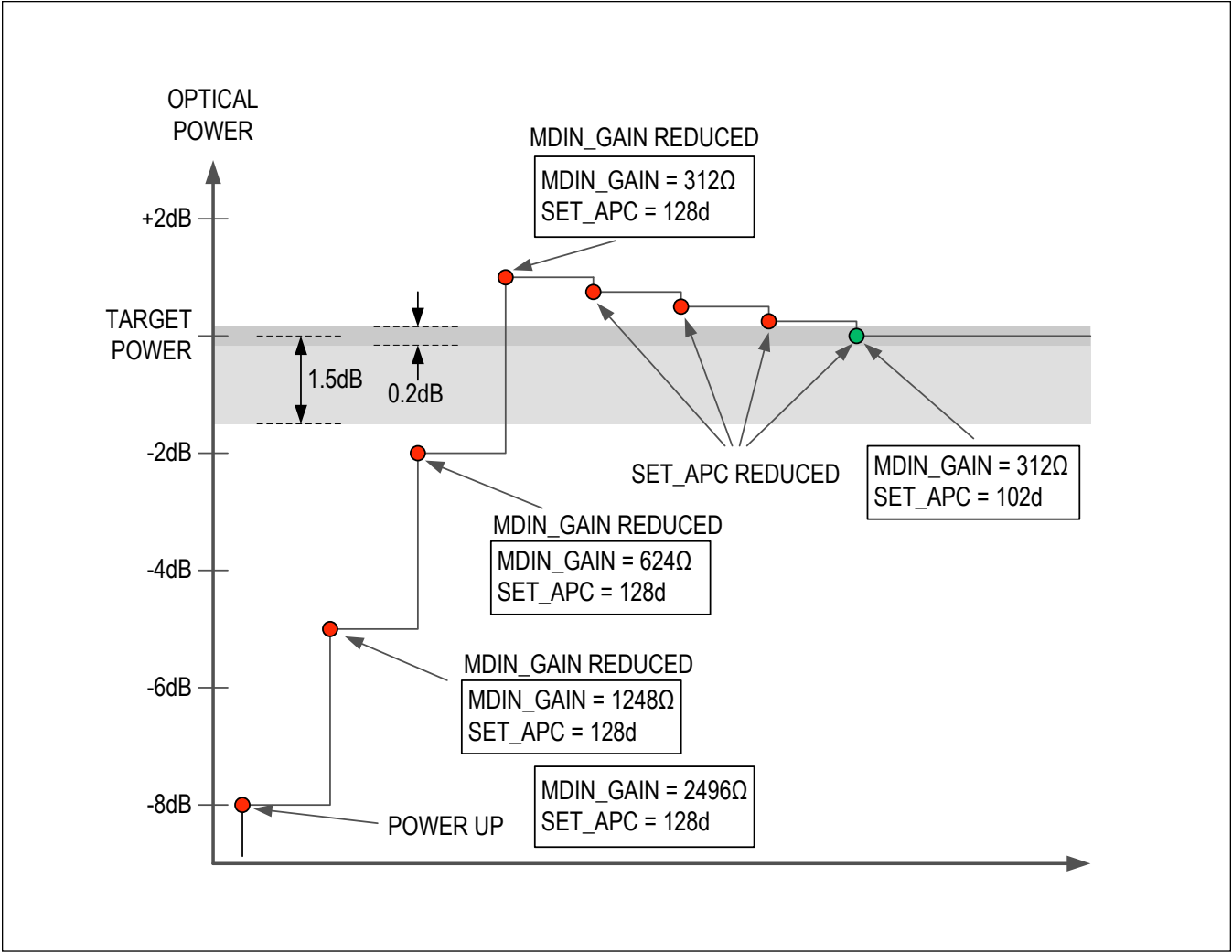
*Figure 11. Example of Optical Power During APC Setup*

of the DAC current generated by the SET_MOD register ($I_{MOD}$) and laser load (R). It is calculated by the formula:

$$I_{MOD} \equiv \text{MOD DAC Current}$$

$$I_{MOD} = (\text{SET\_MOD[8:0]} + 16) \times 234\mu A$$

$$I_{LD\_MOD} = I_{MOD} \times 50\Omega/(R_{LASER} + 50\Omega)$$

## Control of Laser Modulation Current DAC

MODREG controls the modulation DAC current and cannot be written to directly, but it can be adjusted by writing to MODINC or SET_MOD (if IMUPDT_EN=1). Setting IMUPDT_EN = 1 allows writes to SET_MOD[7:0] to automatically transfer to MODREG[8:1]. The LSb of MODREG is initialized to zero after POR and can be updated using the MODINC register. The MODMAX register limits the maximum MODREG[8:1] DAC code.

## MODINC Usage

After initialization the value of the SET_MOD DAC register should be updated using the MODINC register to optimize cycle time and enhance laser safety. The MODINC register is an 8-bit register where the first 5 bits contain the increment information in two's complement notation. Increment values range from -16 to +15 LSbs. If the updated value of SET_MOD[8:1] exceeds MODMAX[7:0], the MOD_OVFL warning flag is set and SET_MOD[8:1] remains unchanged. If an attempt is made to set the overall modulation DAC code to be less than 0 by using a combination of SET_MOD register and MODINC register it will cause an underflow warning bit MOD_UDFL.

## Eye Safety and Output Control Circuitry

There are several fault indicators associated with certain pins on the MAX3956, see Figure 13. If the voltage at the pin can cause an eye safety concern, then a fault is created and the TX output can be shut off. There is also a status indicator bit associated with each kind of fault condition. The MAX3956 has the capability to keep the transmitter active even if there is a fault condition by masking that fault condition. The status register bits will always flag a fault condition even if the actual fault is masked. When the fault is masked the FAULT pin voltage remains low even when there is a fault condition.

## DDM

The MAX3956 integrates the monitoring functions required to implement an SFP system, and when combined with a simple digital-only μC the system can comply with the SFF-8472 MSA. It may be desirable for the μC to implement averaging of the DDM results. Table 10 indicates the ADC registers related to DDM.

## Transceiver Temperature

The MAX3956 reports both the internal die temperature as well as the external board temperature (requires discrete pnp for sensing). Either may be used to support DDM reporting, however the internal die temperature is subject to self-heating. Programmable scale and offset factors allow the user to fine-tune the reported results. Figure 14 shows how the scale and offset are applied to the raw temperature data. The MAX3956 reporting format is consistent with the SFF-8472 reporting requirements.
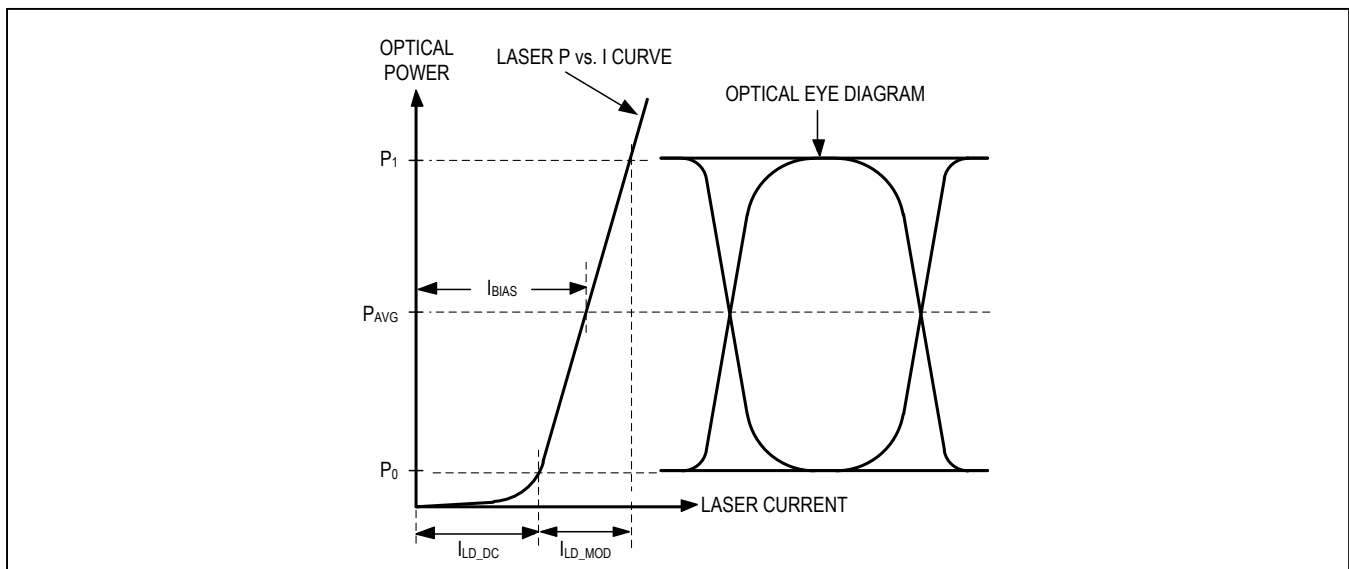


*Figure 12. Laser Current Graph*
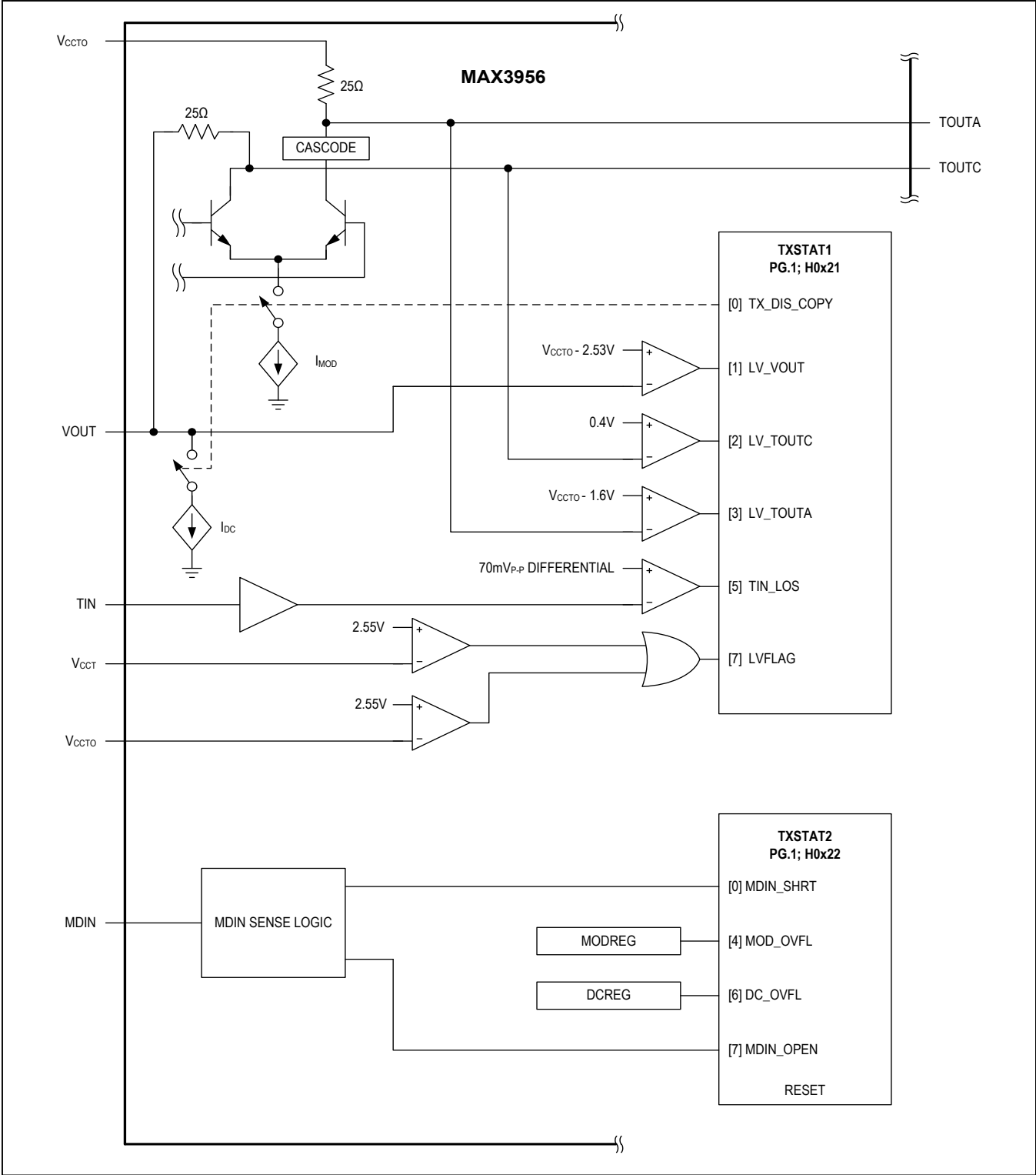
Figure 13. Eye Safety Circuitry

## Table 9. Circuit Response to Single-Point Faults

| PIN | NAME | SHORT TO Vcc | SHORT TO GND | OPEN |
|---|---|---|---|---|
| 1 | INTRPT | No effect (Note 12) | No effect (Note 12) | No effect (Note 12) |
| 2 | FAULT | No effect (Note 12) | No effect (Note 12) | No effect (Note 12) |
| 3 | DISABLE | Tx output is off if DIS_POL = 1 (default). No effect if DIS_POL = 0 | No effect if DIS_POL = 1 (default). Tx output is off if DIS_POL = 0 | Tx output is off if DIS_POL = 1 (default). No effect if DIS_POL = 0 |
| 4, 7 | $V_{CCRO}$ | No effect | Board supply collapsed (Note 3) | No effect (Note 15) |
| 5 | ROUT+ | No effect (Note 12) | No effect (Note 12) | No effect (Note 12) |
| 6 | ROUT- | No effect (Note 12) | No effect (Note 12) | No effect (Note 12) |
| 8 | CSEL | No effect (Note 12) | No effect (Note 12) | No effect (Note 12) |
| 9 | SCL | No effect (Note 12) | No effect (Note 12) | No effect (Note 12) |
| 10 | SDA | No effect (Note 12) | No effect (Note 12) | No effect (Note 12) |
| 11 | REGFILT | POR on | Disabled | No effect (Note 12) |
| 12, 16, 26 | I.C. | No effect | No effect | No effect |
| 13 | TIN+ | No effect depending on TIN- amplitude (Note 16) | No effect depending on TIN- amplitude (Note 16) | No effect depending on TIN- amplitude (Note 16) |
| 14 | TIN- | No effect depending on TIN+ amplitude (Note 16) | No effect depending on TIN+ amplitude (Note 16) | No effect depending on TIN+ amplitude (Note 16) |
| 15 | $V_{CCT}$ | No effect | Board supply collapsed (Note 3) | POR on |
| 17 | MDIN | No effect (Note 16) | No effect (Note 16) | No effect (Note 16) |
| 18 | $V_{CCTO}$ | No effect | LVFLAG flag asserted, laser diode is off (Note 16) | LVFLAG flag asserted, laser diode is off (Note 16) |
| 19 | TOUTA | No effect | Disabled (Note 16) | Laser modulation current is reduced or disabled (Note 16) |
| 20 | TOUTC | Laser diode is off | Disabled (Note 16) | Laser modulation current is reduced or disable (Note 16) |
| 21 | VOUT | $I_{DC}$ is on, but not delivered to laser; no fault. | Disabled (Note 16) | Disabled (Note 16) |
| 22 | TGND | No effect | No effect | No effect |
| 23 | TSNS | No effect | No effect | No effect |
| 24 | RSSI | No effect | No effect | No effect |
| 25 | BADC | No effect | No effect | No effect |
| 27, 30 | $V_{CCX}$ | No effect | Board supply collapsed (Note 14) | No effect (Note 15) |
| 28 | RIN- | No effect | No effect | No effect |
| 29 | RIN+ | No effect | No effect | No effect |
| 31 | RSEL | No effect | No effect | No effect |
| 32 | LOS | No effect | No effect | No effect |
| — | EP | Board supply collapsed (Note 14) | No effect | POR on |

**Note 12:** Normal operation—does not affect the laser power.
**Note 13:** Pin functionality might be affected, which could affect laser power/performance.
**Note 14:** Supply-shorted current is assumed to be primarily on the circuit board (outside this device) and the main supply is collapsed by the short.
**Note 15:** Redundant path. Normal in functionality but performance could be affected.
**Note 16:** Depending on mask settings this condition can create a fault and shut down the Tx output. Default mask settings used for Table 9.
**Warning:** Shorted to $V_{CC}$ or shorted to ground on some pins can violate the *Absolute Maximum Ratings*.

The external temperature may be measured using a discrete PN junction. The MMBT3906 pnp transistor is recommended. For measuring temperatures above +85°C, the BF550 pnp transistor is recommended. During normal operation a current is sourced from the TSNS pin and TGND is internally shorted to ground, so that the base-emitter voltage of the PNP transistor can be measured and the temperature calculated (see Figure 15). The MAX3956 automatically removes the effect of parasitic resistance in series with the sense diode, allowing flexibility in the placement of the diode.

**Internally Measured Supply Voltage**

The MAX3956 reports the voltages of the $V_{CCX}$, $V_{CCT}$, and $V_{CCTO}$ pins. The result from the MAX3956 is not formatted per SFF-8472 requirements, so the µC must format the data.

The supply voltage results are 12 bits, with a full-scale range of 4.656V. SFF-8472 specifies that the supply voltage be reported as a 16-bit number with LSb = 100µV, so the result of the MAX3956 must be scaled by 1.137mV/100µV = 11.37 in the µC.

**Tx DC Current**

The transmit DC value, DDM_TXRPT[11:0], is a calculation based on the laser DC current and the laser modulation current. Due to the laser and external tuning network, a small portion of the modulation adds to the DC current. It is shown as $I_{LD\_DC}$ in Figure 12. This value is located in the DDM_TXRPT[11:0] register (when DDM_TXRPT_SEL is set to 0) and is calculated as:

Tx DC Current = DDM_TXRPT[11:0] = $I_{DC}$ + $I_{MOD}$/12.8

where:

$$I_{DC} = (DCREG[9:0] + 12) \times 58.5µA$$
$$I_{MOD} = (MODREG[8:0] + 16) \times 234µA$$

The LSb size of DDM_TXRPT[11:0] is 58.5µA. The maximum value of DDM_TXRPT[11:0] is 1199d (70.1mA), while the minimum value is 17d (1mA).

**NOTE:** The register DDM_TXRPT[11:0] can take on the value of Tx DC or Tx average. To select Tx DC, set the DDM_TXRPT_SEL bit to 0.

When the DDM_TX_SHDN bit is high, the DDM_TXRPT values (whether Tx DC or Tx average) are invalid and held at last value before the transmitter was disabled. This includes disable by means of POR, fault, DISABLE pin, TX_EN = 0, or XCVR_EN = 0.

**Tx Average Current**

The transmit average current is a calculation based on the laser DC current and the laser modulation current. It is shown as $I_{BIAS}$ in Figure 12. This value is located in the DDM_TXRPT[11:0] register (when DDM_TXRPT_SEL is set to 1) and calculated as:

Tx Average Current = DDM_TXRPT[11:0]

$$= I_{DC} + 0.484 \times I_{MOD}$$

where,

$$I_{DC} = (DCREG[9:0] + 12) \times 58.5µA$$
$$I_{MOD} = (MODREG[8:0] + 16) \times 234µA$$
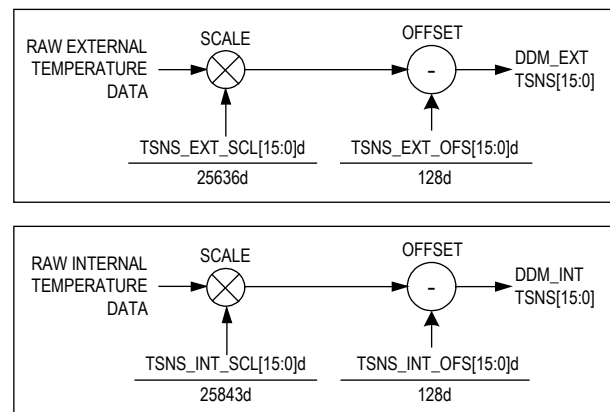


Figure 14. DDM Temperature Scale and Offset

The LSb size of DDM_TXRPT[11:0] is 58.5µA. The maximum value of DDM_TXRPT[11:0] is 2055d (120.2mA), while the minimum value is 43d (2.5mA).

**NOTE:** The register DDM_TXRPT[11:0] can take on the value of Tx DC or Tx average. To select Tx average, set the DDM_TXRPT_SEL bit to 1.

When the DDM_TX_SHDN bit is high, the DDM_TXRPT values (whether Tx DC or Tx average) are invalid and held at last value before the transmitter was disabled. This includes disable by means of POR, fault, DISABLE pin, TX_EN = 0, or XCVR_EN = 0.

**Tx Output Power**

The transmit power register value, DDM_TXP[11:0], is a measure of the monitor diode current at the MDIN pin. To convert the register value to the actual Tx Power, use the following equation:

$$P_{AVG} = (DDM\_TXP[11:0] \times 977nA)/K_{MD}$$

where $K_{MD}$ is the laser diode to monitor diode gain in A/W.

The DDM_TXP value is updated when the automatic power control ADC completes its averaging of 32 (MDAVG_CNT=0) or 256 (MDAVG_CNT=1) samples. These samples occur every 100ns while the transmitter is on, so DDM_TXP updates occur at every 256 × 100ns = 25.6µs when MDAVG_CNT=1.

The maximum value of DDM_TXP[11:0] is 4080d, while the minimum value is 32d.

**Rx Optical Power**

The MAX3956 reports the RSSI input current. The conversion between RSSI current and input optical power must be handled within the µC. For PIN diode receivers a simple linear scaling factor may be all that is needed to convert between RSSI current and optical power.

**RSSI Interface**

The RSSI pin is an ADC input used to measure RSSI current from the TIA. For optimum power-supply rejection it is recommended to connect 100pF in series with 5Ω between the RSSI pin and GND.

The RSSI pin voltage is regulated to 1.62V as shown in Figure 16. The input stage is designed to only sink

## Table 10. DDM Register Descriptions (Note 17)

| RAW ADC PARAMETER | UPPER REGISTER | LOWER REGISTER | BITS | UPDATE RATE DDM_AVG | | LSB SIZE | NOTES |
|---|---|---|---|---|---|---|---|
| | | | | Off (1x) | On (4x) | | |
| VCCX | DDM_VCCX[11:8] | DDM_VCCX[7:0] | 12 | 10ms | 40ms | 1.137mV | 18 |
| VCCT | DDM_VCCT[11:8] | DDM_VCCT[7:0] | 12 | 10ms | 40ms | 1.137mV | 18 |
| VCCTO | DDM_VCCTO[11:8] | DDM_VCCTO[7:0] | 12 | 10ms | 40ms | 1.137mV | 19 |
| BADC | DDM_BADC[11:8] | DDM_BADC[7:0] | 12 | 10ms | 40ms | 284.2µV | 19 |
| RSSI | DDM_RSSI[15:8] | DDM_RSSI[7:0] | 16 | 10ms | 40ms | 35.5nA | 19 |
| Internal Temperature | DDM_INT_TSNS[15:8] | DDM_INT_TSNS[7:0] | 16 | 10ms | 40ms | 1/256°C | 20 |
| External Temperature | DDM_EXT_TSNS[15:8] | DDM_EXT_TSNS[7:0] | 16 | 10ms | 40ms | 1/256°C | 20 |
| TX DC TX Average | DDM_TXRPT[11:8] | DDM_TXRPT[7:0] | 12 | 26µs | | 58.48µA | 21, 22 |
| TX Power | DDM_TXP[11:8] | DDM_TXP[7:0] | 12 | 26µs | | 977nA | 21 |

Note 17: Read both the upper and lower registers in a single block read.
Note 18: Unsigned result.
Note 19: Unsigned result. Results for negative inputs will be clamped to 00h.
Note 20: Upper byte is signed two's complement (-128 to +127), and lower byte is unsigned fractional (0 to 255/256).
Note 21: The result may be toggled between Laser DC current and Laser Average current using the DDM_TXRPT_SEL bit.

current. The RSSI will flag an interrupt (DDM_RSSI_LO_FAIL) if current is pulled out of this pin.

### Signal Loopback

For testing purposes, the Tx input signal can be routed to the Rx output (TIN± to ROUT±). Likewise, the Rx input signal can be routed to the laser output (RIN± to TOUTA/TOUTC). When engaging loopback of TIN to ROUT, be aware that if Rx squelching is enabled there needs to be an active signal at RIN for ROUT to be enabled. Similarly, if the Tx squelch mode is enabled, there needs to be a signal at TIN for TOUTA/TOUTC to be enabled. See Figure 17.

### Tx Fault, Transmitter Enable, Interrupt, and TOPSTAT Logic

#### Tx Fault Logic

The Tx fault logic provides detection of transmitter faults with fault indication bits located in the TXSTAT1 and TXSTAT2 registers. Any of the individual faults can be masked using the FMSK1 and FMSK2 registers.

Any fault indication bit, if masked, will flag but will not create a fault condition. When a fault condition occurs and is not masked, the transmitter will shut down unless masked by FMSK_TXFLT. To restart the transmitter after a shutdown has occurred, the source of the fault must be removed and either the DISABLE pin is toggled or the

MODECTRL register has 68h written to it. The fault logic is shown in Figure 18.
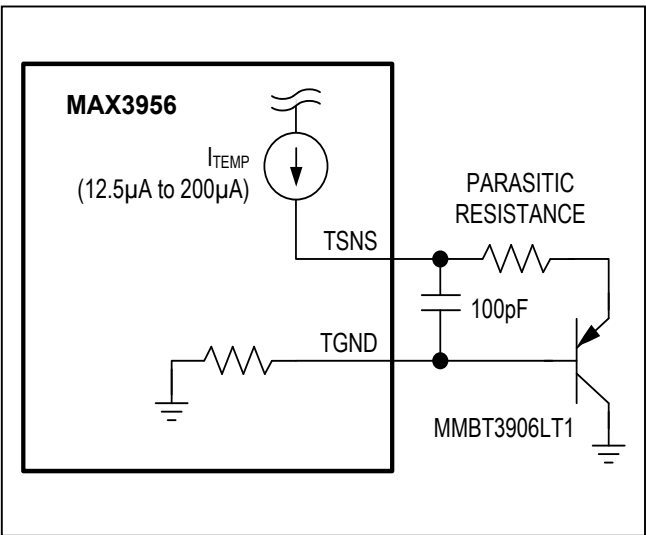


*Figure 15. External Temperature Sense Circuit*
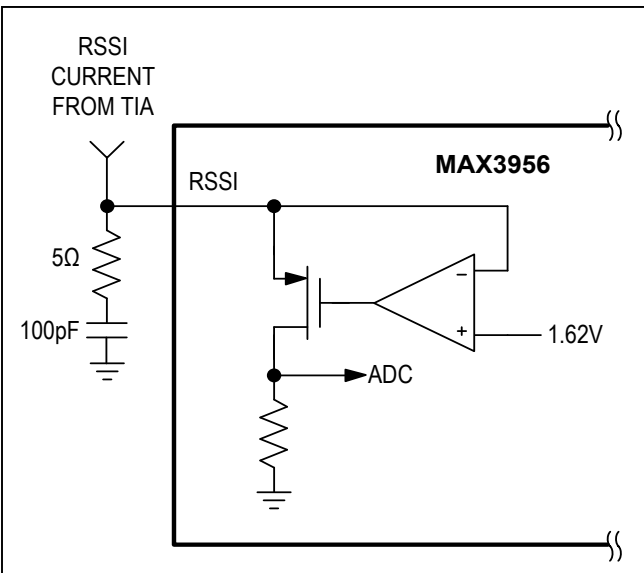


*Figure 16. RSSI Circuitry*
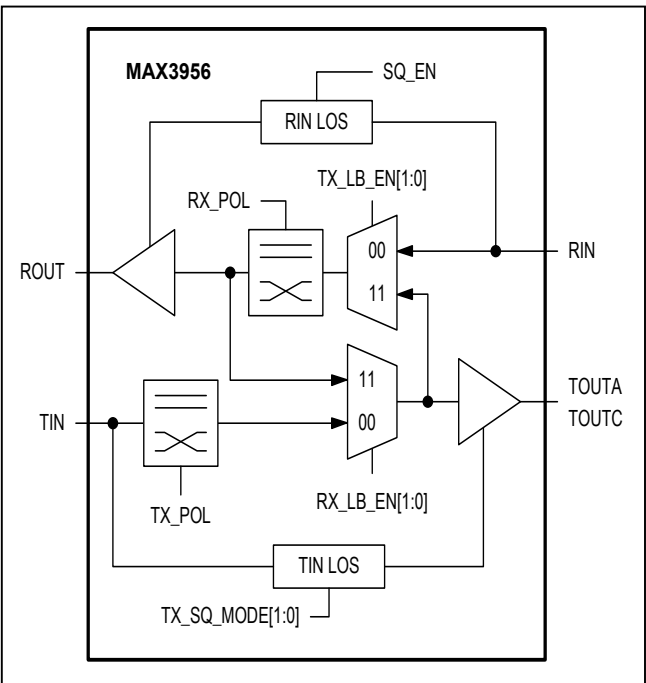


*Figure 17. Loopback Block Diagram*
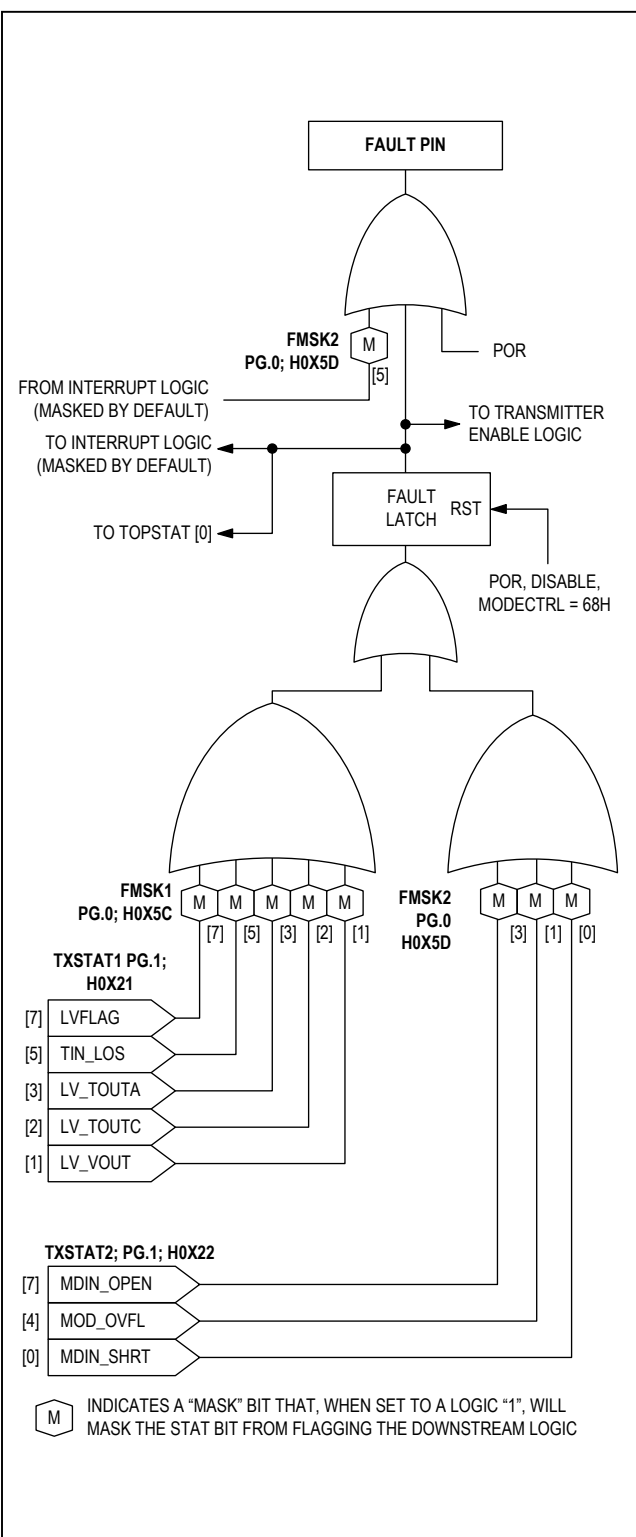
*Figure 18. Fault Logic*
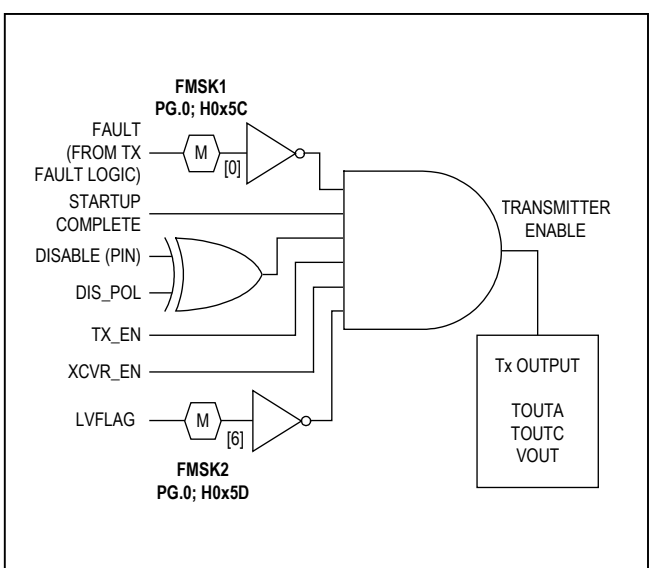


*Figure 19. Transmitter Enable Logic*

## Transmitter Enable Logic

The requirements for the transmitter to be enabled are shown in Figure 19. "Startup complete" is a delay that allows the on-chip systems to become stable after power-up and is typically 100µs.

## Interrupt Programmable Logic

INTRPT is a programmable pin that provides a trigger for real-time monitoring of internal status bits. Status registers RXSTAT, TXSTAT1, TXSTAT2, TXSTAT3, TXSTAT4, and DDMSTAT23 contain the bits that generate interrupt signals. Each of the bits in these registers can be individually masked if desired. If masked, the bit will still flag upon detection of its flag condition but the flag will not propagate to the INTRPT pin or the TOPSTAT register. Additional interrupts are POR and if unflagged, Tx fault. The interrupt logic is shown in Figure 20.

## TOPSTAT Logic

Status registers RXSTAT, TXSTAT1, TXSTAT2, TXSTAT3, TXSTAT4, and DDMSTAT23 feed the TOPSTAT register along with signals Tx fault, P3V sense, and POR. TOPSTAT bits PORD and P3VFLAG will be set to "1" after power-up or a POR event. These bits are "sticky" therefore need to be read to be cleared. The TOPSTAT logic diagram is shown in Figure 21.
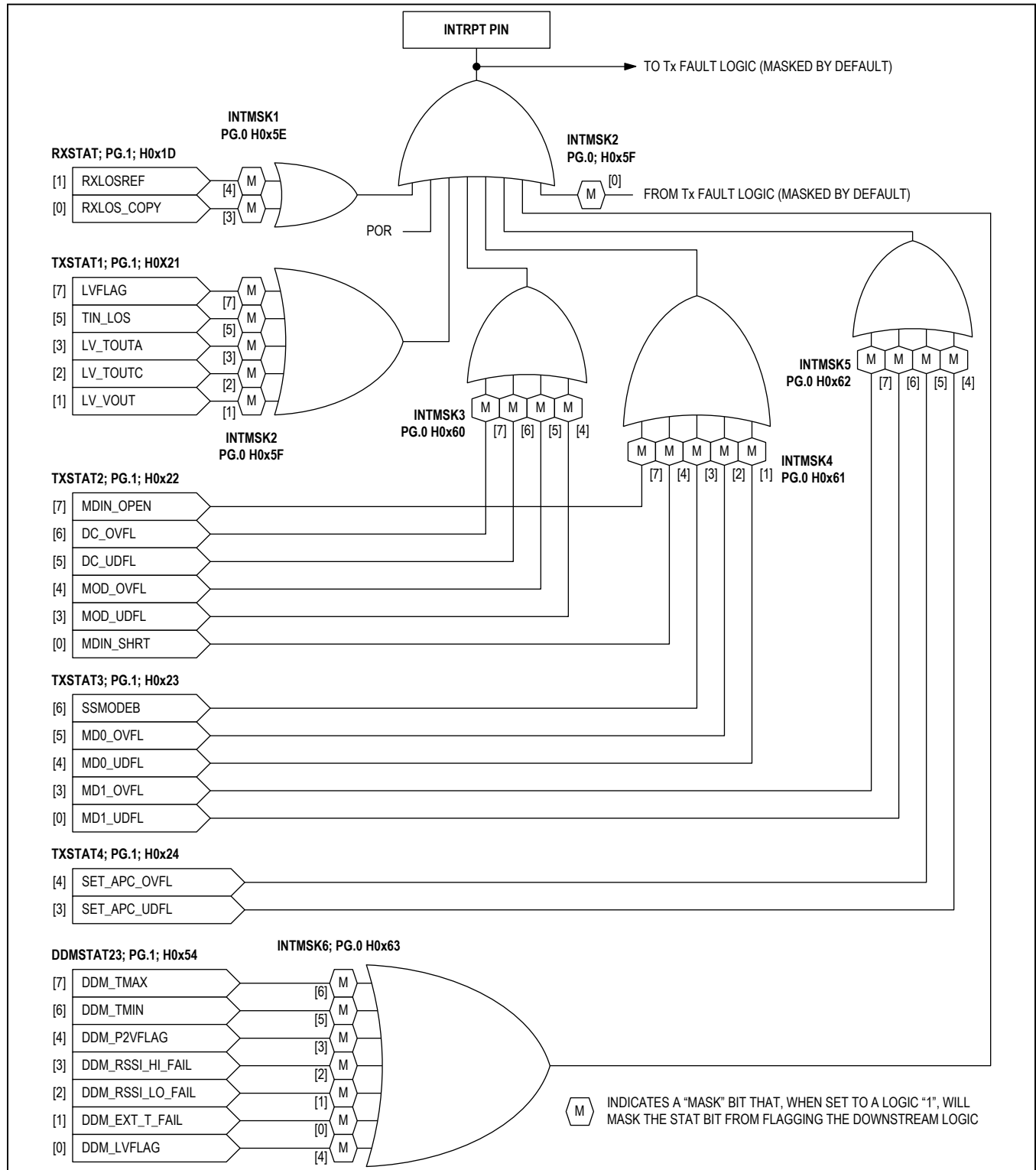
*Figure 20. Interrupt Logic*
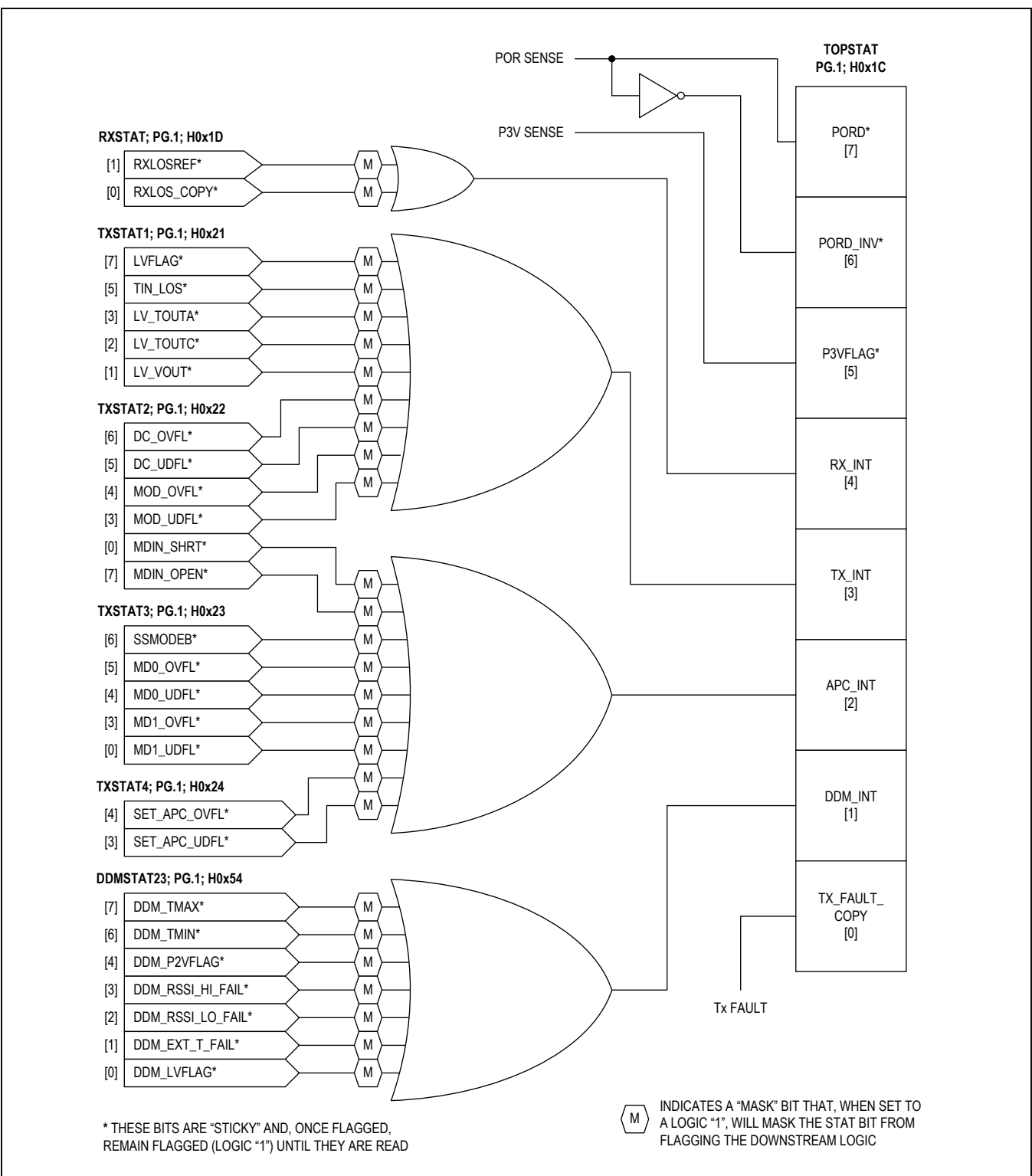
*Figure 21. TOPSTAT Logic*

The following are two different ways for using TOPSTAT:

Using the INTRPT pin

- Mask any undesired flags

- When INTRPT asserts, read TOPSTAT to narrow down the flag source. The flagged TOPSTAT bit indicates the type of interrupt flagged (APC, DDM, etc…) and which "STAT" register(s) must be read to locate the source of the flag, see Figure 21.

- Read the register(s) that triggered the TOPSTAT bit that is flagged. The individual source of the flag will remain flagged in the STAT register until it is read.

Not using the INTRPT Pin

- Mask any undesired flags

- Periodically read TOPSTAT to determine if any interrupts have flagged.

- If a TOPSTAT bit has flagged, read the register(s) responsible for triggering that TOPSTAT bit to determine the specific source of the flag.

## Table 11. Registers and Addresses for PAGE 0

| PAGE | ADDRESS | NAME | DEFAULT VALUE | FUNCTION |
|---|---|---|---|---|
| X | H0x00 | MODECTRL | 00h | Mode Control Register |
| | | | | |
| 0 | H0x3F | DDMCTRL1 | 64h | Upper Byte of External Temp Sensor Scale Factor |
| 0 | H0x40 | DDMCTRL2 | 24h | Lower Byte of External Temp Sensor Scale Factor |
| 0 | H0x41 | DDMCTRL3 | 88h | Upper Byte of External Temp Sensor Offset Factor |
| 0 | H0x42 | DDMCTRL4 | 93h | Lower Byte of External Temp Sensor Offset Factor |
| 0 | H0x43 | DDMCTRL5 | 64h | Upper Byte of Internal Temp Sensor Scale Factor |
| 0 | H0x44 | DDMCTRL6 | F3h | Lower Byte of Internal Temp Sensor Scale Factor |
| 0 | H0x45 | DDMCTRL7 | 88h | Upper Byte of Internal Temp Sensor Offset Factor |
| 0 | H0x46 | DDMCTRL8 | 93h | Lower Byte of Internal Temp Sensor Offset Factor |
| 0 | H0x47 | DDMCTRL9 | 80h | DDM Averaging, DC Monitor Control Register |
| | | | | |
| 0 | H0x49 | CALREG1 | XXh | Calibration Constant Register. Do not overwrite. See the *Load Factory Calibration Constants* section in the *Design Procedure* for the required calibration constants loading procedure. |
| 0 | H0x4A | CALREG2 | XXh | |
| 0 | H0x4B | CALREG3 | XXh | |
| 0 | H0x4C | CALREG4 | XXh | |
| 0 | H0x4D | CALREG5 | XXh | |
| | | | | |
| 0 | H0x4E | RXCTRL1 | 61h | Receiver Control Register |
| 0 | H0x4F | RXCTRL2 | E8h | Receiver Control Register |
| 0 | H0x50 | RXCTRL3 | 4Bh | Receiver Control Register |
| 0 | H0x51 | RXCTRL4 | C4h | Receiver Control Register |
| 0 | H0x52 | RXCTRL5 | 0Bh | Receiver Control Register |
| 0 | H0x53 | RXCTRL6 | A0h | Receiver Control Register |
| 0 | H0x55 | SET_CML | 09h | Receiver Output Voltage DAC |
| 0 | H0x56 | SET_LOS | 10h | Receiver Loss-of-Signal Threshold Setting |
| 0 | H0x58 | LOS_MASKTIME | 00h | LOS Output Masking Time Setting |
| | | | | |
| 0 | H0x59 | TXCTRL1 | 0Fh | Transmitter Control Register |
| 0 | H0x5A | TXCTRL2 | 12h | Transmitter Control Register |
| | | | | |

## Table 11. Registers and Addresses for PAGE 0 (continued)

| PAGE | ADDRESS | NAME | DEFAULT VALUE | FUNCTION |
|---|---|---|---|---|
| 0 | H0x5C | FMSK1 | 70h | Transmitter Fault Mask Register |
| 0 | H0x5D | FMSK2 | 3Fh | Transmitter Fault Mask Register |
| 0 | H0x5E | INTMSK1 | 7Fh | Transmitter Interrupt Mask Register |
| 0 | H0x5F | INTMSK2 | FFh | Transmitter Interrupt Mask Register |
| 0 | H0x60 | INTMSK3 | FFh | Transmitter Interrupt Mask Register |
| 0 | H0x61 | INTMSK4 | FFh | Transmitter Interrupt Mask Register |
| 0 | H0x62 | INTMSK5 | F0h | Transmitter Interrupt Mask Register |
| 0 | H0x63 | INTMSK6 | 7Fh | Transmitter Interrupt Mask Register |
| | | | | |
| 0 | H0x67 | TOPCTRL1 | 00h | Tx to Rx Loopback Control Register |
| 0 | H0x68 | TOPCTRL2 | 00h | Rx to Tx Loopback Control Register |

## Register Descriptions

## MAX3956 Mode Control Register (MODECTRL), Address: H0x00 (Page Independent)

| BIT | D[7:0] | DESCRIPTION |
|---|---|---|
| Bit Name | MODECTRL [7:0] | 00h = normal mode – read-only mode with exception of all increment registers (default) |
| Read/Write | R/W | 12h = setup mode – enables write permission clears after each write operation<br>68h = fault clear mode – clears all faults including the fault latch at FAULT pin |
| POR State | 00h<br>Normal Mode & Page 0 | There are two register address page select settings:<br>55h = select page-1 (default)<br>81h = select page-0 |
| Reset Upon Read | No | Read-back returns 0 when page 0 is selected and 1 when page 1 is selected |

## DDM Control Register (DDMCTRL1), Address: H0x3F (Page 0)

| BIT | D[7:0] | DESCRIPTION |
|---|---|---|
| Bit Name | TSNS_EXT_SCL[15:8] | This is the upper byte of the external temperature sense scale factor. This byte, along with the lower byte represents a 16-bit, unsigned value. |
| Read/Write | R/W<br>Write in setup mode only | |
| POR State | 64h | |

## DDM Control Register (DDMCTRL2), Address: H0x40 (Page 0)

| BIT | D[7:0] | DESCRIPTION |
|---|---|---|
| Bit Name | TSNS_EXT_SCL[7:0] | This is the lower byte of the external temperature sense scale factor. This byte, along with the upper byte represents a 16-bit, unsigned value. |
| Read/Write | R/W Write in setup mode only | |
| POR State | 24h | |

## DDM Control Register (DDMCTRL3), Address: H0x41 (Page 0)

| BIT | D[7:0] | DESCRIPTION |
|---|---|---|
| Bit Name | TSNS_EXT_OFS[15:8] | This is the upper byte of the external temperature offset term. This, along with the lower byte represents a 16-bit, unsigned value. TSNS_EXT_OFS[15:0] is divided by 128 then subtracted from the scaled external-temperature data, see Figure 14. |
| Read/Write | R/W Write in setup mode only | |
| POR State | 88h | |

## DDM Control Register (DDMCTRL4), Address: H0x42 (Page 0)

| BIT | D[7:0] | DESCRIPTION |
|---|---|---|
| Bit Name | TSNS_EXT_OFS[7:0] | This is the lower byte of the external temperature offset term. This, along with the upper byte represents a 16-bit, unsigned value. TSNS_EXT_OFS[15:0] is divided by 128 then subtracted from the scaled external-temperature data, see Figure 14. |
| Read/Write | R/W Write in setup mode only | |
| POR State | 93h | |

## DDM Control Register (DDMCTRL5), Address: H0x43 (Page 0)

| BIT | D[7:0] | DESCRIPTION |
|---|---|---|
| Bit Name | TSNS_INT_SCL[15:8] | This is the upper byte of the internal temperature scale factor. This, along with the lower byte represents a 16-bit, unsigned value. |
| Read/Write | R/W Write in setup mode only | |
| POR State | 64h | |

## DDM Control Register (DDMCTRL6), Address: H0x44 (Page 0)

| BIT | D[7:0] | DESCRIPTION |
|---|---|---|
| Bit Name | TSNS_INT_SCL[7:0] | This is the lower byte of the internal temperature scale factor. This, along with the upper byte represents a 16-bit, unsigned value. |
| Read/Write | R/W Write in setup mode only | |
| POR State | F3h | |

## DDM Control Register (DDMCTRL7), Address: H0x45 (Page 0)

| BIT | D[7:0] | DESCRIPTION |
|---|---|---|
| Bit Name | TSNS_INT_OFS[15:8] | This is the upper byte of the internal temperature offset term. This, along with the lower byte represents a 16-bit, unsigned value. TSNS_INT_OFS[15:0] is divided by 128 then subtracted from the scaled internal-temperature data, see Figure 14. |
| Read/Write | R/W<br>Write in setup mode only | |
| POR State | 88h | |

## DDM Control Register (DDMCTRL8), Address: H0x46 (Page 0)

| BIT | D[7:0] | DESCRIPTION |
|---|---|---|
| Bit Name | TSNS_INT_OFS[7:0] | This is the lower byte of the internal temperature offset term. This, along with the upper byte represents a 16-bit, unsigned value. TSNS_INT_OFS[15:0] is divided by 128 then subtracted from the scaled internal-temperature data, see Figure 14. |
| Read/Write | R/W<br>Write in setup mode only | |
| POR State | 93h | |

## DDM Control Register (DDMCTRL9), Address: H0x47 (Page 0)

| BIT | D7 | D[6:3] | D2 | D[1:0] |
|---|---|---|---|---|
| Bit Name | DDM_AVG | RES | DDM_TXRPT_SEL | RES |
| Read/Write | R/W, Write in setup mode only | | | |
| POR State | 1 | 0000 | 0 | 00 |

| BIT | NAME | DESCRIPTION |
|---|---|---|
| D[7] | DDM_AVG | Enables DDM averaging.<br>0 = no averaging<br>1 = 4x averaging (default) |
| D[6:3] | RES | Reserved |
| D[2] | DDM_TXRPT_SEL | Controls what the DDM_TXRPT register reports<br>0 = Tx DC current monitor (default)<br>1 = Tx average current monitor |
| D[1:0] | RES | Reserved |

## Calibration Register (CALREG1), Address: H0x49 (Page 0)

| BIT | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|
| Bit Name | RES | CAL1[6] | CAL1[5] | CAL1[4] | CAL1[3] | CAL1[2] | CAL1[1] | CAL1[0] |
| Read/Write | R | R/W, Write in setup mode only | | | | | | |
| POR State | 0 | X | X | X | X | X | X | X |

Factory-calibrated register. Do not overwrite. Calibration constants must be loaded after POR. See Load Factory Calibration Constants.

## Calibration Register (CALREG2), Address: H0x4A (Page 0)

| BIT | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|
| Bit Name | RES | CAL2[6] | CAL2[5] | CAL2[4] | CAL2[3] | CAL2[2] | CAL2[1] | CAL2[0] |
| Read/Write | R | R/W, Write in setup mode only | | | | | | |
| POR State | 0 | X | X | X | X | X | X | X |

Factory calibrated register. Do not overwrite. Calibration constants must be loaded after POR. See Load Factory Calibration Constants.

## Calibration Register (CALREG3), Address: H0x4B (Page 0)

| BIT | D[7:6] | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|
| Bit Name | RES | CAL3[5] | CAL3[4] | CAL3[3] | CAL3[2] | CAL3[1] | CAL3[0] |
| Read/Write | R | R/W Write in setup mode only | | | | | |
| POR State | 00 | X | X | X | X | X | X |

Factory-calibrated register. Do not overwrite. Calibration constants must be loaded after POR. See Load Factory Calibration Constants.

## Calibration Register (CALREG4), Address: H0x4C (Page 0)

| BIT | D[7:4] | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|
| Bit Name | RES | CAL4[3] | CAL4[2] | CAL4[1] | CAL4[0] |
| Read/Write | R | R/W, Write in setup mode only | | | |
| POR State | 0000 | X | X | X | X |

Factory-calibrated register. Do not overwrite. Calibration constants must be loaded after POR. See Load Factory Calibration Constants.

## Calibration Register (CALREG5), Address: H0x4D (Page 0)

| BIT | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|
| Bit Name | CAL5[7] | CAL5[6] | CAL5[5] | CAL5[4] | CAL5[3] | CAL5[2] | CAL5[1] | CAL5[0] |
| Read/Write | R/W, Write in setup mode only | | | | | | | |
| POR State | X | X | X | X | X | X | X | X |

Factory-calibrated register. Do not overwrite. Calibration constants must be loaded after POR. See Load Factory Calibration Constants.

## Receiver Control Register (RXCTRL1), Address: H0x4E (Page 0)

| BIT | D7 | D6 | D5 | D4 | D[3:1] | D0 |
|---|---|---|---|---|---|---|
| Bit Name | RES | RX_EN | RX_OUT_EN | SQ_EN | RES | RX_POL |
| Read/Write | R | R/W, Write in setup mode only | | | | |
| POR State | 0 | 1 | 1 | 0 | 000 | 1 |

| BIT | NAME | DESCRIPTION |
|---|---|---|
| D[7] | RES | Reserved |
| D[6] | RX_EN | Enables Rx core circuitry<br>0 = disabled – powers down the entire RX section<br>1 = enabled (default) |
| D[5] | RX_OUT_EN | This bit directly controls the mode of the RX output stage<br>0 = disabled to common-mode voltage<br>1 = enabled (default) |
| D[4] | SQ_EN | This bit enables control of the RX output stage by means of LOS event<br>0 = disabled (default)<br>1 = enabled LOS event disables the RX output stage to common mode |
| D[3:1] | RES | Reserved. Must be set to 000 for proper operation. |
| D[0] | RX_POL | Sets polarity of the Rx receiver path<br>0 = inverted<br>1 = normal (default) |

## Receiver Control Register (RXCTRL2), Address: H0x4F (Page 0)

| BIT | D7 | D6 | D5 | D[4:3] | D[2:0] |
|---|---|---|---|---|---|
| Bit Name | RES | RSEL_POL | RATE_SEL | SET_RXBW[1:0] | SET_RXDE[2:0] |
| Read/Write | R/W, Write in setup mode only | | | | |
| POR State | 1 | 1 | 1 | 01 | 000 |

| BIT | NAME | DESCRIPTION |
|---|---|---|
| D[7] | RES | Reserved. Must be set to 1 for proper operation. |
| D[6] | RSEL_POL | Sets polarity of the RSEL pin<br>0 = inverted<br>1 = normal (default) |
| D[5] | RATE_SEL | Rate select bit. Logical OR combination of this bit and RSEL pin controls Rx path selection.<br>0 = Low-bandwidth mode<br>1 = High-bandwidth mode (default) |
| D[4:3] | SET_RXBW[1:0] | SET_RXBW sets the -3dB BW of the lowpass filter in a low BW Rx path the meaning of the two bits changes with RX data path selection. See below:<br><br>**RATE_SEL + RSEL = 0**　　　　**RATE_SEL + RSEL = 1**<br>　00 = 1GHz　　　　01 = High-bandwidth mode (default)<br>　01 = 2GHz　　　　　All others = Reserved<br>　10 = 2.5GHz<br>　11 = 3GHz |
| D[2:0] | SET_RXDE[2:0] | Sets deemphasis for the Rx output stage to compensate for FR4 loss at 10Gbps<br>0xx = disabled (default)<br>100 = 1dB deemphasis<br>101 = 2dB deemphasis<br>110 = 3dB deemphasis<br>111 = 4dB deemphasis |

## Receiver Control Register (RXCTRL3), Address: H0x50 (Page 0)

| BIT | D[7:3] | D[2:1] | D0 |
|---|---|---|---|
| Bit Name | RES | AZ_BW[1:0] | RES |
| Read/Write | R/W, Write in setup mode only | | |
| POR State | 01001 | 01 | 1 |

| BIT | NAME | DESCRIPTION |
|---|---|---|
| D[7:3] | RES | Reserved |
| D[2:1] | AZ_BW[1:0] | Selects the auto-zero bandwidth<br>00 = 5kHz<br>01 = 10kHz (default)<br>10 = 20kHz<br>11 = 40kHz |
| D[0] | RES | Reserved |

## Receiver Control Register (RXCTRL4), Address: H0x51 (Page 0)

| BIT | D7 | D6 | D[5:0] |
|---|---|---|---|
| Bit Name | RES | LOS_POL | RES |
| Read/Write | R/W, Write in setup mode only | | |
| POR State | 1 | 1 | 000100 |

| BIT | NAME | DESCRIPTION |
|---|---|---|
| D[7] | RES | Reserved |
| D[6] | LOS_POL | Selects the LOS polarity<br>0 = inverted<br>1 = normal (default) |
| D[5:0] | RES | Reserved |

## Receiver Control Register (RXCTRL5), Address: H0x52 (Page 0)

| BIT | D[7:4] | D3 | D[2:0] |
|---|---|---|---|
| Bit Name | RES | LOS_EN | RES |
| Read/Write | R/W, Write in setup mode only | | |
| POR State | 0000 | 1 | 011 |

| BIT | NAME | DESCRIPTION |
|---|---|---|
| D[7:4] | RES | Reserved |
| D[3] | LOS_EN | LOS enable<br>0 = disabled<br>1 = enabled (default) |
| D[2:0] | RES | Reserved |

## Receiver Control Register (RXCTRL6), Address: H0x53 (Page 0)

| BIT | D[7:5] | D4 | D[3:0] |
|---|---|---|---|
| Bit Name | RES | LOS_PU_EN | RES |
| Read/Write | R/W, Write in setup mode only | | |
| POR State | 101 | 0 | 0000 |

| BIT | NAME | DESCRIPTION |
|---|---|---|
| D[7:5] | RES | Reserved |
| D[4] | LOS_PU_EN | Enables active pullup on LOS pin. When enabled the LOS output becomes a push-pull CMOS output.<br>0 = disabled, open-drain output (default)<br>1 = enabled, push-pull CMOS output |
| D[3:0] | RES | Reserved |

### Receiver Control Register (SET_CML), Address: H0x55 (Page 0)

| BIT | D[7:5] | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|
| Bit Name | RES | SET_CML[4] | SET_CML[3] | SET_CML[2] | SET_CML[1] | SET_CML[0] |
| Read/Write | R/W, Write in setup mode only | | | | | |
| POR State | 000 | 0 | 1 | 0 | 0 | 1 |

| BIT | NAME | DESCRIPTION |
|---|---|---|
| D[7:5] | RES | Reserved |
| D[4:0] | SET_CML[4:0] | Set Rx output amplitude. Amplitudes listed below are valid for SET_RXDE = 0xx<br>0 0000 = 400mV$_{P-P}$<br>…<br>0 1001 = 600mV$_{P-P}$ (default)<br>…<br>1 1111 = 1V$_{P-P}$ |

### Receiver Control Register (RXCTRL7), Address: H0x56 (Page 0)

| BIT | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|
| Bit Name | SET_LOS[6] | SET_LOS[5] | SET_LOS[4] | SET_LOS[3] | SET_LOS[2] | SET_LOS[1] | SET_LOS[0] | RES |
| Read/Write | R/W, Write in setup mode only | | | | | | | |
| POR State | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 |

| BIT | NAME | DESCRIPTION |
|---|---|---|
| D[7:1] | SET_LOS[6:0] | Set LOS threshold. Assert threshold approximately 1.2mV$_{P-P}$ × SET_LOS[6:0]. Deassert threshold is approximately 1.6 × the assert threshold to avoid LOS chatter due to noise.<br>00 0000 = minimum assert level<br>…<br>00 1000 = 9.6mV$_{P-P}$ differential (default)<br>…<br>11 1111 = maximum assert level |
| D[0] | RES | Reserved |

## Receiver Control Register (LOS_MASKTIME), Address: H0x58 (Page 0)

| BIT | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| Bit Name | RES | LOS_MASK TIME[6] | LOS_MASK TIME[5] | LOS_ MASK TIME[4] | LOS_MASK TIME[3] | LOS_MASK TIME[2] | LOS_MASK TIME[1] | LOS_MASK TIME[0] |
| Read/Write | R/W, Write in setup mode only | | | | | | | |
| POR State | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| BIT | NAME | DESCRIPTION |
|-----|------|-------------|
| D[7] | RES | Reserved |
| D[6:0] | LOS_MASKTIME[6:0] | Sets masking time for LOS. The LSb size is 36µs.<br>000 0000 = 0µs (default) |

## Transmitter Control Register (TXCTRL1), Address: H0x59 (Page 0)

| BIT | D7 | D[6:5] | D4 | D3 | D[2:1] | D0 |
|-----|-----|--------|-----|-----|--------|-----|
| Bit Name | LOW_DC_EN | RES | FAULT_PU_EN | FAULT_POL | RES | TX_POL |
| Read/Write | R/W, Write in setup mode only | | | | | |
| POR State | 0 | 00 | 0 | 1 | 11 | 1 |

| BIT | NAME | DESCRIPTION |
|-----|------|-------------|
| D[7] | LOW_DC_EN | Enables low-DC current mode when low laser threshold current is needed<br>0 = disabled (default)<br>1 = enabled |
| D[6:5] | RES | Reserved |
| D[4] | FAULT_PU_EN | Enables active pull-up on FAULT pin. When enabled the FAULT output becomes a push-pull CMOS output.<br>0 = disabled, open-drain output (default)<br>1 = enabled, push-pull CMOS output |
| D[3] | FAULT_POL | Sets FAULT pin polarity<br>0 = inverted<br>1 = normal (default) |
| D[2:1] | RES | Reserved |
| D[0] | TX_POL | Sets TX data path polarity<br>0 = inverted<br>1 = normal (default) |

## Transmitter Control Register (TXCTRL2), Address: H0x5A (Page 0)

| BIT | D[7:5] | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|
| Bit Name | RES | DIS_POL | TX_EQ[1] | TX_EQ[0] | TX_SQ_MODE[1] | TX_SQ_MODE[0] |
| Read/Write | R/W Write in setup mode only | | | | | |
| POR State | 000 | 1 | 0 | 0 | 1 | 0 |

| BIT | NAME | DESCRIPTION |
|---|---|---|
| D[7:5] | RES | Reserved |
| D[4] | DIS_POL | Sets polarity of DISABLE pin<br>0 = inverse<br>1 = normal (default) |
| D[3:2] | TX_EQ[1:0] | Selects TX input equalization<br>00 = 1.5dB boost at 5.1GHz (default)<br>01 = 3dB boost at 5.1GHz<br>10 = 4.5dB boost at 5.1GHz<br>11 = 5.5dB boost at 5.1GHz |
| D[1:0] | TX_SQ_MODE[1:0] | Tx output squelch-modes during TIN LOS event<br>00 = no current into TOUTC pin<br>01 = sink current set to a midlevel corresponding to $P_{AVG}$ at current temperature<br>10 = modulation current is disabled but APC loop remains active (default)<br>11 = squelch disabled |

## Fault Mask Control Register (FMSK1), Address: H0x5C (Page 0)

| BIT | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|
| Bit Name | FMSK_ LVFLAG | RES | FMSK_ TIN_LOS | RES | FMSK_ TOUTA | FMSK_ TOUTC | FMSK_ VOUT | FMSK_ TXFLT |
| Read/Write | R/W Write in setup mode only | | | | | | | |
| POR State | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 0 |

The FMSK1 register sets mask bits preventing individual events to latch fault at FAULT pin.

| BIT | NAME | DESCRIPTION |
|---|---|---|
| D[7] | FMSK_LVFLAG | Mask LVFLAG fault condition on $V_{CCTO}$ pin<br>0 = no mask (default)<br>1 = mask |
| D[6] | RES | Reserved |
| D[5] | FMSK_TIN_LOS | Mask TIN_LOS fault condition<br>0 = unmasked<br>1 = mask (default) |
| D[4] | RES | Reserved |
| D[3] | FMSK_TOUTA | Mask LV_TOUTA fault condition<br>0 = no mask (default)<br>1 = mask |
| D[2] | FMSK_TOUTC | Mask LV_TOUTC fault condition<br>0 = no mask (default)<br>1 = mask |
| D[1] | FMSK_VOUT | Mask LV_VOUT fault condition<br>0 = no mask (default)<br>1 = mask |
| D[0] | FMSK_TXFLT | Masks the FAULT latch signal, which controls the output stage on/off behavior.<br>0 = No mask (default)<br>1 = Mask<br>When FMSK1[0] = 1, output stage behavior becomes independent of FAULT conditions. |

## Fault Mask Control Register (FMSK2), Address: H0x5D (Page 0)

| BIT | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|
| Bit Name | — | FMSK_ LVFLAG_ OUTDIS | FMSK_ INTRPT_ FAULT | RES | FMSK_ MDIN_OPEN | RES | FMSK_ MOD_OVFL | FMSK_ MDIN_SHRT |
| Read/Write | R/W Write in setup mode only | | | | | | | |
| POR State | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 |

The FMSK2 register sets mask bits preventing individual events to latch fault at FAULT pin.

| BIT | NAME | DESCRIPTION |
|---|---|---|
| D[6] | FMSK_LVFLAG_OUTDIS | Mask Tx output disable during LVFLAG event<br>0 = no mask (default)<br>1 = mask |
| D[5] | FMSK_INTRPT_FAULT | Mask logic OR combination of interrupt event and fault event at FAULT pin.<br>0 = no mask<br>1 = mask (default) |
| D[4] | RES | Reserved |
| D[3] | FMSK_MDIN_OPEN | Mask MDIN_OPEN fault condition<br>0 = no mask<br>1 = mask (default) |
| D[2] | RES | Reserved |
| D[1] | FMSK_MOD_OVFL | Mask MOD_OVFL fault condition. Threshold set by MODMAX register.<br>0 = no mask<br>1 = mask (default) |
| D[0] | FMSK_MDIN_SHRT | Mask MDIN_SHRT fault condition<br>0 = no mask<br>1 = mask (default) |

## Interrupt Mask Control Register (INTMSK1), Address: H0x5E (Page 0)

| BIT | D[7:5] | D4 | D3 | D[2:0] |
|---|---|---|---|---|
| Bit Name | RES | INTMSK_RXLOSREF | INTMSK_RXLOS | RES |
| Read/Write | R/W Write in setup mode only | | | |
| POR State | 011 | 1 | 1 | 111 |

The INTMSK1 register sets mask bits preventing individual events to latch interrupt at INTRPT pin.

| BIT | NAME | DESCRIPTION |
|---|---|---|
| D[7:5] | RES | Reserved |
| D[4] | INTMSK_RXLOSREF | Mask RXLOSREF interrupt from INTRPT pin and TOPSTAT register<br>0 = no mask<br>1 = mask (default) |
| D[3] | INTMSK_RXLOS | Mask RXLOS copy from INTRPT pin and TOPSTAT register<br>0 = no mask<br>1 = mask (default) |
| D[2:0] | RES | Reserved |

## Interrupt Mask Control Register (INTMSK2), Address: H0x5F (Page 0)

| BIT | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|
| Bit Name | INTMSK_<br>LVFLAG | RES | INTMSK_<br>TIN_LOS | RES | INTMSK_<br>TOUTA | INTMSK_<br>TOUTC | INTMSK_<br>VOUT | INTMSK_<br>FAULT |
| Read/Write | R/W Write in setup mode only | | | | | | | |
| POR State | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

The INTMSK2 register sets mask bits preventing individual events to latch interrupt at INTRPT pin.

| BIT | NAME | DESCRIPTION |
|---|---|---|
| D[7] | INTMSK_LVFLAG | Mask LVFLAG interrupt from INTRPT pin and TOPSTAT register<br>0 = no mask<br>1 = mask (default) |
| D[6] | RES | Reserved |
| D[5] | INTMSK_TIN_LOS | Mask TIN_LOS interrupt from INTRPT pin and TOPSTAT register<br>0 = no mask<br>1 = mask (default) |
| D[4] | RES | Reserved |
| D[3] | INTMSK_TOUTA | Mask LV_TOUTA interrupt from INTRPT pin and TOPSTAT register<br>0 = no mask<br>1 = mask (default) |
| D[2] | INTMSK_TOUTC | Mask LV_TOUTC interrupt from INTRPT pin and TOPSTAT register<br>0 = no mask<br>1 = mask (default) |
| D[1] | INTMSK_VOUT | Mask LV_VOUT interrupt from INTRPT pin and TOPSTAT register<br>0 = no mask<br>1 = mask (default) |
| D[0] | INTMSK_FAULT | Mask fault event from INTRPT pin<br>0 = no mask<br>1 = mask (default) |

## Interrupt Mask Control Register (INTMSK3), Address: H0x60 (Page 0)

| BIT | D7 | D6 | D5 | D4 | D[3:0] |
|---|---|---|---|---|---|
| Bit Name | INTMSK_DC_OVFL | INTMSK_DC_UDFL | INTMSK_MOD_OVFL | INTMSK_MOD_UDFL | RES |
| Read/Write | R/W Write in setup mode only | | | | |
| POR State | 1 | 1 | 1 | 1 | 1111 |

The INTMSK3 register sets mask bits preventing individual events to latch interrupt at INTRPT pin.

| BIT | NAME | DESCRIPTION |
|---|---|---|
| D[7] | INTMSK_DC_OVFL | Mask DC_OVFL interrupt from INTRPT pin and TOPSTAT register<br>0 = no mask<br>1 = mask (default) |
| D[6] | INTMSK_DC_UDFL | Mask DC_UDFL interrupt from INTRPT pin and TOPSTAT register<br>0 = no mask<br>1 = mask (default) |
| D[5] | INTMSK_MOD_OVFL | Mask MOD_OVFL interrupt from INTRPT pin and TOPSTAT register<br>0 = no mask<br>1 = mask (default) |
| D[4] | INTMSK_MOD_UDFL | Mask MOD_UDFL interrupt from INTRPT pin and TOPSTAT register<br>0 = no mask<br>1 = mask (default) |
| D[3:0] | RES | Reserved |

## Interrupt Mask Control Register (INTMSK4), Address: H0x61 (Page 0)

| BIT | D7 | D[6:5] | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|
| Bit Name | INTMSK_MDOPEN | RES | INTMSK_MDIN_SHRT | INTMSK_SSMODE | INTMSK_MD0OVFL | INTMSK_MD0UDFL | RES |
| Read/Write | R/W Write in setup mode only | | | | | | |
| POR State | 1 | 11 | 1 | 1 | 1 | 1 | 1 |

The INTMSK4 register sets mask bits preventing individual events to latch interrupt at INTRPT pin.

| BIT | NAME | DESCRIPTION |
|---|---|---|
| D[7] | INTMSK_MDOPEN | Mask MDIN_OPEN interrupt from INTRPT pin and TOPSTAT register<br>0 = no mask<br>1 = mask (default) |
| D[6:5] | RES | Reserved |
| D[4] | INTMSK_MDIN_SHRT | Mask MDIN_SHRT interrupt from INTRPT pin and TOPSTAT register<br>0 = no mask<br>1 = mask (default) |
| D[3] | INTMSK_SSMODE | Mask SSMODE interrupt from INTRPT pin and TOPSTAT register<br>0 = no mask<br>1 = mask (default) |
| D[2] | INTMSK_MD0OVFL | Mask MD0_OVFL interrupt from INTRPT pin and TOPSTAT register<br>0 = no mask<br>1 = mask (default) |
| D[1] | INTMSK_MD0UDFL | Mask MD0_UDFL interrupt from INTRPT pin and TOPSTAT register<br>0 = no mask<br>1 = mask (default) |
| D[0] | RES | Reserved |

## Interrupt Mask Control Register (INTMSK5), Address: H0x62 (Page 0)

| BIT | D7 | D6 | D5 | D4 | D[3:0] |
|-----|----|----|----|----|--------|
| Bit Name | INTMSK_MD1OVFL | INTMSK_MD1UDFL | INTMSK_SETAPC_OVFL | INTMSK_SETAPC_UDFL | RES |
| Read/Write | R/W Write in setup mode only | | | | |
| POR State | 1 | 1 | 1 | 1 | 0000 |

The INTMSK5 register sets mask bits preventing individual events to latch interrupt at INTRPT pin.

| BIT | NAME | DESCRIPTION |
|-----|------|-------------|
| D[7] | INTMSK_MD1OVFL | Mask MD1_OVFL interrupt from INTRPT pin and TOPSTAT register<br>0 = no mask<br>1 = mask (default) |
| D[6] | INTMSK_MD1UDFL | Mask MD1_UDFL interrupt from INTRPT pin and TOPSTAT register<br>0 = no mask<br>1 = mask (default) |
| D[5] | INTMSK_SETAPC_OVFL | Mask SET_APC_OVFL interrupt from INTRPT pin and TOPSTAT register<br>0 = no mask<br>1 = mask (default) |
| D[4] | INTMSK_SETAPC_UDFL | Mask SET_APC_UDFL interrupt from INTRPT pin and TOPSTAT register<br>0 = no mask<br>1 = mask (default) |
| D[3:0] | RES | Reserved |

## Interrupt Mask Control Register (INTMSK6), Address: H0x63 (Page 0)

| BIT | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|
| Bit Name | RES | INTMSK_ DDMTMAX | INTMSK_ DDMTMIN | INTMSK_DDM_ LVFLAG | INTMSK_ P2VFLAG | INTMSK_ RSSI_HI | INTMSK_ RSSI_LO | INTMSK_ EXT_TF |
| Read/Write | R/W Write in setup mode only | | | | | | | |
| POR State | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

The INTMSK6 register sets mask bits preventing individual events to latch interrupt at INTRPT pin.

| BIT | NAME | DESCRIPTION |
|---|---|---|
| D[7] | RES | Reserved |
| D[6] | INTMSK_DDMTMAX | Mask DDM_TMAX interrupt from INTRPT pin and TOPSTAT register<br>0 = no mask<br>1 = mask (default) |
| D[5] | INTMSK_ DDMTMIN | Mask DDM_TMIN interrupt from INTRPT pin and TOPSTAT register<br>0 = no mask<br>1 = mask (default) |
| D[4] | INTMSK_DDM_ LVFLAG | Mask DDM_LVFLAG interrupt from INTRPT pin and TOPSTAT register<br>0 = no mask<br>1 = mask (default) |
| D[3] | INTMSK_ P2VFLAG | Mask DDM_P2VFLAG interrupt (VCCX and VCCT) from INTRPT pin and TOPSTAT register<br>0 = no mask<br>1 = mask (default) |
| D[2] | INTMSK_RSSI_HI | Mask DDM RSSI reading stuck high interrupt from INTRPT pin and TOPSTAT register<br>0 = no mask<br>1 = mask (default) |
| D[1] | INTMSK_RSSI_LO | Mask DDM RSSI reading stuck low interrupt from INTRPT pin and TOPSTAT register<br>0 = no mask<br>1 = mask (default) |
| D[0] | INTMSK_EXT_TF | Mask DDM_EXT_T_FAIL external temperature reading flag/fault interrupt (missing connection to external PNP) from INTRPT pin and TOPSTAT register<br>0 = no mask<br>1 = mask (default) |

## Tx to Rx Loopback Control Register (TOPCTRL1), Address: H0x67 (Page 0)

| BIT | D[7:6] | D[5:4] | D[3:0] |
|---|---|---|---|
| Bit Name | RES | TX_LB_EN[1:0] | RES |
| Read/Write | R/W Write in setup mode only | | |
| POR State | 00 | 00 | 0000 |

The TOPCTRL1 register enables signal loopback from the Tx input to the Rx output.

| BIT | NAME | DESCRIPTION |
|---|---|---|
| D[7:6] | RES | Reserved |
| D[5:4] | TX_LB_EN[1:0] | Transmitter Loopback Enable<br>00 = Tx to Rx loopback disabled (default)　　01 = Reserved<br>11 = Tx to Rx loopback enabled　　10 = Reserved |
| D[3:0] | RES | Reserved |

## Rx to Tx Loopback Control Register (TOPCTRL2), Address: H0x68 (Page 0)

| BIT | D[7:6] | D[5:4] | D[3:0] |
|---|---|---|---|
| Bit Name | RES | RX_LB_EN[1:0] | RES |
| Read/Write | R/W Write in setup mode only | | |
| POR State | 00 | 00 | 0000 |

The TOPCTRL2 register enables signal loopback from the Rx input to the Tx output.

| BIT | NAME | DESCRIPTION |
|---|---|---|
| D[7:6] | RES | Reserved |
| D[5:4] | RX_LB_EN[1:0] | Receiver Loopback Enable<br>00 = Rx to Tx loopback disabled (default)　　01 = Reserved<br>11 = Rx to Tx loopback enabled　　10 = Reserved |
| D[3:0] | RES | Reserved |

## Table 12. Registers and Addresses for PAGE 1

| PAGE | ADDRESS | NAME | DEFAULT VALUE | FUNCTION |
|---|---|---|---|---|
| X | H0x00 | MODECTRL | 00h | Mode Control Register |
| | | | | |
| 1 | H0x01 | TXCTRL3 | 02h | Transmitter Control Register |
| 1 | H0x02 | TXCTRL4 | 0Ah | Transmitter Control Register |
| 1 | H0x0A | TXCTRL5 | 08h | Transmitter Control Register |
| 1 | H0x0B | TXCTRL6 | 80h | Transmitter Control Register |
| 1 | H0x0C | DCMAX | 12h | This register sets the [9:2] SET_DC DAC Code Limit |
| 1 | H0x0D | MODMAX | 30h | This register sets the [8:1]SET_MOD DAC Code Limit |
| 1 | H0x0E | SET_DC | 00h | Laser DC Current DAC Initial Value |
| 1 | H0x0F | SET_MOD | 00h | Laser Modulation Current DAC Initial Value |

## Table 12. Registers and Addresses for PAGE 1 (continued)

| PAGE | ADDRESS | NAME | DEFAULT VALUE | FUNCTION |
|------|---------|------|---------------|----------|
| 1 | H0x10 | DCINC | 00h | SET_DC DAC Two's Complement Increment Register |
| 1 | H0x11 | MODINC | 00h | SET_MOD DAC Two's Complement Increment Register |
| 1 | H0x12 | SET_APC | 80h | APC Loop Target Setting Register |
| 1 | H0x13 | APCINC | 00h | SET_APC Target Two's Complement Increment Register |
| 1 | H0x14 | TXCTRL7 | 14h | Transmitter Control Register |
| 1 | H0x15 | TOPCTRL3 | 90h | Transceiver Control Register |
| 1 | H0x16 | DCREG | 00h | Laser DC Current DAC Read-Back |
| 1 | H0x17 | MODREG | 00h | Laser Modulation Current DAC Read-Back |
| 1 | H0x18 | MD1REGH | 00h | Upper Byte of Digitized Top Peak Value of MD Input Current |
| 1 | H0x19 | MD1REGL | 00h | Lower Byte of Digitized Top Peak Value of MD Input Current |
| 1 | H0x1A | MD0REGH | 00h | Upper Byte of Digitized Bottom Peak Value of MD Input Current |
| 1 | H0x1B | MD0REGL | 00h | Lower Byte of Digitized Bottom Peak Value of MD Input Current |
| | | | | |
| 1 | H0x1C | TOPSTAT | A0h | Transceiver Status Register |
| 1 | H0x1D | RXSTAT | 10h | Receiver Status Register |
| 1 | H0x21 | TXSTAT1 | 00h | Transmitter Status Register |
| 1 | H0x22 | TXSTAT2 | 00h | Transmitter Status Register |
| 1 | H0x23 | TXSTAT3 | 00h | Transmitter Status Register |
| 1 | H0x24 | TXSTAT4 | 00h | Transmitter Status Register |
| 1 | H0x3E | DDMSTAT1 | 00h | Upper Byte of Digitized RSSI Value |
| 1 | H0x3F | DDMSTAT2 | 00h | Lower Byte of Digitized RSSI Value |
| 1 | H0x40 | DDMSTAT3 | 00h | Upper Byte of Digitized VCCX Value |
| 1 | H0x41 | DDMSTAT4 | 00h | Lower Byte of Digitized VCCX Value |
| 1 | H0x42 | DDMSTAT5 | 00h | Upper Byte of Digitized VCCT Value |
| 1 | H0x43 | DDMSTAT6 | 00h | Lower Byte of Digitized VCCT Value |
| 1 | H0x44 | DDMSTAT7 | 00h | Upper Byte of Digitized VCCTO Value |
| 1 | H0x45 | DDMSTAT8 | 00h | Lower Byte of Digitized VCCTO Value |
| 1 | H0x46 | DDMSTAT9 | 00h | Upper Byte of Digitized Auxiliary Voltage Value at BADC Pin |
| 1 | H0x47 | DDMSTAT10 | 00h | Lower Byte of Digitized Auxiliary Voltage Value at BADC Pin |
| 1 | H0x48 | DDMSTAT11 | 00h | Upper Byte of Digitized External Temp-Sensor Value at TSNS Pin |
| 1 | H0x49 | DDMSTAT12 | 00h | Lower Byte of Digitized External Temp-Sensor Value at TSNS Pin |
| 1 | H0x4A | DDMSTAT13 | 00h | Upper Byte of Digitized Internal Temp-Sensor Value |
| 1 | H0x4B | DDMSTAT14 | 00h | Lower Byte of Digitized Internal Temp-Sensor Value |
| 1 | H0x4C | DDMSTAT15 | 00h | DDM Status Register & Upper 4 bits of DC Monitor Current Value |
| 1 | H0x4D | DDMSTAT16 | 00h | Lower Byte of DC Monitor Current Value |
| 1 | H0x4E | DDMSTAT17 | 00h | Upper Byte of Digitized TX Power Value |
| 1 | H0x4F | DDMSTAT18 | 00h | Lower Byte of Digitized TX Power Value |
| 1 | H0x54 | DDMSTAT23 | 00h | DDM Status Register |

## Transmitter Control Register (TXCTRL3), Address: H0x01 (Page 1)

| BIT | D7 | D[6:2] | D1 | D0 |
|---|---|---|---|---|
| Bit Name | LOOP_STOP | RES | AUTORNG_EN | SOFT_RESET |
| Read/Write | R/W Write in setup mode only | | | |
| POR State | 0 | 0 0000 | 1 | 0 |

| BIT | NAME | DESCRIPTION |
|---|---|---|
| D[7] | LOOP_STOP | Halts the APC loop. This bit can only be changed from a 1 to a 0 by writing 1 to LOOP_RUN.<br>0 = no action (default)<br>1 = halts APC loop |
| D[6:2] | RES | Reserved |
| D[1] | AUTORNG_EN | Enables auto-ranging of MDIN_GAIN.<br>0 = auto-ranging disabled<br>1 = auto-ranging enabled. When using APCINC the MAX3956 will automatically adjust gain setting of MDIN_GAIN in order to keep SET_APC in the range of 127 to 255 (default) |
| D[0] | SOFT_RESET | Soft reset will reset all registers to their default (POR) values. The Tx must be disabled, via DISABLE pin or TX_EN bit, before a soft reset can occur.<br>0 = no action (default)<br>1 = soft reset |

## Transmitter Control Register (TXCTRL4), Address: H0x02 (Page 1)

| BIT | D[7:2] | D1 | D0 |
|---|---|---|---|
| Bit Name | RES | MDAVG_CNT | RES |
| Read/Write | R/W Write in setup mode only | | |
| POR State | 00 0010 | 1 | 0 |

| BIT | NAME | DESCRIPTION |
|---|---|---|
| D[7:2] | RES | Reserved |
| D[1] | MDAVG_CNT | Select averaging depth for the MDIN signal.<br>0 = 32 averaging<br>1 = 256 averaging (default) |
| D[0] | RES | Reserved |

## Transmitter Control Register (TXCTRL5), Address: H0x0A (Page 1)

| BIT | D7 | D6 | D5 | D4 | D[3:0] |
|---|---|---|---|---|---|
| Bit Name | RES | APC_EN | IBUPDT_EN | IMUPDT_EN | RES |
| Read/Write | R/W Write in setup mode only | | | | |
| POR State | 0 | 0 | 0 | 0 | 1000 |

| BIT | NAME | DESCRIPTION |
|---|---|---|
| D[7] | RES | Reserved |
| D[6] | APC_EN | Enables APC loop<br>0 = disabled (default)<br>1 = enabled |
| D[5] | IBUPDT_EN | Sets the way DCREG[9:0] is written to:<br>APC enabled:<br>0 = maintains last value of DCREG[9:0] in initialization (default)<br>1 = FAULT/POR/RESTART initializes DCREG[9:2] with SET_DC[7:0]<br>APC off:<br>0 = DCREG can only be changed by writing to DCINC[4:0] (default)<br>1 = if IBUPDT_EN is already set to 1 a write to SET_DC[7:0] is passed to DCREG[9:2] |
| D[4] | IMUPDT_EN | Sets the way MODREG[9:0] is written to:<br>0 = MODREG can only be changed by writing to MODINC[4:0] (default)<br>1 = if IMUPDT_EN is already set to 1 a write to SET_MOD[7:0] is passed to MODREG[8:1] |
| D[3:0] | RES | Reserved |

## Transmitter Control Register (TXCTRL6), Address: H0x0B (Page 1)

| BIT | D[7:1] | D0 |
|---|---|---|
| Bit Name | RES | AUX_RESTART |
| Read/Write | R/W Write in setup mode only | |
| POR State | 1 | 0 |

| BIT | NAME | DESCRIPTION |
|---|---|---|
| D[7:1] | RES | Reserved |
| D[0] | AUX_RESTART | Enables restarting of APC loop by means of DISABLE pin.<br>0 = disabled (default)<br>1 = enabled |

## Maximum DC-Current Register (DCMAX), Address: H0x0C (Page 1)

| BIT | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|
| Bit Name | DCMAX [7] | DCMAX [6] | DCMAX [5] | DCMAX [4] | DCMAX [3] | DCMAX [2] | DCMAX [1] | DCMAX [0] |
| Read/Write | R/W Write in setup mode only | | | | | | | |
| POR State | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 |

The DCMAX register limits the maximum digital code setting in DCREG current DAC control register.

| BIT | NAME | DESCRIPTION |
|---|---|---|
| D[7:0] | DCMAX[7:0] | Programs the maximum settable DC current (limits the maximum value that can be written to the DCREG[9:2] register). Note that it only relates to the eight most significant bits of the DCREG register.<br>$I_{DCMAX}$ = (DCMAX[7:0] + 3) x 234µA<br>18d = 4.9mA DC current limit (default) |

## Maximum Modulation-Current Register (MODMAX), Address: H0x0D (Page 1)

| BIT | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|
| Bit Name | MODMAX [7] | MODMAX [6] | MODMAX [5] | MODMAX [4] | MODMAX [3] | MODMAX [2] | MODMAX [1] | MODMAX [0] |
| Read/Write | R/W Write in setup mode only | | | | | | | |
| POR State | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 |

The MODMAX register limits the maximum digital code setting in MODREG current DAC control register.

| BIT | NAME | DESCRIPTION |
|---|---|---|
| D[7:0] | MODMAX[7:0] | Programs the maximum settable modulation current (limits the maximum value that can be written to the MODREG[8:1] register). Note that it only relates to the eight MSBs of the MODREG register.<br>$I_{MODMAX}$ = (MODMAX[7:0] + 8) x 468µA<br>48d = 26mA$_{P-P}$ modulation current limit (default) |

## Initial or Open-Loop DC Current Register (SET_DC), Address: H0x0E (Page 1)

| BIT | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|
| Bit Name | SET_DC [7] | SET_DC [6] | SET_DC [5] | SET_DC [4] | SET_DC [3] | SET_DC [2] | SET_DC [1] | SET_DC [0] |
| Read/Write | R/W Write in setup mode only | | | | | | | |
| POR State | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

The SET_DC register set the initial or open-loop laser DC current.

| BIT | NAME | DESCRIPTION |
|---|---|---|
| D[7:0] | SET_DC[7:0] | Programs the initial or open-loop DC current. The value in this register is sent to the DCREG[9:0] register's eight MSBs.<br>$I_{DC}$ = (SET_DC[7:0] + 3) x 234µA<br>0d = 0.7mA DC current (default) |

## Modulation Current Register (SET_MOD), Address: H0x0F (Page 1)

| BIT | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|
| Bit Name | SET_MOD [7] | SET_MOD [6] | SET_MOD [5] | SET_MOD [4] | SET_MOD [3] | SET_MOD [2] | SET_MOD [1] | SET_MOD [0] |
| Read/Write | R/W Write in setup mode only | | | | | | | |
| POR State | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

The SET_MOD register sets modulation current.

| BIT | NAME | DESCRIPTION |
|---|---|---|
| D[7:0] | SET_MOD[7:0] | Programs the modulation current. The value in this register is sent to the MODREG[8:0] register's eight MSBs.<br>$I_{MOD} = (SET\_MOD[7:0] + 8) \times 468\mu A$<br>0d = 3.7mA$_{P\text{-}P}$ modulation current (default) |

## DC Current Increment Register (DCINC), Address: H0x10 (Page 1)

| BIT | D[7:5] | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|
| Bit Name | RES | DCINC[4] | DCINC[3] | DCINC[2] | DCINC[1] | DCINC[0] |
| Read/Write | R | R/W Write in any mode | | | | |
| POR State | 000 | 0 | 0 | 0 | 0 | 0 |

The DCINC register increments/decrements code in DCREG DAC control register as described below.

| BIT | NAME | DESCRIPTION |
|---|---|---|
| D[7:5] | RES | Reserved |
| D[4:0] | DCINC[4:0] | Mode when APC enabled:<br>DCINC[3:0] controls the maximum allowed step and hence influences APC loop dynamics especially during startup.<br>x 0000 = 0 maximum step allowed for DCREG[9:0]<br>x 1111 = 15d maximum step allowed for DCREG[9:0]<br><br>Mode when APC disabled:<br>Laser DC current increment/decrement applied to DCREG[9:0] upon write (two's complement number, the range is +15/-16).<br>1 0000 = subtract 16 from DCREG[9:0]<br>0 1111 = add 15 to DCREG[9:0] |

## Modulation Increment Register (MODINC), Address: H0x11 (Page 1)

| BIT | D[7:5] | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|
| Bit Name | RES | MODINC[4] | MODINC[3] | MODINC[2] | MODINC[1] | MODINC[0] |
| Read/Write | R | R/W Write in any mode | | | | |
| POR State | 000 | 0 | 0 | 0 | 0 | 0 |

The MODINC register increments/decrements code in MODREG DAC control register as described below.

| BIT | NAME | DESCRIPTION |
|---|---|---|
| D[7:5] | RES | Reserved |
| D[4:0] | MODINC[4:0] | Laser modulation current increment/decrement applied to MODREG[8:0] upon write (two's complement number, the range is +15/-16).<br>1 0000 = subtract 16 from MODREG[8:0]<br>0 1111 = add 15 to MODREG[8:0] |

## Average MD Current Target Register (SET_APC), Address: H0x12 (Page 1)

| BIT | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|
| Bit Name | SET_APC[7] | SET_APC[6] | SET_APC[5] | SET_APC[4] | SET_APC[3] | SET_APC[2] | SET_APC[1] | SET_APC[0] |
| Read/Write | R/W Write in setup mode only | | | | | | | |
| POR State | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

The SET_APC register sets the average laser power for the APC loop (see the *Design Procedure* section for more information).

| BIT | NAME | DESCRIPTION |
|---|---|---|
| D[7:0] | SET_APC [7:0] | Sets the closed-loop MDIN target average current. This closed-loop current depends on SET_APC and MDIN_GAIN registers. |

## APC Increment Register (APCINC), Address: H0x13 (Page 1)

| BIT | D[7:4] | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|
| Bit Name | RES | APCINC[3] | APCINC[2] | APCINC[1] | APCINC[0] |
| Read/Write | R | R/W Write in any mode | | | |
| POR State | 0000 | 0 | 0 | 0 | 0 |

The APCINC register increments/decrements the SET_APC register.

| BIT | NAME | DESCRIPTION |
|---|---|---|
| D[7:4] | RES | Reserved |
| D[3:0] | APCINC[3:0] | Increments or decrements the SET_APC[7:0] value with the two's complement value from APCINC[3:0] (the range is +7/-8).<br>1000 = subtract 8 from SET_APC[7:0]<br>0111 = add 7 to SET_APC[7:0] |

## Transmitter Control Register (TXCTRL7), Address: H0x14 (Page 1)

| BIT | D[7:3] | D2 | D1 | D0 |
|---|---|---|---|---|
| Bit Name | RES | MDIN_GAIN[2] | MDIN_GAIN[1] | MDIN_GAIN[0] |
| Read/Write | R/W Write in setup mode only | | | |
| POR State | 0 0010 | 1 | 0 | 0 |

| BIT | NAME | DESCRIPTION |
|---|---|---|
| D[7:3] | RES | Reserved |
| D[2:0] | MDIN_GAIN[2:0] | Selects the transimpedance gain of the MDIN input<br>000 = 156Ω          011 = 1248Ω<br>001 = 312Ω         1xx = 2496Ω (default)<br>010 = 624Ω |

## Transceiver Control Register (TOPCTRL3), Address: H0x15 (Page 1)

| BIT | D7 | D6 | D[5:3] | D2 | D1 | D0 |
|---|---|---|---|---|---|---|
| Bit Name | LOOP_RUN | LOOP_RESTART | RES | LOOP_TH | TX_EN | XCVR_EN |
| Read/Write | R/W Write in setup mode only | | | | | |
| POR State | 1 | 0 | 010 | 0 | 0 | 0 |

| BIT | NAME | DESCRIPTION |
|---|---|---|
| D[7] | LOOP_RUN | Controls the APC loop. LOOP_RUN can only be changed from a 1 to a 0 by writing a 1 to LOOP_STOP.<br>0 = no action<br>1 = APC loop will restart from last saved prefreeze conditions (subject to IBUPDT_EN) |
| D[6] | LOOP_RESTART | Forces APC loop out of steady-state and enables the start-up state machine<br>0 = no action (default)<br>1 = restart |
| D[5:3] | RES | Reserved |
| D[2] | LOOP_TH | Sets threshold for updating DCREG<br>0 = 0.125 LSb (default)<br>1 = 0.75 LSb |
| D[1] | TX_EN | Enables the Tx data path, control loop, and the DC current and modulation current DACs.<br>0 = Tx disabled (default)<br>1 = Tx enabled |
| D[0] | XCVR_EN | Top-level Transceiver enable<br>0 = disabled (default)<br>1 = enabled |

## DC Current DAC Readback Register (DCREG), Address: H0x16 (Page 1)

| BIT | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|
| Bit Name | DCREG [9] | DCREG [8] | DCREG [7] | DCREG [6] | DCREG [5] | DCREG [4] | DCREG [3] | DCREG [2] |
| Read/Write | Read only | | | | | | | |
| POR State | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Reset Upon Read | No | No | No | No | No | No | No | No |

The DCREG register provides a read-back value of the DC current DAC.

| BIT | NAME | DESCRIPTION |
|---|---|---|
| D[7:0] | DCREG[9:2] | DC current DAC readback. The two LSbs for this register are located at Page 1 Address: H0x24[2:1]. |

## Modulation Current DAC Readback Register (MODREG), Address: H0x17 (Page 1)

| BIT | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|
| Bit Name | MODREG [8] | MODREG [7] | MODREG [6] | MODREG [5] | MODREG [4] | MODREG [3] | MODREG [2] | MODREG [1] |
| Read/Write | Read only | | | | | | | |
| POR State | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

The MODREG register provides a read-back value of the MOD current DAC.

| BIT | NAME | DESCRIPTION |
|---|---|---|
| D[7:0] | MODREG[8:1] | Modulation current DAC readback. The LSb for this register is located at Page 1 Address: H0x24[0]. |

## Monitor Diode Top Peak (Averaged) Register (MD1REGH), Address: H0x18 (Page 1)

| BIT | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|
| Bit Name | MD1REG [15] | MD1REG [14] | MD1REG [13] | MD1REG [12] | MD1REG [11] | MD1REG [10] | MD1REG [9] | MD1REG [8] |
| Read/Write | Read only | | | | | | | |
| POR State | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Reset Upon Read | No | No | No | No | No | No | No | No |

The MD1REGH register provides a read-back value of the digitized top peak current at MD input.

| BIT | NAME | DESCRIPTION |
|---|---|---|
| D[7:0] | MD1REG[15:8] | Stored (averaged) value for monitor-diode current peak corresponding to optical P1. MD1REGH is the upper 8 bits of the 16-bit value MD1REG[15:0]. |

## Monitor Diode Top Peak (Averaged) Register (MD1REGL), Address: H0x19 (Page 1)

| BIT | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|
| Bit Name | MD1REG [7] | MD1REG [6] | MD1REG [5] | MD1REG [4] | MD1REG [3] | MD1REG [2] | MD1REG [1] | MD1REG [0] |
| Read/Write | Read only | | | | | | | |
| POR State | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Reset Upon Read | No | No | No | No | No | No | No | No |

The MD1REGL register provides a read-back value of the digitized top peak current at MD input.

| BIT | NAME | DESCRIPTION |
|---|---|---|
| D[7:0] | MD1REG[7:0] | Stored (averaged) value for monitor-diode current peak corresponding to optical P1. MD1REGL is the lower 8 bits of the 16-bit value MD1REG[15:0]. |

## Monitor Diode Bottom Peak (Averaged) Register (MD0REGH), Address: H0x1A (Page 1)

| BIT | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|
| Bit Name | MD0REG [15] | MD0REG [14] | MD0REG [13] | MD0REG [12] | MD0REG [11] | MD0REG [10] | MD0REG [9] | MD0REG [8] |
| Read/Write | Read only | | | | | | | |
| POR State | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Reset Upon Read | No | No | No | No | No | No | No | No |

The MD0REGH register provides a read-back value of the digitized bottom peak current at MD input.

| BIT | NAME | DESCRIPTION |
|---|---|---|
| D[7:0] | MD0REG[15:8] | Stored (averaged) value for monitor-diode current peak corresponding to optical P0. MD0REGH is the upper 8 bits of the 16-bit value MD0REG[15:0]. |

## Monitor Diode Bottom Peak (Averaged) Register (MD0REGL), Address: H0x1B (Page 1)

| BIT | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|
| Bit Name | MD0REG [7] | MD0REG [6] | MD0REG [5] | MD0REG [4] | MD0REG [3] | MD0REG [2] | MD0REG [1] | MD0REG [0] |
| Read/Write | Read only | | | | | | | |
| POR State | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Reset Upon Read | No | No | No | No | No | No | No | No |

The MD0REGL register provides a read-back value of the digitized bottom peak current at MD input.

| BIT | NAME | DESCRIPTION |
|---|---|---|
| D[7:0] | MD0REG[7:0] | Stored (averaged) value for monitor-diode current peak corresponding to optical P0. MD0REGL is the lower 8 bits of the 16-bit value MD0REG[15:0]. |

## Top Level Status Register (TOPSTAT), Address: H0x1C (Page 1)

| BIT | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|
| Bit Name | PORD | PORD_INV | P3VFLAG | RX_INT | TX_INT | APC_INT | DDM_INT | TX_FAULT_ COPY |
| Read/Write | Read only | | | | | | | |
| POR State | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 |
| Reset Upon Read | Yes* | Yes* | Yes* | No | No | No | No | No |

*Sticky bit—Once flagged these registers remain flagged (logic 1) until they are read. Once read, they are reset to 0 if the source of the flag has been removed.

The TOPSTAT register is a status register for the top-level circuitry.

| BIT | NAME | DESCRIPTION |
|---|---|---|
| D[7] | PORD | Power-on-reset of the digital core. $V_{DD}$ vs. 1.3V<br>0 = deasserted<br>1 = asserted (default) |
| D[6] | PORD_INV | Inverse of PORD<br>0 = deasserted (default)<br>1 = asserted |
| D[5] | P3VFLAG | $V_{CCX}$/$V_{CCT}$ vs. 2.5V<br>0 = deasserted<br>1 = asserted (default) |
| D[4] | RX_INT | Interrupt/fault in Rx group. Read RXSTAT.<br>0 = deasserted (default)<br>1 = asserted |
| D[3] | TX_INT | Interrupt/fault in Tx group. Read TXSTAT1 and TXSTAT2.<br>0 = deasserted (default)<br>1 = asserted |
| D[2] | APC_INT | Interrupt/fault in APC group. Read TXSTAT2, TXSTAT3, and TXSTAT4<br>0 = deasserted (default)<br>1 = asserted |
| D[1] | DDM_INT | Interrupt/fault in DDM group. Read DDMSTAT23.<br>0 = deasserted (default)<br>1 = asserted |
| D[0] | TX_FAULT_COPY | A copy of FAULT pin value<br>0 = deasserted (default)<br>1 = asserted |

## Receiver Status Register (RXSTAT), Address: H0x1D (Page 1)

| BIT | D[7:5] | D4 | D[3:2] | D1 | D0 |
|---|---|---|---|---|---|
| Bit Name | RES | RX_RATE | RES | RXLOSREF | RXLOS_COPY |
| Read/Write | Read only | | | | |
| POR State | 000 | 1 | 00 | 0 | 0 |
| Reset Upon Read | N/A | No | N/A | Yes* | Yes* |

*Sticky bit- Once flagged these registers remain flagged (logic 1) until they are read. Once read, they are reset to 0 if the source of the flag has been removed.

| BIT | NAME | DESCRIPTION |
|---|---|---|
| D[7:5] | RES | Reserved |
| D[4] | RX_RATE | Receiver data-rate setting. It is the logical OR of the RSEL pin and RATE_SEL bit.<br>0 = Rx set for < 4G operation<br>1 = Rx set for > 4G operation |
| D[3:2] | RES | Reserved |
| D[1] | RXLOSREF | Interrupt Rx LOS block reference signal failure<br>0 = deasserted (default)<br>1 = asserted |
| D[0] | RXLOS_COPY | A copy of Rx LOS pin value<br>0 = deasserted (default)<br>1 = asserted |

## Transmitter Status Register (TXSTAT1), Address: H0x21 (Page 1)

| BIT | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|
| Bit Name | LVFLAG | RES | TIN_LOS | RES | LV_TOUTA | LV_TOUTC | LV_VOUT | TX_DIS_ COPY |
| Read/Write | Read only | | | | | | | |
| POR State | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Reset Upon Read | Yes* | No | Yes* | Yes* | Yes* | Yes* | Yes* | No |

*Sticky bit- Once flagged these registers remain flagged (logic 1) until they are read. Once read, they are reset to 0 if the source of the flag has been removed.

| BIT | NAME | DESCRIPTION |
|---|---|---|
| D[7] | LVFLAG | Interrupt/fault: $V_{CCT}$ or $V_{CCTO}$ under-voltage detection<br>0 = deasserted (default)<br>1 = asserted |
| D[6] | RES | Reserved |
| D[5] | TIN_LOS | Interrupt/fault: Indicates TIN AC signal too low<br>0 = deasserted (default)<br>1 = asserted |
| D[4] | RES | Reserved |
| D[3] | LV_TOUTA | Interrupt/fault: TOUTA open or shorted to GND.<br>0 = deasserted (default)<br>1 = asserted |
| D[2] | LV_TOUTC | Interrupt/fault: TOUTC open or shorted to GND.<br>0 = deasserted (default)<br>1 = asserted |
| D[1] | LV_VOUT | Interrupt/fault: VOUT fault under-voltage detection (referenced to $V_{CCTO}$)<br>0 = deasserted (default)<br>1 = asserted |
| D[0] | TX_DIS_COPY | Copy of DISABLE pin. Polarity, controlled by DIS_POL, is included in this bit. |

## Transmitter Status Register (TXSTAT2), Address: H0x22 (Page 1)

| BIT | D7 | D6 | D5 | D4 | D3 | D[2:1] | D0 |
|---|---|---|---|---|---|---|---|
| Bit Name | MDIN_OPEN | DC_OVFL | DC_UDFL | MOD_OVFL | MOD_UDFL | RES | MDIN_SHRT |
| Read/Write | Read only | | | | | | |
| POR State | 0 | 0 | 0 | 0 | 0 | 00 | 0 |
| Reset Upon Read | Yes* | Yes* | Yes* | Yes* | Yes* | No | Yes* |

*Sticky bit—Once flagged these registers remain flagged (logic 1) until they are read. Once read, they are reset to 0 if the source of the flag has been removed.

| BIT | NAME | DESCRIPTION |
|---|---|---|
| D[7] | MDIN_OPEN | Interrupt/fault: MDIN pin open<br>0 = deasserted (default)<br>1 = asserted |
| D[6] | DC_OVFL | Interrupt: DCREG input over maximum warning<br>0 = deasserted (default)<br>1 = asserted |
| D[5] | DC_UDFL | Interrupt: DCREG input underflow warning<br>0 = deasserted (default)<br>1 = asserted |
| D[4] | MOD_OVFL | Interrupt/fault: MODREG input over maximum warning<br>0 = deasserted (default)<br>1 = asserted |
| D[3] | MOD_UDFL | Interrupt: MODREG input underflow warning<br>0 = deasserted (default)<br>1 = asserted |
| D[2:1] | RES | Reserved |
| D[0] | MDIN_SHRT | Interrupt/fault: MDIN shorted to ground or supply.<br>0 = deasserted (default)<br>1 = asserted |

## Transmitter Status Register (TXSTAT3), Address: H0x23 (Page 1)

| BIT | D7 | D6 | D5 | D4 | D3 | D2 | D[1:0] |
|---|---|---|---|---|---|---|---|
| Bit Name | SSMODE | SSMODEB | MD0_OVFL | MD0_UDFL | MD1_OVFL | MD1_UDFL | RES |
| Read/Write | Read only | | | | | | |
| POR State | 0 | 1 | 0 | 0 | 0 | 0 | 00 |
| Reset Upon Read | No | Yes* | Yes* | Yes* | Yes* | Yes* | No |

*Sticky bit—Once flagged these registers remain flagged (logic 1) until they are read. Once read, they are reset to 0 if the source of the flag has been removed.

| BIT | NAME | DESCRIPTION |
|---|---|---|
| D[7] | SSMODE | APC steady-state mode monitor<br>0 = acquisition mode (default)<br>1 = steady-state mode |
| D[6] | SSMODEB | APC inverted steady-state mode monitor<br>0 = steady-state mode<br>1 = acquisition mode (default) |
| D[5] | MD0_OVFL | Interrupt: MD0REG input over maximum warning<br>0 = deasserted (default)<br>1 = asserted |
| D[4] | MD0_UDFL | Interrupt: MD0REG input underflow warning<br>0 = deasserted (default)<br>1 = asserted |
| D[3] | MD1_OVFL | Interrupt: MD1REG input over maximum warning<br>0 = deasserted (default)<br>1 = asserted |
| D[2] | MD1_UDFL | Interrupt: MD1REG input underflow warning<br>0 = deasserted (default)<br>1 = asserted |
| D[1:0] | RES | Reserved |

## Transmitter Status Register (TXSTAT4), Address: H0x24 (Page 1)

| BIT | D[7:5] | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|
| Bit Name | RES | SET_APC_OVFL | SET_APC_UDFL | DCREG[1] | DCREG[0] | MODREG[0] |
| Read/Write | Read only | | | | | |
| POR State | 000 | 0 | 0 | 0 | 0 | 0 |
| Reset Upon Read | No | Yes* | Yes* | No | No | No |

*Sticky bit—Once flagged these registers remain flagged (logic 1) until they are read. Once read, they are reset to 0 if the source of the flag has been removed.

| BIT | NAME | DESCRIPTION |
|---|---|---|
| D[7:5] | RES | Reserved |
| D[4] | SET_APC_OVFL | Interrupt: APCINC setting attempting to overflow SET_APC register<br>0 = deasserted (default)<br>1 = asserted |
| D[3] | SET_APC_UDFL | (AUTORNG_EN=1)<br>Interrupt: SET_APC below minimum value.<br>0 = deasserted (default)<br>1 = asserted<br><br>(AUTORNG_EN = 0)<br>Interrupt: SET_APC below 64d.<br>0 = deasserted (default)<br>1 = asserted |
| D[2:1] | DCREG[1:0] | LSbs of DCREG register |
| D[0] | MODREG[0] | LSb of MODREG register |

## DDM Status Register (DDMSTAT1), Address: H0x3E (Page 1)

| BIT | D[7:0] | DESCRIPTION |
|---|---|---|
| Bit Name | DDM_RSSI [15:8] | Reports upper byte of the measured value of RSSI. |
| Read/Write | Read only | |
| POR State | 00h | |

## DDM Status Register (DDMSTAT2), Address: H0x3F (Page 1)

| BIT | D[7:0] | DESCRIPTION |
|---|---|---|
| Bit Name | DDM_RSSI [7:0] | Reports lower byte of the measured value of RSSI. |
| Read/Write | Read only | |
| POR State | 00h | |

### DDM Status Register (DDMSTAT3), Address: H0x40 (Page 1)

| BIT | D[3:0] | DESCRIPTION |
|---|---|---|
| Bit Name | DDM_VCCX [11:8] | Reports upper nibble of the measured value of VCCX. The DDM_VCCX[11:0] value is unsigned with full scale of 4.658V. See the *Electrical Characteristics* for VCCX operational range. |
| Read/Write | Read only | |
| POR State | 00h | |

### DDM Status Register (DDMSTAT4), Address: H0x41 (Page 1)

| BIT | D[7:0] | DESCRIPTION |
|---|---|---|
| Bit Name | DDM_VCCX [7:0] | Reports lower byte of the measured value of VCCX. The DDM_VCCX[11:0] value is unsigned with full scale of 4.658V. See the *Electrical Characteristics* for VCCX operational range. |
| Read/Write | Read only | |
| POR State | 00h | |

### DDM Status Register (DDMSTAT5), Address: H0x42 (Page 1)

| BIT | D[3:0] | DESCRIPTION |
|---|---|---|
| Bit Name | DDM_VCCT [11:8] | Reports upper nibble of the measured value of VCCT. The DDM_VCCT[11:0] value is unsigned with full scale of 4.658V. See the *Electrical Characteristics* for VCCT operational range. |
| Read/Write | Read only | |
| POR State | 00h | |

### DDM Status Register (DDMSTAT6), Address: H0x43 (Page 1)

| BIT | D[7:0] | DESCRIPTION |
|---|---|---|
| Bit Name | DDM_VCCT [7:0] | Reports lower byte of the measured value of VCCT. The DDM_VCCT[11:0] value is unsigned with full scale of 4.658V. See the *Electrical Characteristics* for VCCT operational range. |
| Read/Write | Read only | |
| POR State | 00h | |

### DDM Status Register (DDMSTAT7), Address: H0x44 (Page 1)

| BIT | D[3:0] | DESCRIPTION |
|---|---|---|
| Bit Name | DDM_VCCTO [11:8] | Reports upper nibble of the measured value of VCCTO. The DDM_VCCTO[11:0] value is unsigned with full scale of 4.658V. See the *Electrical Characteristics* for VCCTO operational range. |
| Read/Write | Read only | |
| POR State | Hx00 | |

### DDM Status Register (DDMSTAT8), Address: H0x45 (Page 1)

| BIT | D[7:0] | DESCRIPTION |
|---|---|---|
| Bit Name | DDM_VCCTO [7:0] | Reports lower byte of the measured value of VCCTO. The DDM_VCCTO[11:0] value is unsigned with full scale of 4.658V. See the *Electrical Characteristics* for VCCTO operational range. |
| Read/Write | Read only | |
| POR State | 00h | |

## DDM Status Register (DDMSTAT9), Address: H0x46 (Page 1)

| BIT | D[3:0] | DESCRIPTION |
|---|---|---|
| Bit Name | DDM_BADC [11:8] | Reports upper nibble of the measured voltage value BADC pin. The DDM_BADC[11:0] value is unsigned with full scale of 1.164V. |
| Read/Write | Read only | |
| POR State | 00h | |

## DDM Status Register (DDMSTAT10), Address: H0x47 (Page 1)

| BIT | D[7:0] | DESCRIPTION |
|---|---|---|
| Bit Name | DDM_BADC [7:0] | Reports lower byte of the measured voltage value BADC pin. The DDM_BADC[11:0] value is unsigned with full scale of 1.164V. |
| Read/Write | Read only | |
| POR State | 00h | |

## DDM Status Register (DDMSTAT11), Address: H0x48 (Page 1)

| BIT | D[7:0] | DESCRIPTION |
|---|---|---|
| Bit Name | DDM_EXT_TSNS [15:8] | Reports upper byte of the measured value of external temperature sensor between the pins TSNS and TGND. This is the signed integer portion of the external temperature result (range: -128°C to +127°C). |
| Read/Write | Read only | |
| POR State | 00h | |

## DDM Status Register (DDMSTAT12), Address: H0x49 (Page 1)

| BIT | D[7:0] | DESCRIPTION |
|---|---|---|
| Bit Name | DDM_EXT_TSNS [7:0] | Reports lower byte of the measured voltage value of external temperature sensor between the pins TSNS and TGND. This is the fractional portion of the external temperature result (range: 0°C to 255/256°C). |
| Read/Write | Read only | |
| POR State | 00h | |

## DDM Status Register (DDMSTAT13), Address: H0x4A (Page 1)

| BIT | D[7:0] | DESCRIPTION |
|---|---|---|
| Bit Name | DDM_INT_TSNS [15:8] | Reports upper byte of the measured value of internal temperature sensor. This is the signed integer portion of the internal temperature result (range: -128°C to +127°C). |
| Read/Write | Read only | |
| POR State | 00h | |

## DDM Status Register (DDMSTAT14), Address: H0x4B (Page 1)

| BIT | D[7:0] | DESCRIPTION |
|---|---|---|
| Bit Name | DDM_INT_TSNS [7:0] | Reports lower byte of the measured voltage value of internal temperature sensor. This is the fractional portion of the internal temperature result (range: 0°C to 255/256°C). |
| Read/Write | Read only | |
| POR State | 00h | |

## DDM Status Register (DDMSTAT15), Address: H0x4C (Page 1)

| BIT | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|
| Bit Name | RES | DDM_TX_SHDN | RES | DDM_TIN_LOS | DDM_TXRPT[11] | DDM_TXRPT[10] | DDM_TXRPT[9] | DDM_TXRPT[8] |
| Read/Write | Read only | | | | | | | |
| POR State | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Reset Upon Read | No | No | No | No | No | No | No | No |

The DDMSTAT15 register is a status register showing flags with impact on digital monitors.

| BIT | NAME | DESCRIPTION |
|---|---|---|
| D[7] | RES | Reserved |
| D[6] | DDM_TX_SHDN | TX status flag<br>0 = normal operation (default)<br>1 = shut down (due to POR, FAULT, DISABLE, TX_EN=0, or XCVR_EN = 0) |
| D[5] | RES | Reserved |
| D[4] | DDM_TIN_LOS | Loss-of-signal at TIN<br>0 = deasserted (default)<br>1 = asserted |
| D[3:0] | DDM_TXRPT[11:8] | Reports the measured value of DC or average laser current. This is the upper nibble of TXB. These bits along with the lower byte in DDMSTAT16 make up the 12-bit value. |

## DDM Status Register (DDMSTAT16), Address: H0x4D (Page 1)

| BIT | D[7:0] | DESCRIPTION |
|---|---|---|
| Bit Name | DDM_TXRPT [7:0] | Reports lower byte of DC or average laser current. |
| Read/Write | Read only | The DDM_TXRPT_SEL bit in DDM_CTRL9 register selects whether DC or average laser |
| POR State | 00h | current is reported. |

## DDM Status Register (DDMSTAT17), Address: H0x4E (Page 1)

| BIT | D[3:0] | DESCRIPTION |
|---|---|---|
| Bit Name | DDM_TXP [11:8] | Reports the measured value of the monitor diode current which represents average laser |
| Read/Write | Read only | power. This is the upper nibble of the 12-bit value. |
| POR State | 00h | |

## DDM Status Register (DDMSTAT18), Address: H0x4F (Page 1)

| BIT | D[7:0] | DESCRIPTION |
|---|---|---|
| Bit Name | DDM_TXP [7:0] | Reports the measured value of the monitor diode current which represents average laser |
| Read/Write | Read only | power. This is the lower byte of the 12-bit value. |
| POR State | 00h | |

## DDM Status Register (DDMSTAT23), Address: H0x54 (Page 1)

| BIT | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|
| Bit Name | DDM_ TMAX | DDM_ TMIN | RES | DDM_ P2VFLAG | DDM_RSSI_ HI_FAIL | DDM_RSSI_ LO_FAIL | DDM_EXT_ T_FAIL | DDM_ LVFLAG |
| Read/Write | Read only | | | | | | | |
| POR State | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Reset Upon Read | Yes* | Yes* | No | Yes* | Yes* | Yes* | Yes* | Yes* |

*Sticky bit—Once flagged these registers remain flagged (logic 1) until they are read. Once read, they are reset to 0 if the source of the flag has been removed.

| BIT | NAME | DESCRIPTION |
|---|---|---|
| D[7] | DDM_TMAX | Interrupt: Internal temperature above +120°C.<br>0 = deasserted (default)<br>1 = asserted |
| D[6] | DDM_TMIN | Interrupt: Internal temperature below -50°C.<br>0 = deasserted (default)<br>1 = asserted |
| D[5] | RES | Reserved |
| D[4] | DDM_P2VFLAG | Interrupt: VCCX/VCCT vs. 2.1V<br>0 = deasserted (default)<br>1 = asserted |
| D[3] | DDM_RSSI_HI_FAIL | Interrupt: RSSI is stuck high.<br>0 = deasserted (default)<br>1 = asserted |
| D[2] | DDM_RSSI_LO_FAIL | Interrupt: RSSI is stuck low.<br>0 = deasserted (default)<br>1 = asserted |
| D[1] | DDM_EXT_T_FAIL | Interrupt: Status indicating that the external temperature sense has failed. When this condition occurs, the external temperature is forced to -128°C.<br>0 = deasserted (default)<br>1 = asserted |
| D[0] | DDM_LVFLAG | Interrupt: Supply voltage too low for accurate DDM measurement.<br>0 = deasserted (default)<br>1 = asserted |

## Layout Considerations

The high-speed data inputs and outputs are the most criti-
cal paths for the device, and great care should be taken
to minimize discontinuities on these transmission lines
between the connector and the IC. The following are some
suggestions for maximizing the device's performance:

• The data inputs should be wired directly between the
connector and IC without stubs.

• The data transmission lines to the laser should be
kept as short as possible, and the impedance of the
transmission lines must be considered part of the
laser matching network.

• An uninterrupted ground plane should be positioned
beneath the high-speed I/Os.

• Ground path vias should be placed close to the IC
and the input/output interfaces to allow a return cur-
rent path to the IC and the laser.

• Maintain 100Ω differential transmission line imped-
ance for the RIN, ROUT, and TIN I/Os.

• The data transmission lines to the laser should be
kept as short as possible, and must be designed for
50Ω differential or 25Ω single-ended characteristic
impedance.

• Use good high-frequency layout techniques and mul-
tilayer boards with an uninterrupted ground plane to
minimize EMI and crosstalk.

Refer to the schematic and board layers of the HFRD-67
reference design data sheet for more information.

## Exposed-Pad Package and Thermal Consider-ations

The exposed pad on the MAX3956 is the only electrical
connection to ground and provides a very low-thermal
resistance path for heat removal from the IC. The pad
is also electrical ground on the device and must be sol-
dered to the circuit board ground for proper thermal and
electrical performance. Refer to Application Note 862:
HFAN-08.1: *Thermal Considerations of QFN and Other
Exposed-Paddle Packages* for additional information.

## Typical Application Circuit
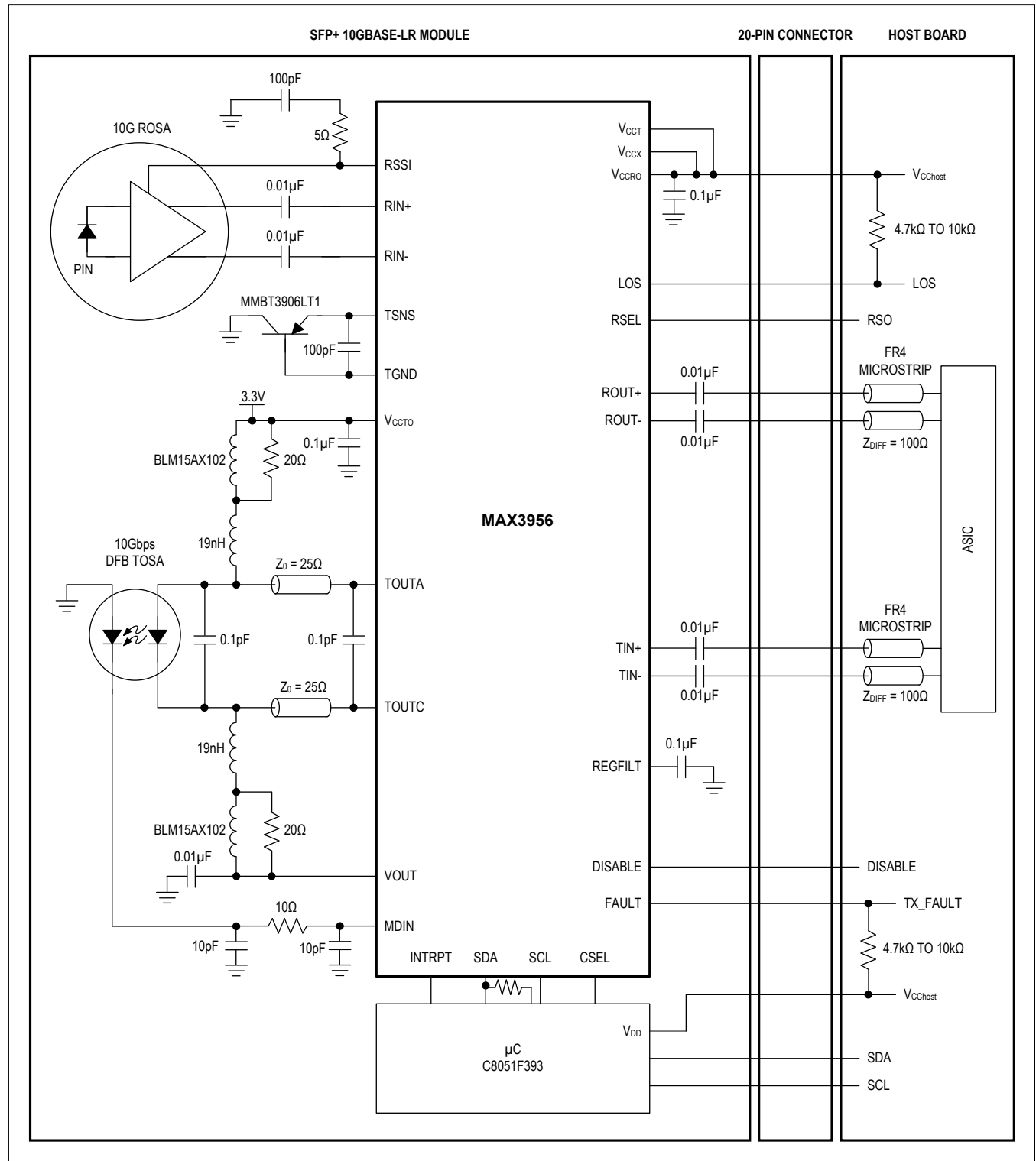
## Ordering Information

| PART | TEMP RANGE | PIN-PACKAGE |
|---|---|---|
| MAX3956ETJ+ | -40°C to +85°C | 32 TQFN-EP* |

**Note:** *Parts are guaranteed by design and characterization to operate over the -40°C to +95°C ambient temperature range ($T_A$) and are tested up to +95°C.*

*+Denotes a lead(Pb)-free/RoHS-compliant package.*

*\*Exposed pad.*

## Chip Information

PROCESS: BiCMOS

## Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

| PACKAGE TYPE | PACKAGE CODE | OUTLINE NO. | LAND PATTERN NO. |
|---|---|---|---|
| 32 TQFN-EP | T3255+3 | 21-0140 | 90-0001 |

## Revision History

| REVISION NUMBER | REVISION DATE | DESCRIPTION | PAGES CHANGED |
|---|---|---|---|
| 0 | 8/13 | Initial release | — |
| 1 | 2/14 | Fixed errors in *Electrical Characteristics*, *Detailed Description*, Figure 7, Figure 8, Figure 14, Table 11, DDM Control Register tables, *Design Procedure*, Fault Mask Control Register, DDM Status Register tables, and *Typical Application Circuit* | 7, 22, 26, 27, 35, 41, 43, 44, 50, 53, 75, 76, 80 |
| 2 | 6/14 | Fixed errors in *Electrical Characteristics*, *Power-On-Reset (POR)* section, Figure 18, and the *MAX3956 Mode Control Register, DDM Control Register, Fault Mask Control Register, Transmitter Status Register* tables, and *Typical Application Circuit* | 6, 27, 38, 42, 44, 53, 72, 80 |
| 3 | 9/14 | Updated the *Electrical Characteristics* and added TOC27 to *Typical Operating Characteristics* | 2, 11 |

## Данный компонент на территории Российской Федерации

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