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June 2014

FDMA410NZ

Single N-Channel 1.5 V Specified PowerTrench® MOSFET 20 V, 9.5 A, 23 m Ω

Features

- Max $r_{DS(on)}$ = 23 m Ω at V_{GS} = 4.5 V, I_D = 9.5 A
- Max $r_{DS(on)}$ = 29 m Ω at V_{GS} = 2.5 V, I_D = 8.0 A
- Max $r_{DS(on)}$ = 36 m Ω at V_{GS} = 1.8 V, I_D = 4.0 A
- Max $r_{DS(on)}$ = 50 m Ω at V_{GS} = 1.5 V, I_D = 2.0 A
- HBM ESD protection level > 2.5 kV (Note 3)
- Low Profile-0.8 mm maximum in the new package MicroFET 2x2 mm
- Free from halogenated compounds and antimony oxides
- RoHS Compliant

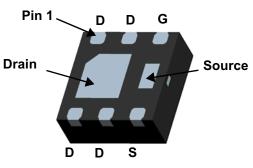


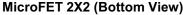
General Description

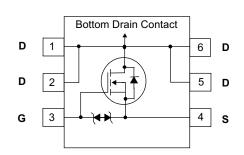
This Single N-Channel MOSFET has been designed using Fairchild Semiconductor's advanced Power Trench process to optimize the $r_{\text{DS}(\text{ON})}$ @ V_{GS} = 1.5 V on special MicroFET leadframe.

Applications

- Li-Ion Battery Pack
- Baseband Switch
- Load Switch
- DC-DC Conversion







MOSFET Maximum Ratings T_A = 25 °C unless otherwise noted

Symbol	Param	Parameter			
V _{DS}	Drain to Source Voltage			20	V
V_{GS}	Gate to Source Voltage			±8	V
ı	-Continuous	T _A = 25 °C	(Note 1a)	9.5	
l _D	-Pulsed			24	A
Ъ	Power Dissipation	T _A = 25 °C	(Note 1a)	2.4	w
P _D	Power Dissipation	T _A = 25 °C	(Note 1b)	0.9	\ \v
T _J , T _{STG}	Operating and Storage Junction Tempera	ature Range		-55 to +150	°C

Thermal Characteristics

$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1a)	52	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1b)	145	C/VV

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
410	FDMA410NZ	MicroFET 2X2	7 "	8 mm	3000 units

Electrical Characteristics T_J = 25 °C unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Тур	Max	Units
Off Chara	cteristics					
BV _{DSS}	Drain to Source Breakdown Voltage	I _D = 250 μA, V _{GS} = 0 V	20			V
$\frac{\Delta BV_{DSS}}{\Delta T_{J}}$	Breakdown Voltage Temperature Coefficient	I _D = 250 μA, referenced to 25 °C		17		mV/°C
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} = 16 V, V _{GS} = 0 V			1	μΑ
I _{GSS}	Gate to Source Leakage Current	V _{GS} = ±8 V, V _{DS} = 0 V			±10	μΑ

On Characteristics

V _{GS(th)}	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}, I_{D} = 250 \mu A$	0.4	0.7	1.0	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	I _D = 250 μA, referenced to 25 °C		-3		mV/°C
		$V_{GS} = 4.5 \text{ V}, I_D = 9.5 \text{ A}$		17	23	
	Static Drain to Source On Resistance	$V_{GS} = 2.5 \text{ V}, I_D = 8.0 \text{ A}$		20	29	
r		$V_{GS} = 1.8 \text{ V}, I_D = 4.0 \text{ A}$		24	36	$m\Omega$
r _{DS(on)}	Statio Brain to Godroe On Resistance	$V_{GS} = 1.5 \text{ V}, I_D = 2.0 \text{ A}$		29	50	11132
		$V_{GS} = 4.5 \text{ V}, I_D = 9.5 \text{ A},$ $T_J = 125 ^{\circ}\text{C}$		23	32	
9 _{FS}	Forward Transconductance	$V_{DD} = 5 \text{ V}, I_{D} = 9.5 \text{ A}$		35		S

Dynamic Characteristics

C _{iss}	Input Capacitance	V 40.V.V. 0.V.		815	1080	pF
C _{oss}	Output Capacitance	V _{DS} = 10 V, V _{GS} = 0 V, f = 1 MHz		130	175	pF
C _{rss}	Reverse Transfer Capacitance	1 - 1 WILIZ		85	130	pF
R_g	Gate Resistance	f = 1 MHz		2.1		Ω

Switching Characteristics

t _{d(on)}	Turn-On Delay Time		7.5	15	ns
t _r	Rise Time	V _{DD} = 10 V, I _D = 9.5 A,	3.9	10	ns
t _{d(off)}	Turn-Off Delay Time	$V_{GS} = 4.5 \text{ V}, R_{GEN} = 6 \Omega$	27	44	ns
t _f	Fall Time		3.7	10	ns
Q_g	Total Gate Charge	V 45V V 40V	10	14	nC
Q _{gs}	Gate to Source Charge	V _{GS} = 4.5 V , V _{DD} = 10 V, I _D = 9.5 A	1.2		nC
Q_{gd}	Gate to Drain "Miller" Charge	ID = 3.3 A	2.0		nC

Drain-Source Diode Characteristics

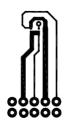
Is	Maximum Continuous Drain-Source Diode I	Maximum Continuous Drain-Source Diode Forward Current			2.0	Α
V_{SD}	Source to Drain Diode Forward Voltage $V_{GS} = 0 \text{ V}, I_S = 2.0 \text{ A}$ (Note 2)			0.7	1.2	V
t _{rr}	Reverse Recovery Time	I _F = 9.5 A, di/dt = 100 A/μs		12	22	ns
Q _{rr}	Reverse Recovery Charge	- 1 _F - 9.5 A, α//αι - 100 A/μS		2.6	10	nC

NOTES:

^{1.} $R_{\theta JA}$ is determined with the device mounted on a 1 in 2 pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta JA}$ is determined by the user's board design.



a.52 °C/W when mounted on a 1 in² pad of 2 oz copper.



b. 145 °C/W when mounted on a minimum pad of 2 oz copper.

^{2.} Pulse Test: Pulse Width < 300 μ s, Duty cycle < 2.0%.

^{3.} The diode connected between the gate and source serves only as protection against ESD. No gate overvoltage rating is implied.

Typical Characteristics $T_J = 25$ °C unless otherwise noted

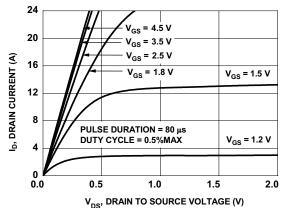


Figure 1. On-Region Characteristics

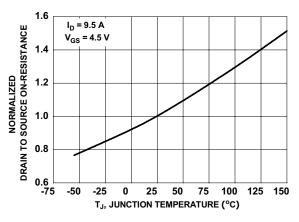


Figure 3. Normalized On-Resistance vs Junction Temperature

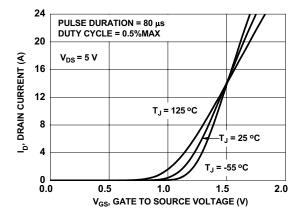


Figure 5. Transfer Characteristics

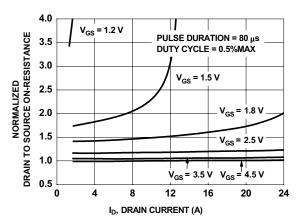


Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

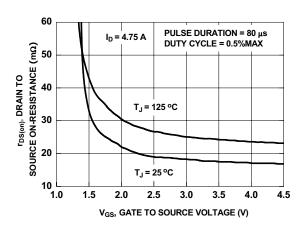


Figure 4. On-Resistance vs Gate to Source Voltage

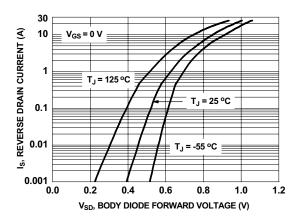


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

Typical Characteristics $T_J = 25$ °C unless otherwise noted

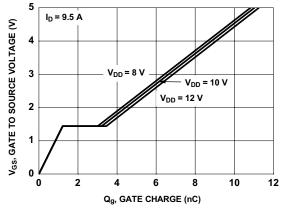


Figure 7. Gate Charge Characteristics

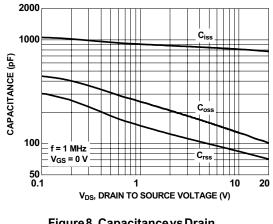


Figure 8. Capacitance vs Drain to Source Voltage

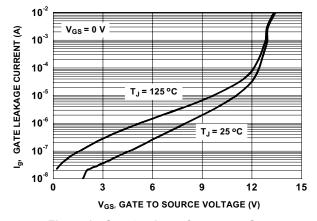


Figure 9. Gate Leakage Current vs Gate to Source Voltage

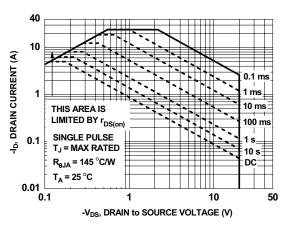


Figure 10. Forward Bias Safe Operation Area

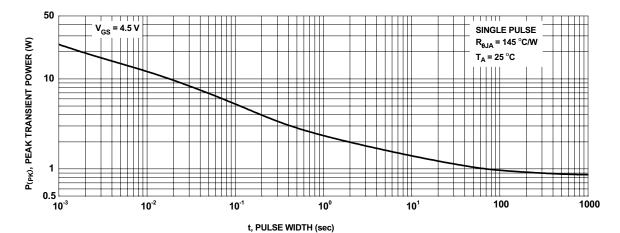


Figure 11. Single Pulse Maximum Power Dissipation

Typical Characteristics T_J = 25 °C unless otherwise noted

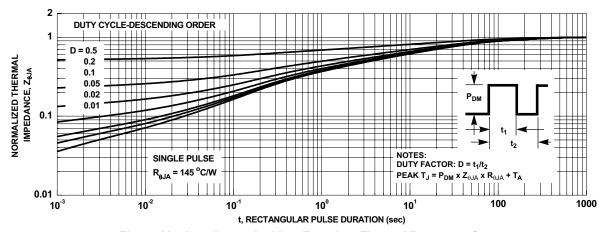
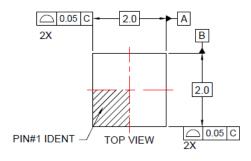
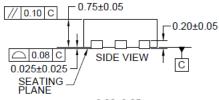
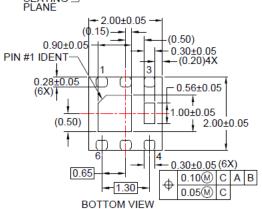


Figure 12. Junction-to-Ambient Transient Thermal Response Curve

Dimensional Outline and Pad Layout

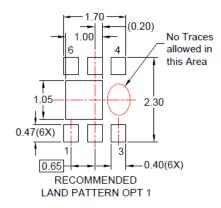


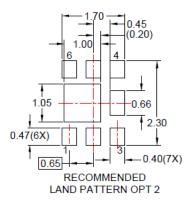




NOTES:

- A. PACKAGE DOES NOT FULLY CONFORM TO JEDEC MO-229 REGISTRATION
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 2009.
- D. LAND PATTERN RECOMMENDATION IS EXISTING INDUSTRY LAND PATTERN.
- E. DRAWING FILENAME: MKT-MLP06Lrev4.







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