# HIGH POWER SPDT SWITCH GaAs MMIC

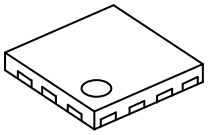
## ■ GENERAL DESCRIPTION

The NJG1681MD7 is a GaAs SPDT switch MMIC suitable for LTE/UMTS/CDMA/GSM applications.

The NJG1681MD7 features very low insertion loss, high isolation and excellent linearity performance down to 1.8V control voltage at high frequency up to 6GHz. In addition, this switch is able to handle high power signals.

The NJG1681MD7 has ESD protection devices to achieve excellent ESD performances. No DC Blocking capacitors are required for all RF ports unless DC is biased externally. And the ultra small & ultra thin EQFN14-D7 package is adopted.

## ■ PACKAGE OUTLINE



NJG1681MD7

## ■ APPLICATIONS

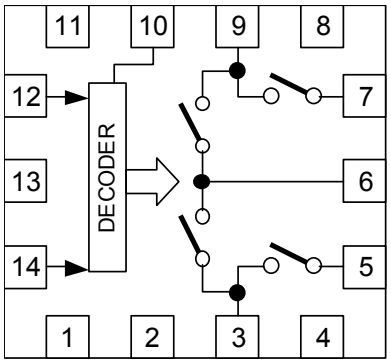
LTE, UMTS, CDMA, GSM applications
Post PA switching, antenna switching, bands switching, and general purpose switching applications
IEEE 802.11p applications

## ■ FEATURES

| | |
|---|---|
| ● Low voltage logic control | $V_{CTL(H)}$=1.8V typ. |
| ● Low voltage operation | $V_{DD}$=2.7V typ. |
| ● Low distortion | IIP3=+73dBm typ. @f=829+849MHz, $P_{IN}$=24dBm |
| | IIP3=+71dBm typ. @f=1870+1910MHz, $P_{IN}$=24dBm |
| | 2nd harmonics=-85dBc typ. @ f=0.9GHz, $P_{IN}$=35dBm |
| | 3rd harmonics=-90dBc typ. @ f=0.9GHz, $P_{IN}$=35dBm |
| ● High linearity | P-0.1dB=+36dBm min. |
| ● Low insertion loss | 0.18dB typ. @f=0.9GHz, $P_{IN}$=35dBm |
| | 0.20dB typ. @f=1.9GHz, $P_{IN}$=33dBm |
| | 0.23dB typ. @f=2.7GHz, $P_{IN}$=27dBm |
| ● Ultra small & ultra thin package | EQFN14-D7 (Package size: 1.6 x 1.6 x 0.397mm.) |
| ● RoHS compliant and Halogen Free, MSL1 | |

## ■ PIN CONFIGURATION

(TOP VIEW)




Pin connection

| | |
|---|---|
| 1. GND | 8. GND |
| 2. NC(GND) | 9. P1 |
| 3. P2 | 10. GND |
| 4. GND | 11. GND |
| 5. GND | 12. VDD |
| 6. PC | 13. NC(GND) |
| 7. GND | 14. VCTL |

Exposed PAD: GND

## ■ TRUTH TABLE

"H"=$V_{CTL(H)}$, "L"=$V_{CTL(L)}$

| VCTL | Path |
|---|---|
| H | PC-P1 |
| L | PC-P2 |

NOTE: Please note that any information on this datasheet will be subject to change.

## ■ ABSOLUTE MAXIMUM RATINGS

($T_a$=+25°C, $Z_s$=$Z_l$=50Ω)

| PARAMETER | SYMBOL | CONDITIONS | RATINGS | UNITS |
|---|---|---|---|---|
| RF Input Power | $P_{IN}$ | $V_{DD}$ =2.7V | 37 | dBm |
| Supply Voltage | $V_{DD}$ | | 5.0 | V |
| Control Voltage | $V_{CTL}$ | | 5.0 | V |
| Power Dissipation | $P_D$ | Four-layer FR4 PCB with through-hole (74.2x74.2mm), Tj=150°C | 1300 | mW |
| Operating Temp. | $T_{opr}$ | | -40~+85 | °C |
| Storage Temp. | $T_{stg}$ | | -55~+150 | °C |

## ■ ELECTRICAL CHARACTERISTICS 1 (DC)

(General conditions: $T_a$=+25°C, $V_{DD}$=2.7V, $V_{CTL(L)}$=0V, $V_{CTL(H)}$=1.8V)

| PARAMETERS | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| Supply Voltage | $V_{DD}$ | | 2.375 | 2.7 | 5.0 | V |
| Operating Current | $I_{DD}$ | No RF input, $V_{DD}$=2.7V | - | 95 | 180 | μA |
| Control Voltage (LOW) | $V_{CTL(L)}$ | | 0 | - | 0.45 | V |
| Control Voltage (HIGH) | $V_{CTL(H)}$ | | 1.35 | 1.8 | 5.0 | V |
| Control Current | $I_{CTL}$ | $V_{CTL(H)}$=1.8V | - | 4 | 10 | μA |

■ **ELECTRICAL CHARACTERISTICS 2 (RF)**

(General conditions: $T_a$=+25°C, $Z_s$=$Z_l$=50Ω, $V_{DD}$=2.7V, $V_{CTL(L)}$=0V, $V_{CTL(H)}$=1.8V)

| PARAMETERS | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| Insertion Loss 1 | LOSS1 | f=0.9GHz, $P_{IN}$=35dBm | - | 0.18 | 0.33 | dB |
| Insertion Loss 2 | LOSS2 | f=1.9GHz, $P_{IN}$=33dBm | - | 0.20 | 0.40 | dB |
| Insertion Loss 3 | LOSS3 | f=2.7GHz, $P_{IN}$=27dBm | - | 0.23 | 0.43 | dB |
| Insertion Loss 4 | LOSS4 | f=6.0GHz, $P_{IN}$=27dBm | - | 0.45 | 0.65 | dB |
| Isolation 1 | ISL1 | f=0.9GHz, $P_{IN}$=35dBm | 40 | 45 | - | dB |
| Isolation 2 | ISL2 | f=1.9GHz, $P_{IN}$=33dBm | 30 | 35 | - | dB |
| Isolation 3 | ISL3 | f=2.7GHz, $P_{IN}$=27dBm | 25 | 30 | - | dB |
| Isolation 4 | ISL4 | f=6.0GHz, $P_{IN}$=27dBm | 16.5 | 20 | - | dB |
| Input Power at 0.1dB Compression Point1 | $P_{-0.1dB}1$ | f=0.9GHz, 1.9GHz, 2.7GHz | +36 | - | - | dBm |
| Input Power at 0.1dB Compression Point2 | $P_{-0.1dB}2$ | f=6.0GHz | +36 | - | - | dBm |
| 2nd Harmonics 1 | 2fo(1) | f=0.9GHz, $P_{IN}$=35dBm | - | -85 | -70 | dBc |
| 2nd Harmonics 2 | 2fo(2) | f=1.9GHz, $P_{IN}$=33dBm | - | -90 | -70 | dBc |
| 2nd Harmonics 3 | 2fo(3) | f=2.7GHz, $P_{IN}$=27dBm | - | -90 | -70 | dBc |
| 3rd Harmonics 1 | 3fo(1) | f=0.9GHz, $P_{IN}$=35dBm | - | -90 | -70 | dBc |
| 3rd Harmonics 2 | 3fo(2) | f=1.9GHz, $P_{IN}$=33dBm | - | -80 | -70 | dBc |
| 3rd Harmonics 3 | 3fo(3) | f=2.7GHz, $P_{IN}$=27dBm | - | -90 | -70 | dBc |
| Input 3rd order intercept point1 | IIP3(1) | f=829+849MHz, $P_{IN}$=24dBm each | +65 | +73 | - | dBm |
| Input 3rd order intercept point2 | IIP3(2) | f=1870+1910MHz, $P_{IN}$=24dBm each | +65 | +71 | - | dBm |
| VSWR1 | VSWR1 | on-state ports, f=2.7GHz | - | 1.1 | 1.4 | |
| VSWR2 | VSWR2 | on-state ports, f=6.0GHz | - | 1.1 | 1.4 | |
| Switching time | $T_{SW}$ | 50% $V_{CTL}$ to 10/90% RF | - | 1 | 5 | μs |

*1: IIP3 are defined by the following equations.
IIP3=(3 x Pout-IM3)/2+LOSS

■ **TERMINAL INFORMATION**

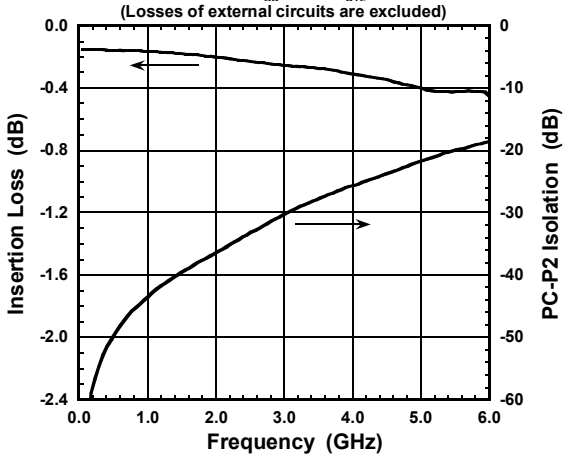
| No. | SYMBOL | DESCRIPTION |
|---|---|---|
| 1 | GND | Ground terminal. Please connect this terminal with ground plane as close as possible for excellent RF performance. |
| 2 | NC(GND) | Ground terminal. Please connect this terminal with ground plane as close as possible for excellent RF performance. |
| 3 | P2 | RF transmitting/receiving port. No DC blocking capacitor is required for this port unless DC is biased externally. |
| 4 | GND | Ground terminal. Please connect this terminal with ground plane as close as possible for excellent RF performance. |
| 5 | GND | Ground terminal. Please connect this terminal with ground plane as close as possible for excellent RF performance. |
| 6 | PC | RF transmitting/receiving port. No DC blocking capacitor is required for this port unless DC is biased externally. Please connect an inductor with GND terminal for ESD protection. |
| 7 | GND | Ground terminal. Please connect this terminal with ground plane as close as possible for excellent RF performance. |
| 8 | GND | Ground terminal. Please connect this terminal with ground plane as close as possible for excellent RF performance. |
| 9 | P1 | RF transmitting/receiving port. No DC blocking capacitor is required for this port unless DC is biased externally. |
| 10 | GND | Ground terminal. Please connect this terminal with ground plane as close as possible for excellent RF performance. |
| 11 | GND | Ground terminal. Please connect this terminal with ground plane as close as possible for excellent RF performance. |
| 12 | VDD | Positive voltage supply terminal. The positive voltage (+2.375~+5V) has to be supplied. Please connect a bypass capacitor with GND terminal for excellent RF performance. |
| 13 | NC(GND) | Ground terminal. Please connect this terminal with ground plane as close as possible for excellent RF performance. |
| 14 | VCTL | Control signal input terminal. This terminal is set to High-Level (+1.35~+5.0V) or Low-Level (0~+0.45V). |
| Exposed Pad | GND | Ground terminal. |

■ **ELECTRICAL CHARACTERISTICS** (With application circuit)

**Loss, ISL vs Frequency**

(PC-P1 ON, $V_{DD}$=2.7V, $V_{CTL}$=1.8V)

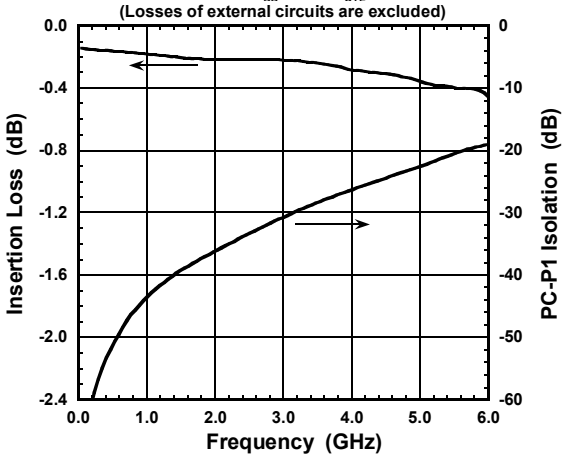
(Losses of external circuits are excluded)




**Loss, ISL vs Frequency**

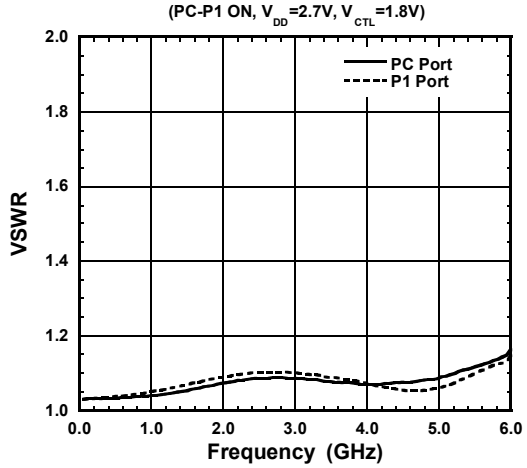
(PC-P2 ON, $V_{DD}$=2.7V, $V_{CTL}$=0V)

(Losses of external circuits are excluded)



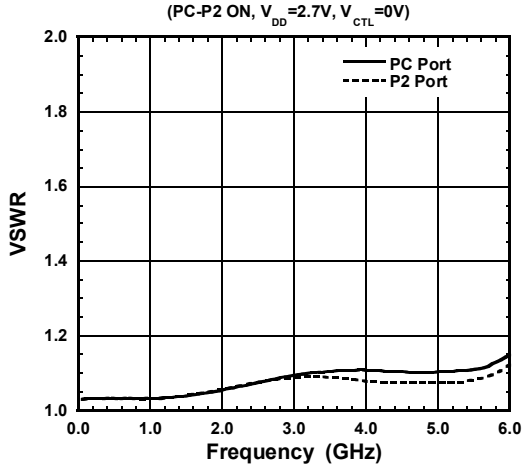

**VSWR vs Frequency**

(PC-P1 ON, $V_{DD}$=2.7V, $V_{CTL}$=1.8V)



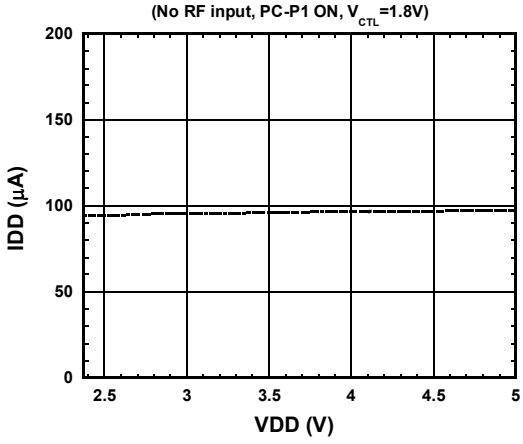

**VSWR vs Frequency**

(PC-P2 ON, $V_{DD}$=2.7V, $V_{CTL}$=0V)



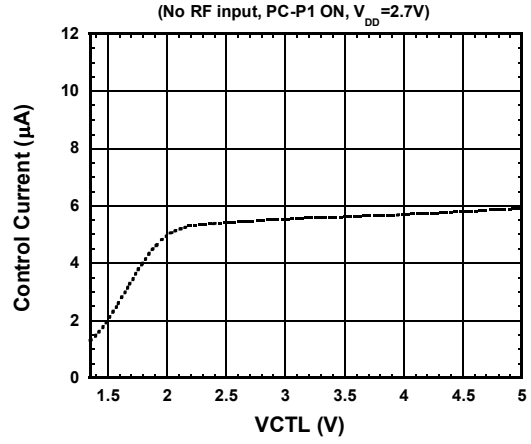

**IDD vs. VDD**

(No RF input, PC-P1 ON, $V_{CTL}$=1.8V)




**Control Current vs. VCTL**

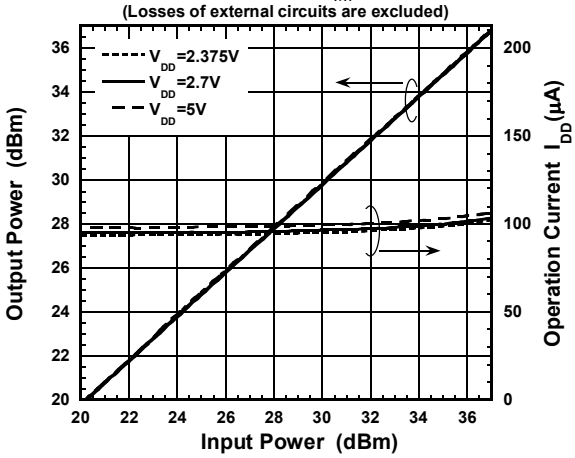
(No RF input, PC-P1 ON, $V_{DD}$=2.7V)



■ **ELECTRICAL CHARACTERISTICS** (With application circuit)

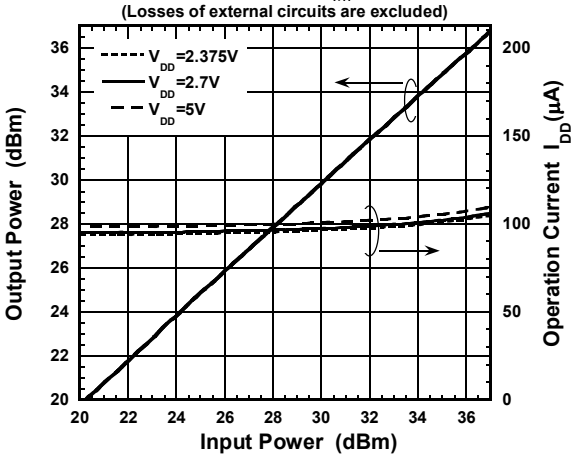
**Output Power, $I_{DD}$ vs Input Power**

(f=0.9GHz, PC-P1 ON, $V_{CTL}$=1.8V)
(Losses of external circuits are excluded)



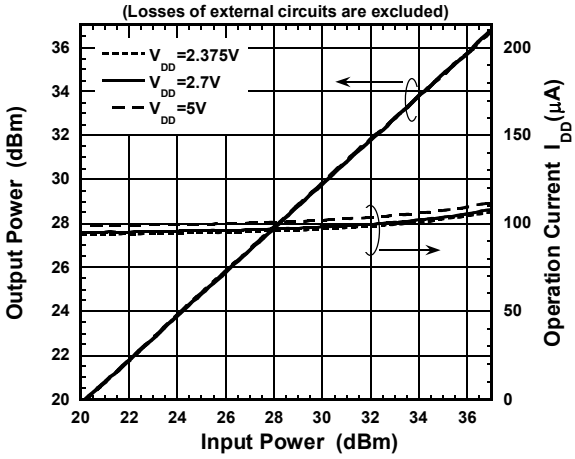

**Output Power, $I_{DD}$ vs Input Power**

(f=1.9GHz, PC-P1 ON, $V_{CTL}$=1.8V)
(Losses of external circuits are excluded)



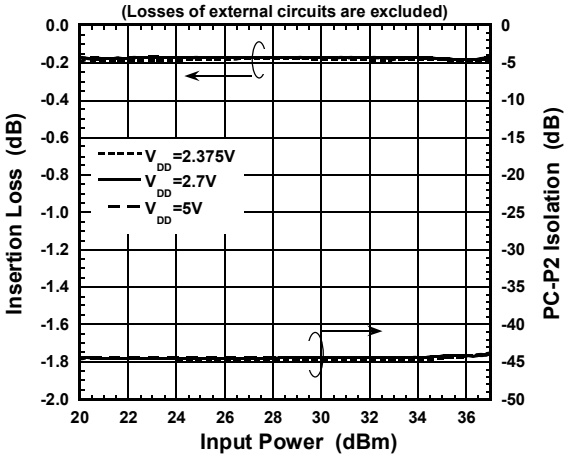

**Output Power, $I_{DD}$ vs Input Power**

(f=2.7GHz, PC-P1 ON, $V_{CTL}$=1.8V)
(Losses of external circuits are excluded)



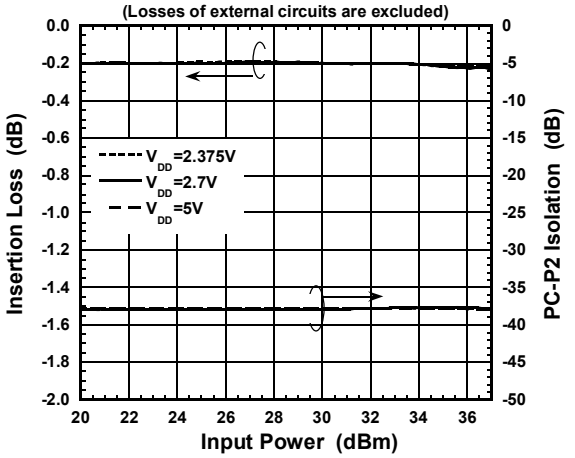

**Loss, ISL vs Input Power**

(f=0.9GHz, PC-P1 ON, $V_{CTL}$=1.8V)
(Losses of external circuits are excluded)



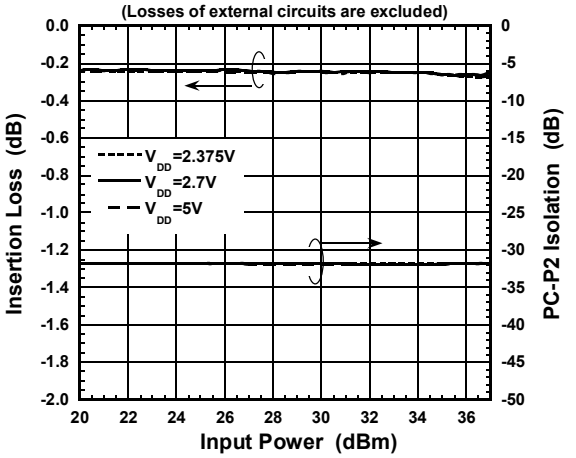

**Loss, ISL vs Input Power**

(f=1.9GHz, PC-P1 ON, $V_{CTL}$=1.8V)
(Losses of external circuits are excluded)




**Loss, ISL vs Input Power**

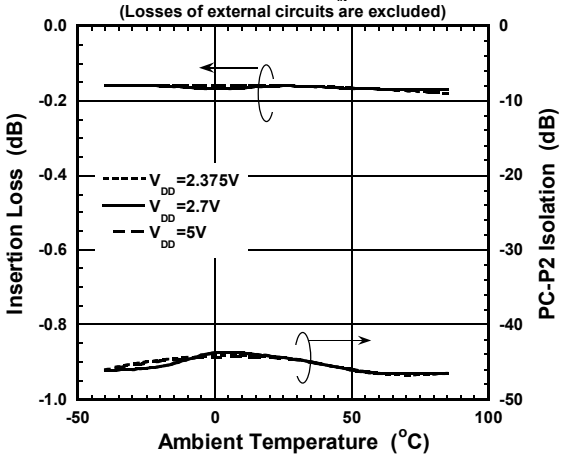
(f=2.7GHz, PC-P1 ON, $V_{CTL}$=1.8V)
(Losses of external circuits are excluded)



■ **ELECTRICAL CHARACTERISTICS** (With application circuit)

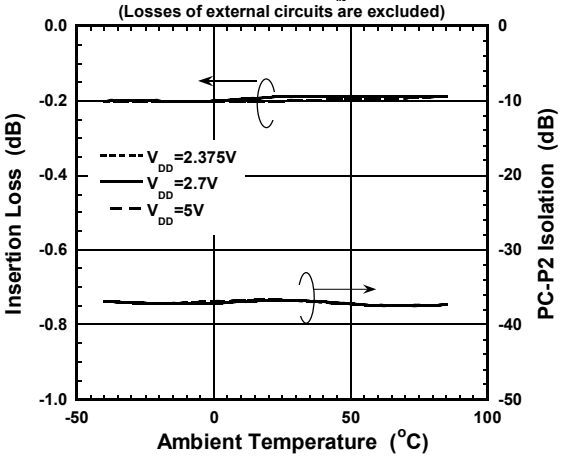
**Loss, ISL vs Ambient Temperature**

(f=0.9GHz, PC-P1 ON, $P_{IN}$=35dBm)
(Losses of external circuits are excluded)



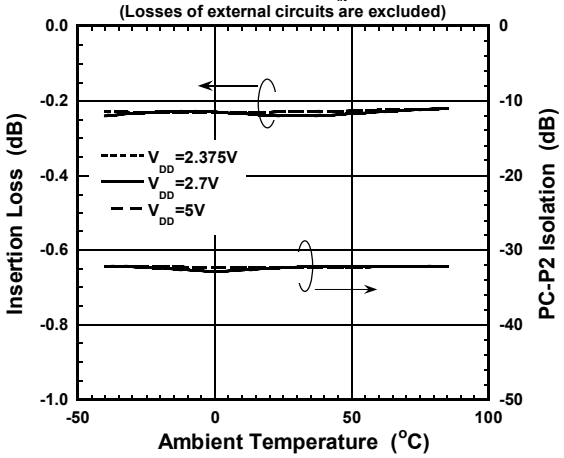

**Loss, ISL vs Ambient Temperature**

(f=1.9GHz, PC-P1 ON, $P_{IN}$=33dBm)
(Losses of external circuits are excluded)



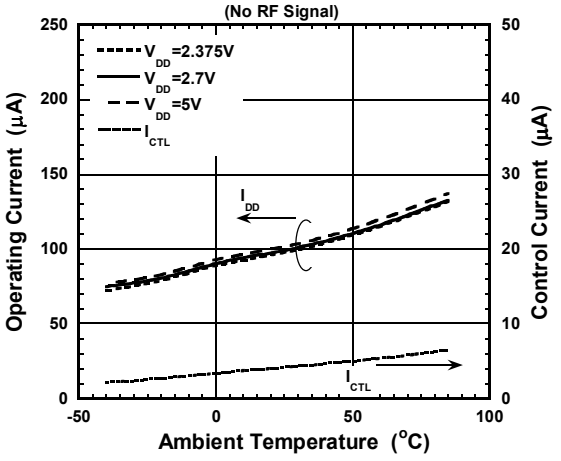

**Loss, ISL vs Ambient Temperature**

(f=2.7GHz, PC-P1 ON, $P_{IN}$=27dBm)
(Losses of external circuits are excluded)



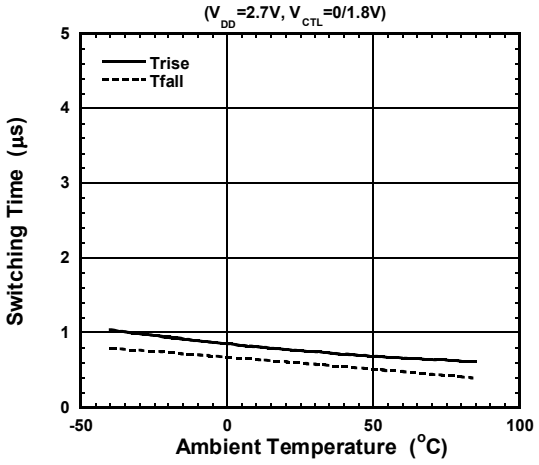

**DC Current vs Ambient Temperature**

(No RF Signal)

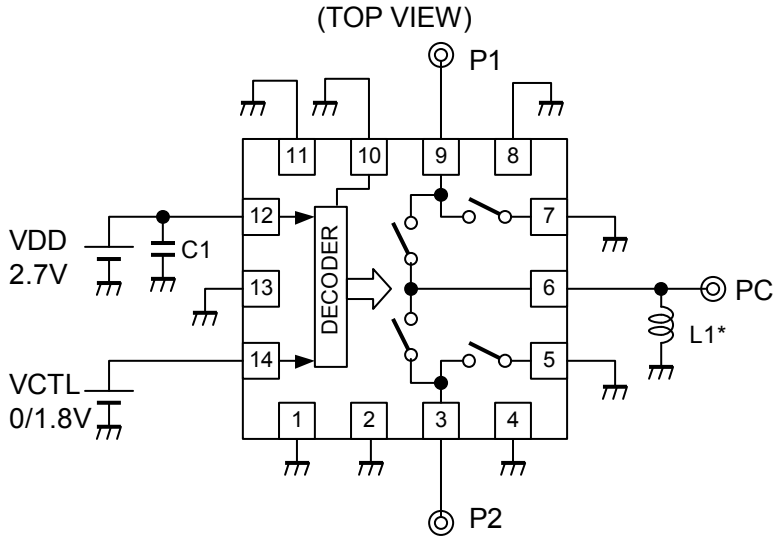



**Switching Time vs Ambient Temperature**

($V_{DD}$=2.7V, $V_{CTL}$=0/1.8V)



## ■ APPLICATION CIRCUIT




Note: No DC blocking capacitors are required on all RF ports, unless DC is biased externally.

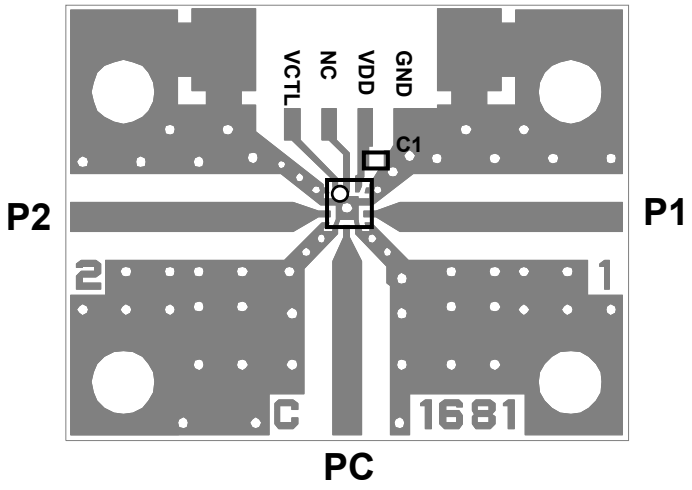
* The Inductor L1 is required for enhancing ESD protection level.
The inductor L1 is recommended in order to keep the DC bias level of each RF port at 0 V level tightly.

## ■ PARTS LIST

| No. | Parameters | Note |
|---|---|---|
| C1 | 1000pF | MURATA (GRM15) |
| L1 | 68nH | TAIYO-YUDEN (HK1005) |

## ■ PCB LAYOUT

(TOP VIEW)




PCB SIZE: 19.4 x 15.0 mm
PCB: FR-4, t=0.5mm
Capacitor size: 1005
MICROSTRIP LINE WIDTH: 0.98mm

Losses of PCB and connectors, Ta=+25°C

| Frequency (GHz) | Loss (dB) |
|---|---|
| 0.9 | 0.09 |
| 1.9 | 0.18 |
| 2.7 | 0.26 |
| 6.0 | 0.48 |

## ■ PRECAUTIONS

[1] No DC blocking capacitors are required at each RF port normally. When the other device is biased at certain voltage and connected to the NJG1681MD7, a DC block capacitor is required between the device and the switch IC. This is because the each RF port of NJG1681MD7 is biased at 0 V (GND).
[2] For avoiding the degradation of RF performance, the bypass capacitor (C1) should be placed as close as possible to VDD terminal
[3] For good RF performance, all GND terminals are must be connected to PCB ground plane of substrate, and through - holes for GND should be placed the IC near.

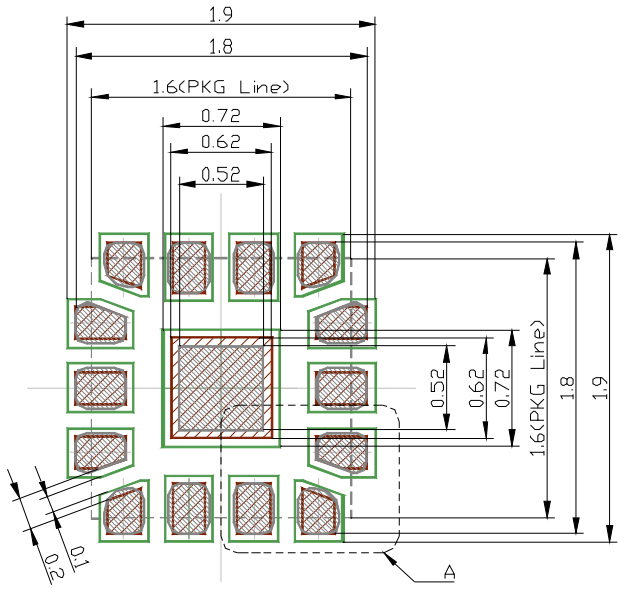
## ■ RECOMMENDED FOOTPRINT PATTERN (EQFN14-D7 PACKAGE Reference)

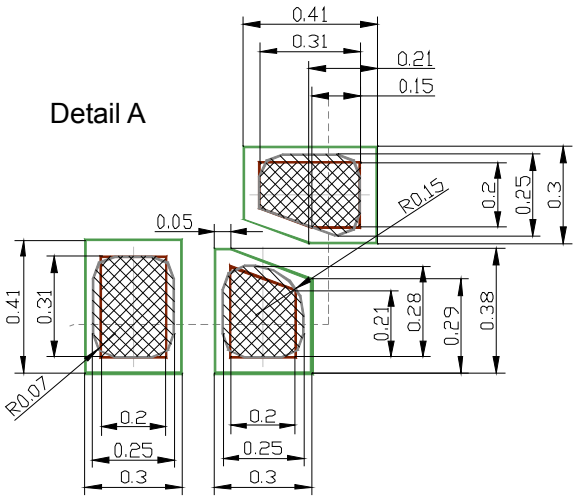
: Land

: Mask (Open area)  *Metal mask thickness : 100μm

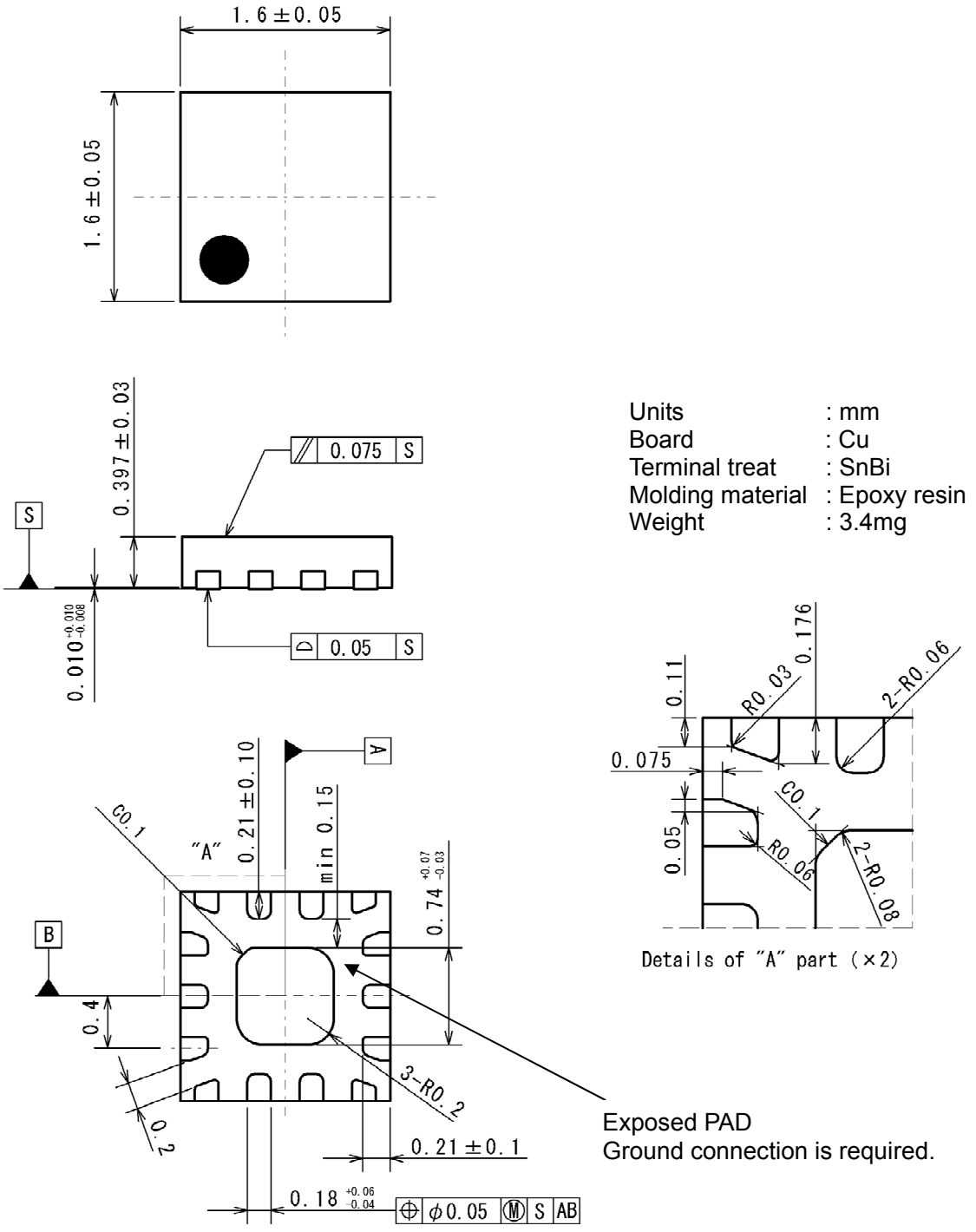
: Resist(Open area)

PKG:  1.6mm x 1.6mm
Pin pitch: 0.4mm



## ■ PACKAGE OUTLINE (EQFN14-D7)




| | |
|---|---|
| Units | : mm |
| Board | : Cu |
| Terminal treat | : SnBi |
| Molding material | : Epoxy resin |
| Weight | : 3.4mg |

**Cautions on using this product**

This product contains Gallium-Arsenide (GaAs) which is a harmful material.

- Do NOT eat or put into mouth.
- Do NOT dispose in fire or break up this product.
- Do NOT chemically make gas or powder with this product.
- To waste this product, please obey the relating law of your country.

This product may be damaged with electric static discharge (ESD) or spike voltage. Please handle with care to avoid these damages.

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NJR:

NJG1681MD7

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Адрес: 105318, г.Москва, ул.Щербаковская д.3, офис 1107

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Сотрудничество с глобальными дистрибьюторами электронных компонентов, предоставляет возможность заказывать и получать с международных складов практически любой перечень компонентов в оптимальные для Вас сроки.

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