

# KAI-02050

## 1600 (H) x 1200 (V) Interline CCD Image Sensor

### Description

The KAI-02050 Image Sensor is a 2-megapixel CCD in a 2/3" optical format. Based on the TRUESENSE 5.5 micron Interline Transfer CCD Platform, the sensor features broad dynamic range, excellent imaging performance, and a flexible readout architecture that enables use of 1, 2, or 4 outputs for full resolution readout up to 68 frames per second. A vertical overflow drain structure suppresses image blooming and enables electronic shuttering for precise exposure control. Other features include low dark current, negligible lag, and low smear.

The sensor shares common PGA pin-out and electrical configurations with other devices based on the TRUESENSE 5.5 micron Interline Transfer CCD Platform, allowing a single camera design to support multiple members of this sensor family.

Table 1. GENERAL SPECIFICATIONS

| Parameter   | Typical Value  |
|---|--|
| Architecture  | Interline CCD, Progressive Scan                                    |
| Total Number of Pixels  | 1684 (H) x 1264 (V)  |
| Number of Effective Pixels  | 1640 (H) x 1240 (V)  |
| Number of Active Pixels   | 1600 (H) x 1200 (V)  |
| Pixel Size  | 5.5 $\mu\text{m}$ (H) x 5.5 $\mu\text{m}$ (V)                      |
| Active Image Size   | 8.8 mm (H) x 6.6 mm (V)<br>11.0 mm (diagonal), 2/3" Optical Format |
| Aspect Ratio  | 4:3  |
| Number of Outputs   | 1, 2, or 4   |
| Charge Capacity   | 20,000 electrons   |
| Output Sensitivity  | 34 $\mu\text{V}/\text{e}^-$  |
| Quantum Efficiency<br>Mono (-ABA)<br>R, G, B (-FBA)<br>R, G, B (-CBA) | 44%<br>29%, 37%, 39%<br>31%, 37%, 38%                              |
| Read Noise (f = 40 MHz)   | 12 $\text{e}^-$ rms  |
| Dark Current<br>Photodiode / VCCD                                     | 7 / 100 $\text{e}^-/\text{s}$                                      |
| Dark Current Doubling Temp<br>Photodiode / VCCD                       | 7°C / 9°C  |
| Dynamic Range   | 64 dB  |
| Charge Transfer Efficiency  | 0.999999   |
| Blooming Suppression  | > 300 X  |
| Smear   | -100 dB  |
| Image Lag   | < 10 electrons   |
| Maximum Pixel Clock Speed   | 40 MHz   |
| Maximum Frame Rates<br>Quad / Dual / Single Output                    | 68 / 34 / 18 fps   |
| Package   | 68 Pin PGA<br>64 Pin CLCC  |
| Cover Glass   | AR Coated, 2-Sides or Clear Glass                                  |

NOTE: All Parameters are specified at T = 40°C unless otherwise noted.



ON Semiconductor®

[www.onsemi.com](http://www.onsemi.com)

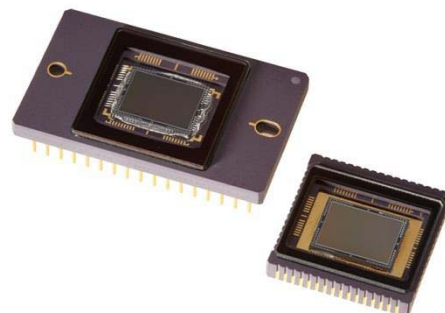


Figure 1. KAI-02050 Interline CCD Image Sensor

### Features

- Color or Monochrome Configurations
- Progressive Scan Readout
- Flexible Readout Architecture
- High Frame Rate
- High Sensitivity
- Low Noise Architecture
- Excellent Smear Performance
- Package Pin Reserved for Device Identification

### Applications

- Industrial Imaging
- Medical Imaging
- Security

### ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

# KAI-02050

## ORDERING INFORMATION

### Standard Devices

See full datasheet for ordering information associated with devices no longer recommended for new designs.

**Table 2. ORDERING INFORMATION – STANDARD DEVICES**

| Part Number           | Description  | Marking Code   |
|-----------------------|--|--|
| KAI-02050-AAA-JP-BA   | Monochrome, No Microlens, PGA Package, Taped Clear Cover Glass, No Coatings, Standard Grade.   | KAI-02050-AAA<br>Serial Number                           |
| KAI-02050-AAA-JP-AE   | Monochrome, No Microlens, PGA Package, Taped Clear Cover Glass, No Coatings, Engineering Grade.  |  |
| KAI-02050-ABA-JD-BA   | Monochrome, Telecentric Microlens, PGA Package, Sealed Clear Cover Glass with AR Coating (Both Sides), Standard Grade.                 | KAI-02050-ABA<br>Serial Number                           |
| KAI-02050-ABA-JD-AE   | Monochrome, Telecentric Microlens, PGA Package, Sealed Clear Cover Glass with AR Coating (Both Sides), Engineering Grade.              |  |
| KAI-02050-ABA-JP-BA   | Monochrome, Telecentric Microlens, PGA Package, Taped Clear Cover Glass, No Coatings, Standard Grade.                                  |  |
| KAI-02050-ABA-JP-AE   | Monochrome, Telecentric Microlens, PGA Package, Taped Clear Cover Glass, No Coatings, Engineering Grade.                               |  |
| KAI-02050-ABA-FD-BA   | Monochrome, Telecentric Microlens, CLCC Package, Sealed Clear Cover Glass with AR Coating (Both Sides), Standard Grade.                |  |
| KAI-02050-ABA-FD-AE   | Monochrome, Telecentric Microlens, CLCC Package, Sealed Clear Cover Glass with AR Coating (Both Sides), Engineering Grade.             |  |
| KAI-02050-FBA-JD-BA   | Gen2 Color (Bayer RGB), Telecentric Microlens, PGA Package, Sealed Clear Cover Glass with AR Coating (Both Sides), Standard Grade.     | KAI-02050-FBA<br>Serial Number                           |
| KAI-02050-FBA-JD-AE   | Gen2 Color (Bayer RGB), Telecentric Microlens, PGA Package, Sealed Clear Cover Glass with AR Coating (Both Sides), Engineering Grade.  |  |
| KAI-02050-FBA-FD-BA   | Gen2 Color (Bayer RGB), Telecentric Microlens, CLCC Package, Sealed Clear Cover Glass with AR Coating (Both Sides), Standard Grade.    |  |
| KAI-02050-FBA-FD-AE   | Gen2 Color (Bayer RGB), Telecentric Microlens, CLCC Package, Sealed Clear Cover Glass with AR Coating (Both Sides), Engineering Grade. |  |
| KAI-02050-FBA-JB-B2   | Gen2 Color (Bayer RGB), Telecentric Microlens, PGA Package, Sealed Clear Cover Glass (No Coatings), Grade 2.                           | KAI-02050-FBA<br>Serial Number<br>V <sub>AB</sub> = xx.x |
| KAI-02050-FBA-JB-AE   | Gen2 Color (Bayer RGB), Telecentric Microlens, PGA Package, Sealed Clear Cover Glass (No Coatings), Engineering Grade.                 |  |
| KAI-02050-FBA-JB-B2-T | Gen2 Color (Bayer RGB), Telecentric Microlens, PGA Package, Sealed Clear Cover Glass (No Coatings), Grade 2, Packed in Trays.          |  |

See the ON Semiconductor *Device Nomenclature* document (TND310/D) for a full description of the naming convention used for image sensors. For reference documentation, including information on evaluation kits, please visit our web site at [www.onsemi.com](http://www.onsemi.com).

# KAI-02050

## Not Recommended for New Designs

**Table 3. ORDERING INFORMATION – NOT RECOMMENDED FOR NEW DESIGNS**

| Part Number           | Description  | Marking Code   |
|-----------------------|--|--|
| KAI-02050-CBA-JD-BA   | Gen1 Color (Bayer RGB), Telecentric Microlens, PGA Package, Sealed Clear Cover Glass with AR Coating (Both Sides), Standard Grade.     | KAI-02050-CBA<br>Serial Number                           |
| KAI-02050-CBA-JD-AE   | Gen1 Color (Bayer RGB), Telecentric Microlens, PGA Package, Sealed Clear Cover Glass with AR Coating (Both Sides), Engineering Grade.  |  |
| KAI-02050-CBA-FD-BA   | Gen1 Color (Bayer RGB), Telecentric Microlens, CLCC Package, Sealed Clear Cover Glass with AR Coating (Both Sides), Standard Grade.    |  |
| KAI-02050-CBA-FD-AE   | Gen1 Color (Bayer RGB), Telecentric Microlens, CLCC Package, Sealed Clear Cover Glass with AR Coating (Both Sides), Engineering Grade. |  |
| KAI-02050-CBA-JB-B2   | Gen1 Color (Bayer RGB), Telecentric Microlens, PGA Package, Sealed Clear Cover Glass (No Coatings), Grade 2.                           | KAI-02050-CBA<br>Serial Number<br>V <sub>AB</sub> = xx.x |
| KAI-02050-CBA-JB-AE   | Gen1 Color (Bayer RGB), Telecentric Microlens, PGA Package, Sealed Clear Cover Glass (No Coatings), Engineering Grade.                 |  |
| KAI-02050-CBA-JB-B2-T | Gen1 Color (Bayer RGB), Telecentric Microlens, PGA Package, Sealed Clear Cover Glass (No Coatings), Grade 2, Packed in Trays.          |  |

DEVICE DESCRIPTION

Architecture

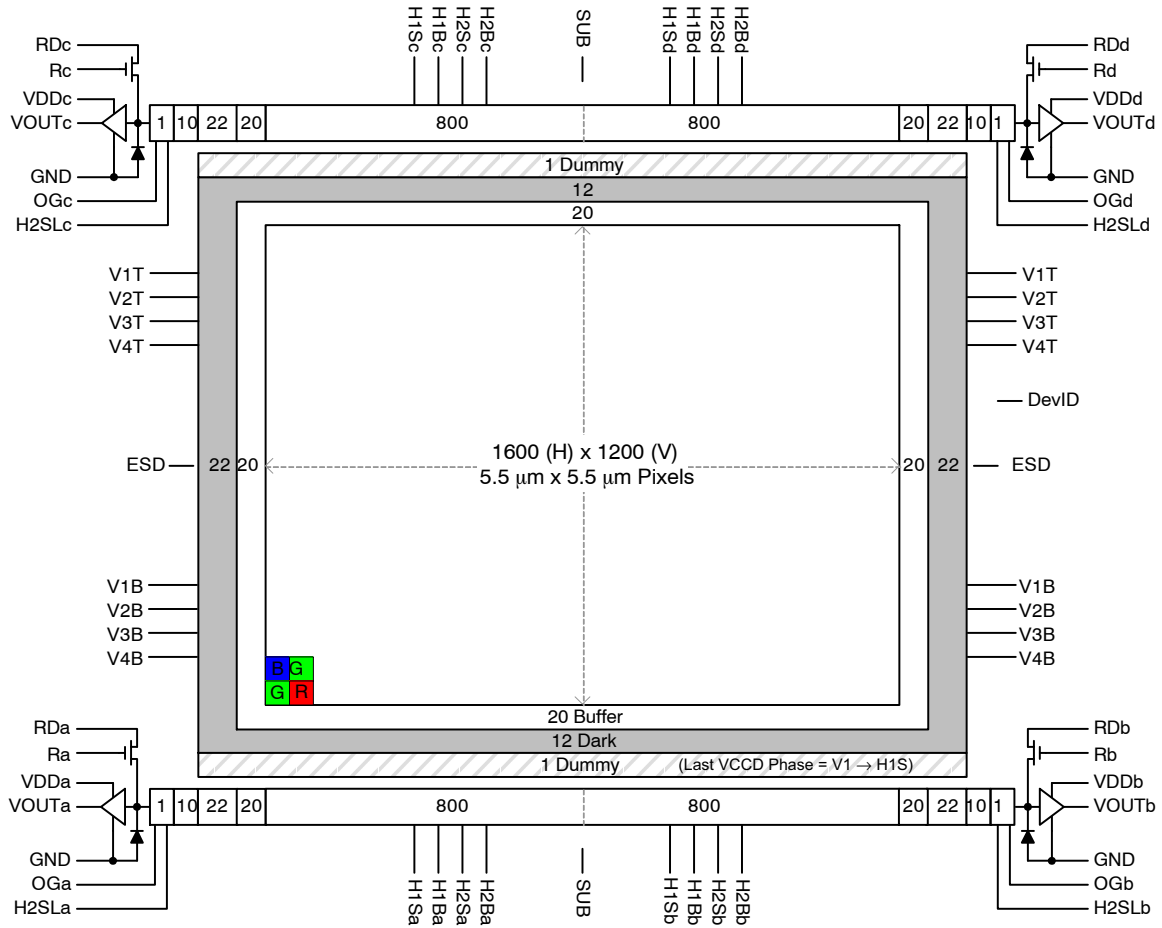


Figure 2. Block Diagram

**Dark Reference Pixels**

There are 12 dark reference rows at the top and 12 dark rows at the bottom of the image sensor. The dark rows are not entirely dark and so should not be used for a dark reference level. Use the 22 dark columns on the left or right side of the image sensor as a dark reference.

Under normal circumstances use only the center 20 columns of the 22 column dark reference due to potential light leakage.

**Dummy Pixels**

Within each horizontal shift register there are 11 leading additional shift phases. These pixels are designated as dummy pixels and should not be used to determine a dark reference level.

In addition, there is one dummy row of pixels at the top and bottom of the image.

**Active Buffer Pixels**

20 unshielded pixels adjacent to any leading or trailing dark reference regions are classified as active buffer pixels.

These pixels are light sensitive but are not tested for defects and non-uniformities.

**Image Acquisition**

An electronic representation of an image is formed when incident photons falling on the sensor plane create electron-hole pairs within the individual silicon photodiodes. These photoelectrons are collected locally by the formation of potential wells at each photosite. Below photodiode saturation, the number of photoelectrons collected at each pixel is linearly dependent upon light level and exposure time and non-linearly dependent on wavelength. When the photodiodes charge capacity is reached, excess electrons are discharged into the substrate to prevent blooming.

**ESD Protection**

Adherence to the power-up and power-down sequence is critical. Failure to follow the proper power-up and power-down sequences may cause damage to the sensor. See Power-Up and Power-Down Sequence section.

Physical Description

PGA Pin Description and Device Orientation

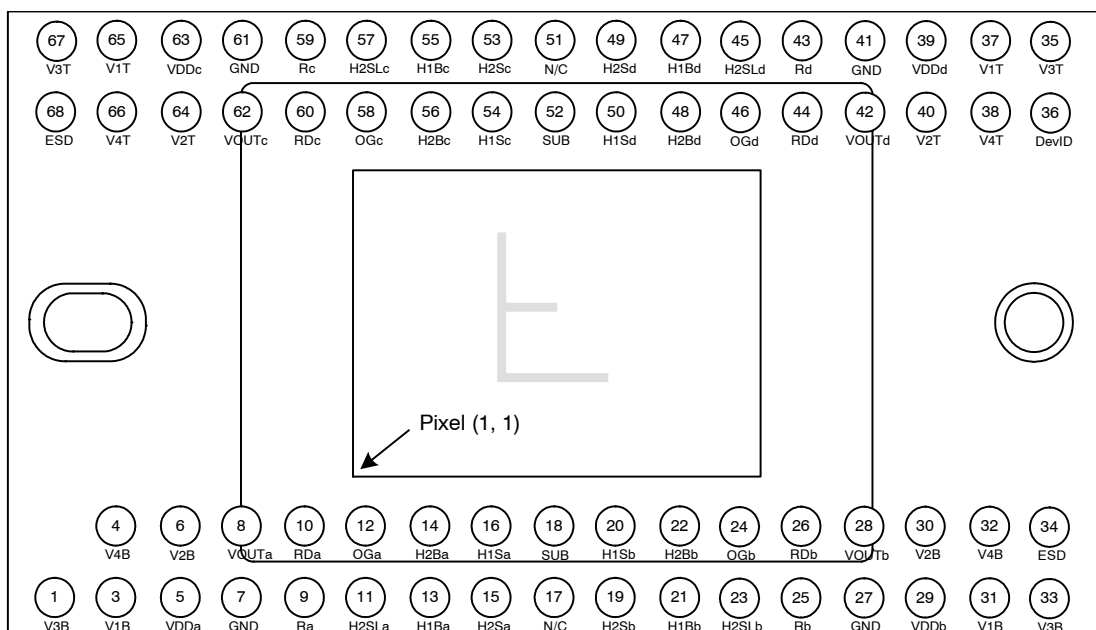


Figure 3. PGA Package Pin Designations – Top View

Table 4. PGA PACKAGE PIN DESCRIPTION

| Pin | Name  | Description  |
|-----|-------|--|
| 1   | V3B   | Vertical CCD Clock, Phase 3, Bottom                            |
| 3   | V1B   | Vertical CCD Clock, Phase 1, Bottom                            |
| 4   | V4B   | Vertical CCD Clock, Phase 4, Bottom                            |
| 5   | VDDa  | Output Amplifier Supply, Quadrant a                            |
| 6   | V2B   | Vertical CCD Clock, Phase 2, Bottom                            |
| 7   | GND   | Ground   |
| 8   | VOUTa | Video Output, Quadrant a                                       |
| 9   | Ra    | Reset Gate, Quadrant a   |
| 10  | RDa   | Reset Drain, Quadrant a  |
| 11  | H2SLa | Horizontal CCD Clock, Phase 2, Storage, Last Phase, Quadrant a |
| 12  | OGa   | Output Gate, Quadrant a  |
| 13  | H1Ba  | Horizontal CCD Clock, Phase 1, Barrier, Quadrant a             |
| 14  | H2Ba  | Horizontal CCD Clock, Phase 2, Barrier, Quadrant a             |
| 15  | H2Sa  | Horizontal CCD Clock, Phase 2, Storage, Quadrant a             |
| 16  | H1Sa  | Horizontal CCD Clock, Phase 1, Storage, Quadrant a             |
| 17  | N/C   | No Connect   |
| 18  | SUB   | Substrate  |
| 19  | H2Sb  | Horizontal CCD Clock, Phase 2, Storage, Quadrant b             |
| 20  | H1Sb  | Horizontal CCD Clock, Phase 1, Storage, Quadrant b             |
| 21  | H1Bb  | Horizontal CCD Clock, Phase 1, Barrier, Quadrant b             |
| 22  | H2Bb  | Horizontal CCD Clock, Phase 2, Barrier, Quadrant b             |
| 23  | H2SLb | Horizontal CCD Clock, Phase 1, Storage, Last Phase, Quadrant b |
| 24  | OGb   | Output Gate, Quadrant b  |

# KAI-02050

**Table 4. PGA PACKAGE PIN DESCRIPTION** (continued)

| Pin | Name  | Description  |
|-----|-------|--|
| 25  | Rb    | Reset Gate, Quadrant b   |
| 26  | RDb   | Reset Drain, Quadrant b  |
| 27  | GND   | Ground   |
| 28  | VOuTb | Video Output, Quadrant b                                       |
| 29  | VDDb  | Output Amplifier Supply, Quadrant b                            |
| 30  | V2B   | Vertical CCD Clock, Phase 2, Bottom                            |
| 31  | V1B   | Vertical CCD Clock, Phase 1, Bottom                            |
| 32  | V4B   | Vertical CCD Clock, Phase 4, Bottom                            |
| 33  | V3B   | Vertical CCD Clock, Phase 3, Bottom                            |
| 34  | ESD   | ESD Protection Disable   |
| 35  | V3T   | Vertical CCD Clock, Phase 3, Top                               |
| 36  | DevID | Device Identification  |
| 37  | V1T   | Vertical CCD Clock, Phase 1, Top                               |
| 38  | V4T   | Vertical CCD Clock, Phase 4, Top                               |
| 39  | VDDd  | Output Amplifier Supply, Quadrant d                            |
| 40  | V2T   | Vertical CCD Clock, Phase 2, Top                               |
| 41  | GND   | Ground   |
| 42  | VOuTd | Video Output, Quadrant d                                       |
| 43  | Rd    | Reset Gate, Quadrant d   |
| 44  | RdD   | Reset Drain, Quadrant d  |
| 45  | H2SLd | Horizontal CCD Clock, Phase 2, Storage, Last Phase, Quadrant d |
| 46  | OGd   | Output Gate, Quadrant d  |
| 47  | H1Bd  | Horizontal CCD Clock, Phase 1, Barrier, Quadrant d             |
| 48  | H2Bd  | Horizontal CCD Clock, Phase 2, Barrier, Quadrant d             |
| 49  | H2Sd  | Horizontal CCD Clock, Phase 2, Storage, Quadrant d             |
| 50  | H1Sd  | Horizontal CCD Clock, Phase 1, Storage, Quadrant d             |
| 51  | N/C   | No Connect   |
| 52  | SUB   | Substrate  |
| 53  | H2Sc  | Horizontal CCD Clock, Phase 2, Storage, Quadrant c             |
| 54  | H1Sc  | Horizontal CCD Clock, Phase 1, Storage, Quadrant c             |
| 55  | H1Bc  | Horizontal CCD Clock, Phase 1, Barrier, Quadrant c             |
| 56  | H2Bc  | Horizontal CCD Clock, Phase 2, Barrier, Quadrant c             |
| 57  | H2SLc | Horizontal CCD Clock, Phase 2, Storage, Last Phase, Quadrant c |
| 58  | OGc   | Output Gate, Quadrant c  |
| 59  | Rc    | Reset Gate, Quadrant c   |
| 60  | RdC   | Reset Drain, Quadrant c  |
| 61  | GND   | Ground   |
| 62  | VOuTc | Video Output, Quadrant c                                       |
| 63  | VDDc  | Output Amplifier Supply, Quadrant c                            |
| 64  | V2T   | Vertical CCD Clock, Phase 2, Top                               |
| 65  | V1T   | Vertical CCD Clock, Phase 1, Top                               |
| 66  | V4T   | Vertical CCD Clock, Phase 4, Top                               |
| 67  | V3T   | Vertical CCD Clock, Phase 3, Top                               |
| 68  | ESD   | EDS Protection Disable   |

1. Liked named pins are internally connected and should have a common drive signal.
2. N/C pins (17, 51) should be left floating.

Ceramic Leadless Chip Carrier Pin Description

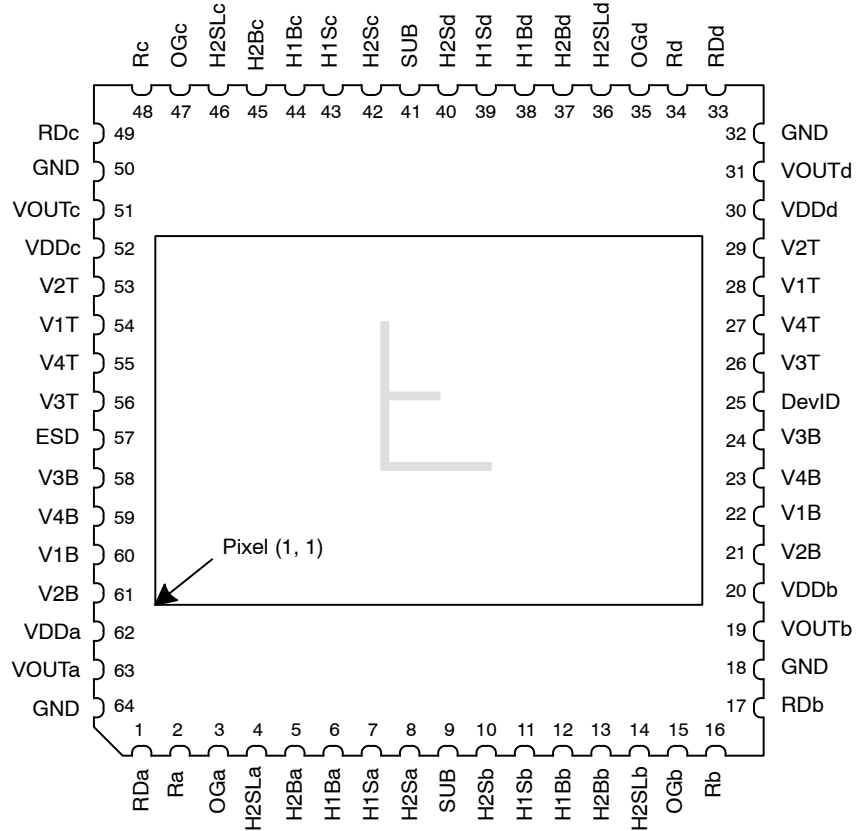


Figure 4. CLCC Package Pin Designations – Top View

Table 5. CLCC PACKAGE PIN DESCRIPTION

| Pin | Name  | Description  |
|-----|-------|--|
| 1   | RDa   | Reset Drain, Quadrant a  |
| 2   | Ra    | Reset Gate, Quadrant a   |
| 3   | OGa   | Output Gate, Quadrant a  |
| 4   | H2SLa | Horizontal CCD Clock, Phase 2, Storage, Last Phase, Quadrant a |
| 5   | H2Ba  | Horizontal CCD Clock, Phase 2, Barrier, Quadrant a             |
| 6   | H1Ba  | Horizontal CCD Clock, Phase 1, Barrier, Quadrant a             |
| 7   | H1Sa  | Horizontal CCD Clock, Phase 1, Storage, Quadrant a             |
| 8   | H2Sa  | Horizontal CCD Clock, Phase 2, Storage, Quadrant a             |
| 9   | SUB   | Substrate  |
| 10  | H2Sb  | Horizontal CCD Clock, Phase 2, Storage, Quadrant b             |
| 11  | H1Sb  | Horizontal CCD Clock, Phase 1, Storage, Quadrant b             |
| 12  | H1Bb  | Horizontal CCD Clock, Phase 1, Barrier, Quadrant b             |
| 13  | H2Bb  | Horizontal CCD Clock, Phase 2, Barrier, Quadrant b             |
| 14  | H2SLb | Horizontal CCD Clock, Phase 2, Storage, Last Phase, Quadrant b |
| 15  | OGb   | Output Gate, Quadrant b  |
| 16  | Rb    | Reset Gate, Quadrant b   |
| 17  | RDb   | Reset Drain, Quadrant b  |
| 18  | GND   | Ground   |
| 19  | VOUTb | Video Output, Quadrant b                                       |

**Table 5. CLCC PACKAGE PIN DESCRIPTION** (continued)

| Pin | Name  | Description  |
|-----|-------|--|
| 20  | VDDb  | Output Amplifier Supply, Quadrant b                            |
| 21  | V2B   | Vertical CCD Clock, Phase 2, Bottom                            |
| 22  | V1B   | Vertical CCD Clock, Phase 1, Bottom                            |
| 23  | V4B   | Vertical CCD Clock, Phase 4, Bottom                            |
| 24  | V3B   | Vertical CCD Clock, Phase 3, Bottom                            |
| 25  | DevID | Device Identification  |
| 26  | V3T   | Vertical CCD Clock, Phase 3, Top                               |
| 27  | V4T   | Vertical CCD Clock, Phase 4, Top                               |
| 28  | V1T   | Vertical CCD Clock, Phase 1, Top                               |
| 29  | V2T   | Vertical CCD Clock, Phase 2, Top                               |
| 30  | VDDd  | Output Amplifier Supply, Quadrant d                            |
| 31  | VOUtd | Video Output, Quadrant d                                       |
| 32  | GND   | Ground   |
| 33  | RDd   | Reset Drain, Quadrant d  |
| 34  | Rd    | Reset Gate, Quadrant d   |
| 35  | OGd   | Output Gate, Quadrant d  |
| 36  | H2SLd | Horizontal CCD Clock, Phase 2, Storage, Last Phase, Quadrant d |
| 37  | H2Bd  | Horizontal CCD Clock, Phase 2, Barrier, Quadrant d             |
| 38  | H1Bd  | Horizontal CCD Clock, Phase 1, Barrier, Quadrant d             |
| 39  | H1Sd  | Horizontal CCD Clock, Phase 1, Storage, Quadrant d             |
| 40  | H2Sd  | Horizontal CCD Clock, Phase 2, Storage, Quadrant d             |
| 41  | SUB   | Substrate  |
| 42  | H2Sc  | Horizontal CCD Clock, Phase 2, Storage, Quadrant c             |
| 43  | H1Sc  | Horizontal CCD Clock, Phase 1, Storage, Quadrant c             |
| 44  | H1Bc  | Horizontal CCD Clock, Phase 1, Barrier, Quadrant c             |
| 45  | H2Bc  | Horizontal CCD Clock, Phase 2, Barrier, Quadrant c             |
| 46  | H2SLc | Horizontal CCD Clock, Phase 2, Storage, Last Phase, Quadrant c |
| 47  | OGc   | Output Gate, Quadrant c  |
| 48  | Rc    | Reset Gate, Quadrant c   |
| 49  | RDc   | Reset Drain, Quadrant c  |
| 50  | GND   | Ground   |
| 51  | VOUtc | Video Output, Quadrant c                                       |
| 52  | VDDc  | Output Amplifier Supply, Quadrant c                            |
| 53  | V2T   | Vertical CCD Clock, Phase 2, Top                               |
| 54  | V1T   | Vertical CCD Clock, Phase 1, Top                               |
| 55  | V4T   | Vertical CCD Clock, Phase 4, Top                               |
| 56  | V3T   | Vertical CCD Clock, Phase 3, Top                               |
| 57  | ESD   | ESD Protection Disable   |
| 58  | V3B   | Vertical CCD Clock, Phase 3, Bottom                            |
| 59  | V4B   | Vertical CCD Clock, Phase 4, Bottom                            |
| 60  | V1B   | Vertical CCD Clock, Phase 1, Bottom                            |
| 61  | V2B   | Vertical CCD Clock, Phase 2, Bottom                            |
| 62  | VDDa  | Output Amplifier Supply, Quadrant a                            |
| 63  | VOUta | Video Output, Quadrant a                                       |
| 64  | GND   | Ground   |

1. Liked named pins are internally connected and should have a common drive signal.



**IMAGING PERFORMANCE**

**Typical Operational Conditions**

Unless otherwise noted, the Imaging Performance Specifications are measured using the following conditions.

**Table 6. TYPICAL OPERATIONAL CONDITIONS**

| Description  | Condition  | Notes                                       |
|--------------|--|---|
| Light Source | Continuous Red, Green and Blue LED Illumination. | For monochrome sensor, only green LED used. |
| Operation    | Nominal Operating Voltages and Timing.           |   |

**Specifications**

**Table 7. PERFORMANCE SPECIFICATIONS**

| Description  | Symbol              | Min.     | Nom.     | Max. | Unit        | Sampling Plan | Temperature Tested at (°C) |
|--|---------------------|----------|----------|------|-------------|---------------|----------------------------|
| <b>ALL CONFIGURATIONS</b>                                      |                     |          |          |      |             |               |                            |
| Dark Field Global Non-Uniformity                               | DSNU                | -        | -        | 2.0  | mVpp        | Die           | 27, 40                     |
| Bright Field Global Non-Uniformity (Note 1)                    |                     | -        | 2.0      | 5.0  | % rms       | Die           | 27, 40                     |
| Bright Field Global Peak to Peak Non-Uniformity (Note 1)       | PRNU                | -        | 5.0      | 15.0 | % pp        | Die           | 27, 40                     |
| Bright Field Center Non-Uniformity (Note 1)                    |                     | -        | 1.0      | 2.0  | % rms       | Die           | 27, 40                     |
| Maximum Photoresponse Non-Linearity (Note 2)                   | NL                  | -        | 2        | -    | %           | Design        |                            |
| Maximum Gain Difference between Outputs (Note 2)               | $\Delta G$          | -        | 10       | -    | %           | Design        |                            |
| Maximum Signal Error due to Non-Linearity Differences (Note 2) | $\Delta NL$         | -        | 1        | -    | %           | Design        |                            |
| Horizontal CCD Charge Capacity                                 | $H_{Ne}$            | -        | 55       | -    | $ke^-$      | Design        |                            |
| Vertical CCD Charge Capacity                                   | $V_{Ne}$            | -        | 45       | -    | $ke^-$      | Design        |                            |
| Photodiode Charge Capacity (Note 3)                            | $P_{Ne}$            | -        | 20       | -    | $ke^-$      | Die           | 27, 40                     |
| Horizontal CCD Charge Transfer Efficiency                      | HCTTE               | 0.999995 | 0.999999 | -    |             | Die           |                            |
| Vertical CCD Charge Transfer Efficiency                        | VCTE                | 0.999995 | 0.999999 | -    |             | Die           |                            |
| Photodiode Dark Current  | $I_{PD}$            | -        | 7        | 70   | e/p/s       | Die           | 40                         |
| Vertical CCD Dark Current                                      | $I_{VD}$            | -        | 100      | 300  | e/p/s       | Die           | 40                         |
| Image Lag  | Lag                 | -        | -        | 10   | $e^-$       | Design        |                            |
| Anti-Blooming Factor   | $X_{AB}$            | 300      | -        | -    |             | Design        |                            |
| Vertical Smear   | Smr                 | -        | -100     | -    | dB          | Design        |                            |
| Read Noise (Note 4)  | $n_{e-T}$           | -        | 12       | -    | $e^-$ rms   | Design        |                            |
| Dynamic Range (Notes 4, 5)                                     | DR                  | -        | 64       | -    | dB          | Design        |                            |
| Output Amplifier DC Offset                                     | $V_{ODC}$           | -        | 9.4      | -    | V           | Die           | 27, 40                     |
| Output Amplifier Bandwidth (Note 6)                            | $f_{-3db}$          | -        | 250      | -    | MHz         | Die           |                            |
| Output Amplifier Impedance                                     | $R_{OUT}$           | -        | 127      | -    | $\Omega$    | Die           | 27, 40                     |
| Output Amplifier Sensitivity                                   | $\Delta V/\Delta N$ | -        | 34       | -    | $\mu V/e^-$ | Design        |                            |

# KAI-02050

**Table 7. PERFORMANCE SPECIFICATIONS** (continued)

| Description | Symbol | Min. | Nom. | Max. | Unit | Sampling Plan | Temperature Tested at (°C) |
|-------------|--------|------|------|------|------|---------------|----------------------------|
|-------------|--------|------|------|------|------|---------------|----------------------------|

**KAI-02050-ABA CONFIGURATION**

|                                    |                   |   |     |   |    |        |  |
|------------------------------------|-------------------|---|-----|---|----|--------|--|
| Peak Quantum Efficiency            | QE <sub>MAX</sub> | - | 44  | - | %  | Design |  |
| Peak Quantum Efficiency Wavelength | λ <sub>QE</sub>   | - | 480 | - | nm | Design |  |

**KAI-02050-FBA GEN2 COLOR CONFIGURATION WITH MAR GLASS**

|  |                   |             |                   |             |    |        |  |
|--|-------------------|-------------|-------------------|-------------|----|--------|--|
| Peak Quantum Efficiency<br>Blue<br>Green<br>Red            | QE <sub>MAX</sub> | -<br>-<br>- | 38<br>37<br>31    | -<br>-<br>- | %  | Design |  |
| Peak Quantum Efficiency Wavelength<br>Blue<br>Green<br>Red | λ <sub>QE</sub>   | -<br>-<br>- | 460<br>530<br>605 | -<br>-<br>- | nm | Design |  |

**KAI-02050-CBA GEN1 COLOR CONFIGURATION WITH MAR GLASS** (Note 7)

|  |                   |             |                   |             |    |        |  |
|--|-------------------|-------------|-------------------|-------------|----|--------|--|
| Peak Quantum Efficiency<br>Blue<br>Green<br>Red            | QE <sub>MAX</sub> | -<br>-<br>- | 39<br>37<br>29    | -<br>-<br>- | %  | Design |  |
| Peak Quantum Efficiency Wavelength<br>Blue<br>Green<br>Red | λ <sub>QE</sub>   | -<br>-<br>- | 470<br>540<br>620 | -<br>-<br>- | nm | Design |  |

**KAI-02050-FBA GEN2 COLOR CONFIGURATION WITH CLEAR GLASS**

|  |                   |             |                   |             |    |        |  |
|--|-------------------|-------------|-------------------|-------------|----|--------|--|
| Peak Quantum Efficiency<br>Blue<br>Green<br>Red            | QE <sub>MAX</sub> | -<br>-<br>- | 35<br>34<br>29    | -<br>-<br>- | %  | Design |  |
| Peak Quantum Efficiency Wavelength<br>Blue<br>Green<br>Red | λ <sub>QE</sub>   | -<br>-<br>- | 460<br>530<br>605 | -<br>-<br>- | nm | Design |  |

**KAI-02050-CBA GEN1 COLOR CONFIGURATION WITH CLEAR GLASS** (Note 7)

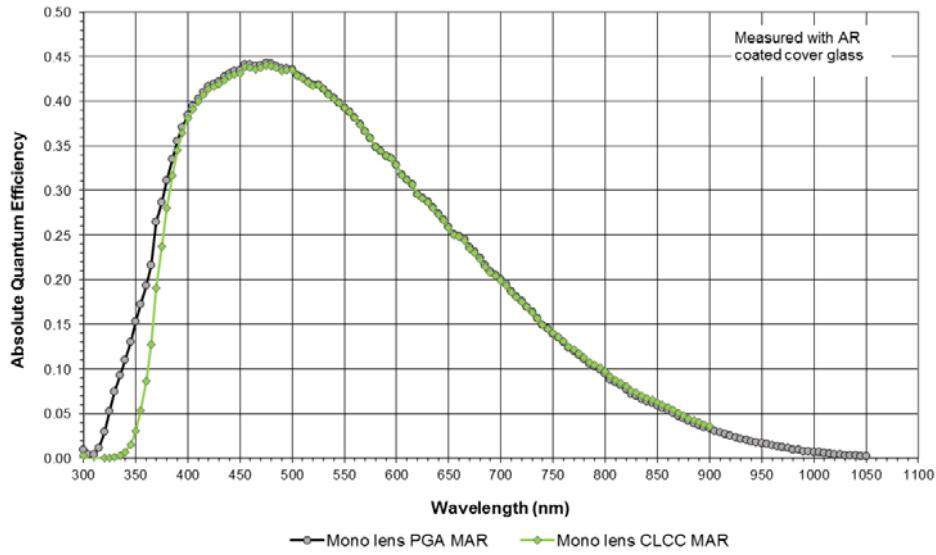
|  |                   |             |                   |             |    |        |  |
|--|-------------------|-------------|-------------------|-------------|----|--------|--|
| Peak Quantum Efficiency<br>Blue<br>Green<br>Red            | QE <sub>MAX</sub> | -<br>-<br>- | 36<br>34<br>27    | -<br>-<br>- | %  | Design |  |
| Peak Quantum Efficiency Wavelength<br>Blue<br>Green<br>Red | λ <sub>QE</sub>   | -<br>-<br>- | 470<br>540<br>620 | -<br>-<br>- | nm | Design |  |

1. Per color.
2. Value is over the range of 10% to 90% of photodiode saturation.
3. The operating value of the substrate voltage, V<sub>AB</sub>, will be marked on the shipping container for each device. The value of V<sub>AB</sub> is set such that the photodiode charge capacity is 680 mV.
4. At 40 MHz.
5. Uses 20LOG (P<sub>Ne</sub> / n<sub>e-T</sub>).
6. Assumes 5 pF load.
7. This color filter set configuration (Gen1) is not recommended for new designs.

TYPICAL PERFORMANCE CURVES

Quantum Efficiency

*Monochrome with Microlens*



NOTE: The PGA and CLCC versions have different quantum efficiencies due to differences in the cover glass transmission. See Figure 32: Cover Glass Transmission for more details.

Figure 5. Monochrome with Microlens Quantum Efficiency

*Monochrome without Microlens*

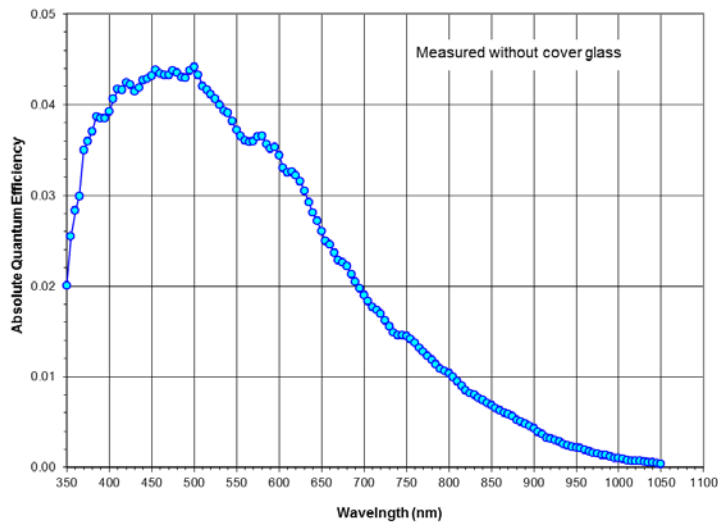


Figure 6. Monochrome without Microlens Quantum Efficiency

Color (Bayer RGB) with Microlens and MAR Cover Glass (Gen2 and Gen1 CFA)

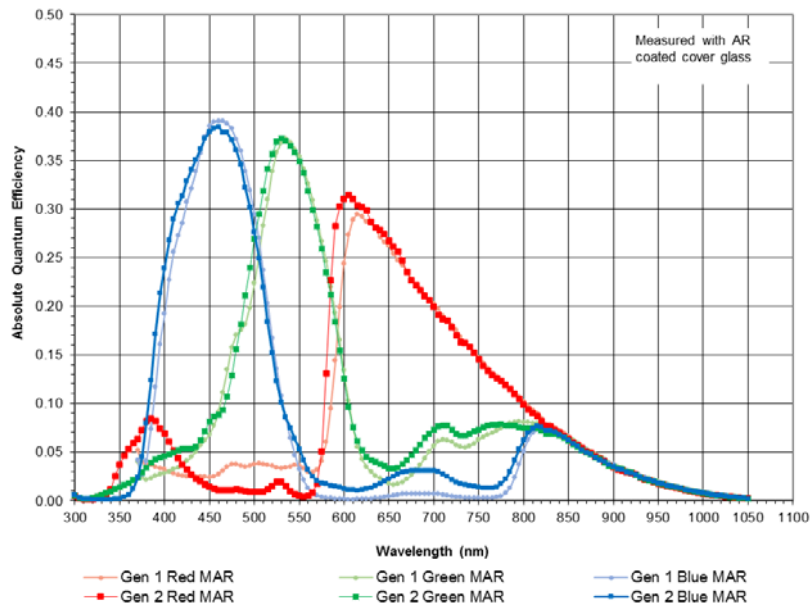


Figure 7. MAR Glass Color (Bayer) with Microlens Quantum Efficiency

Color (Bayer RGB) with Microlens and Clear Cover Glass (Gen2 and Gen1 CFA)

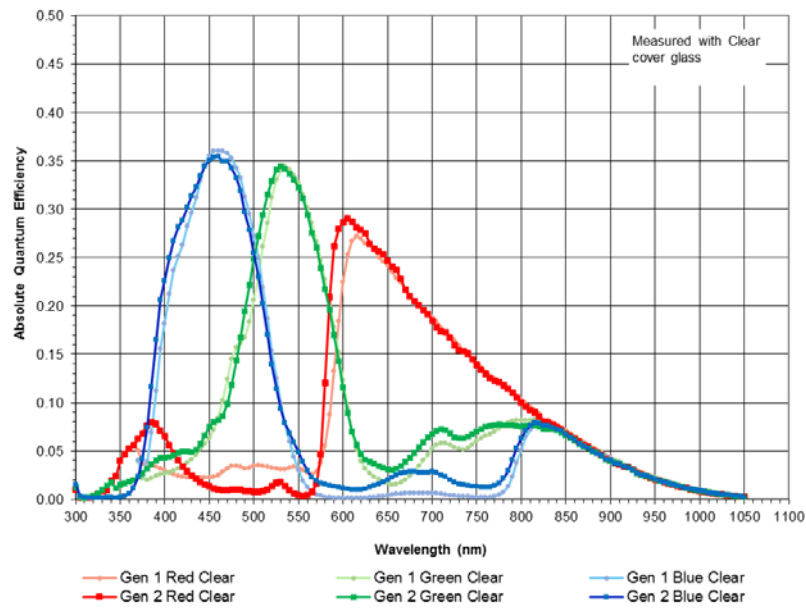
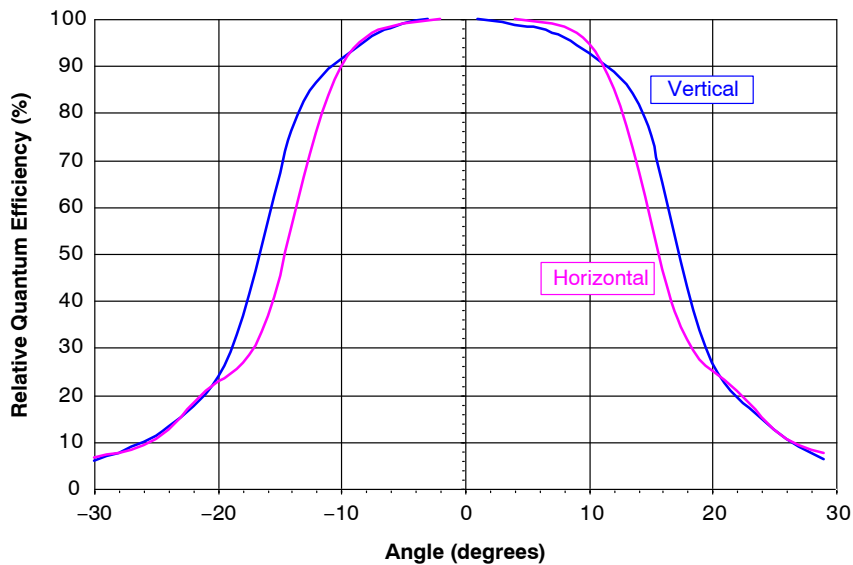


Figure 8. Clear Glass Color (Bayer) with Microlens Quantum Efficiency

**Angular Quantum Efficiency**

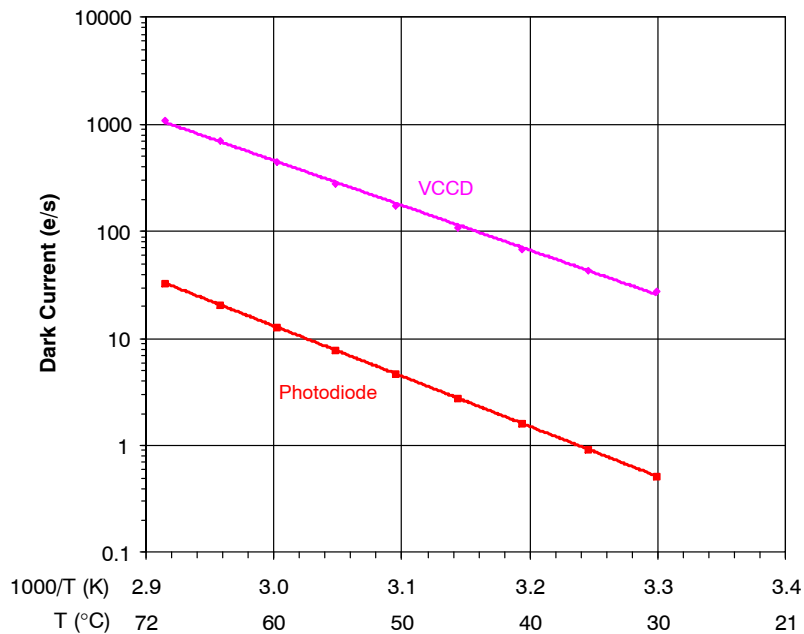
For the curves marked “Horizontal”, the incident light angle is varied in a plane parallel to the HCCD.  
 For the curves marked “Vertical”, the incident light angle is varied in a plane parallel to the VCCD.

*Monochrome with Microlens*



**Figure 9. Monochrome with Microlens Angular Quantum Efficiency**

**Dark Current vs. Temperature**



**Figure 10. Dark Current vs. Temperature**

Power-Estimated

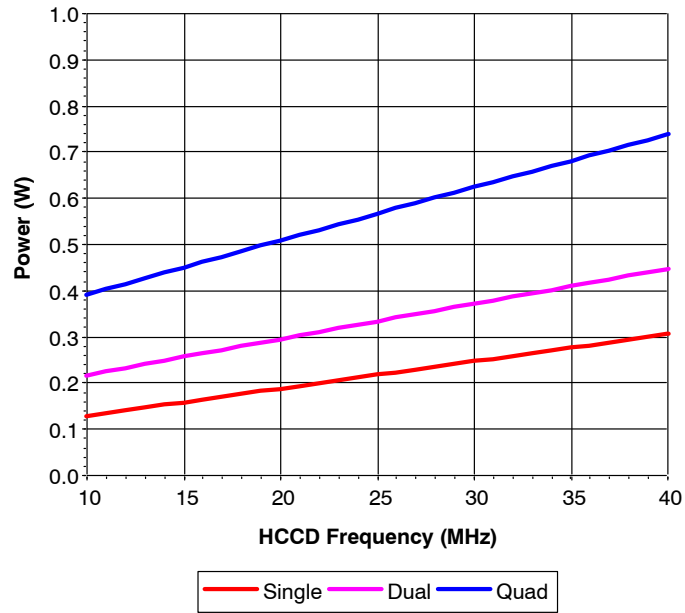


Figure 11. Power

Frame Rates

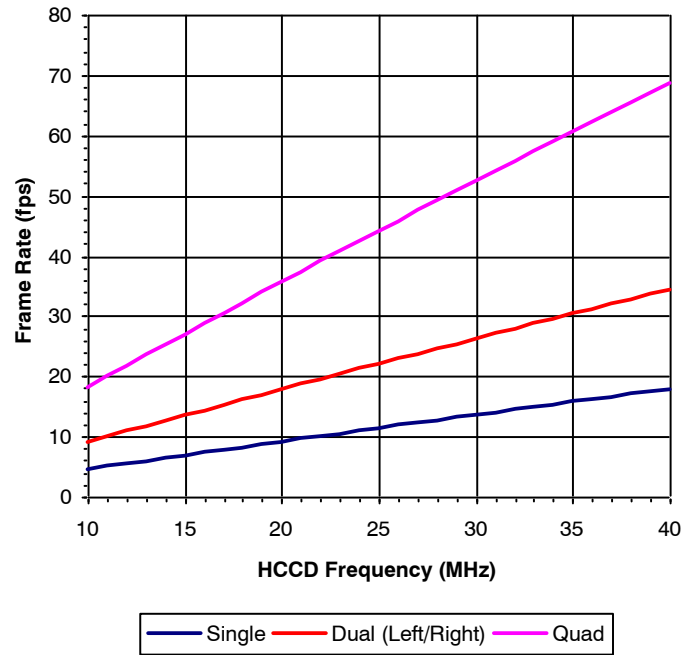


Figure 12. Frame Rates

**DEFECT DEFINITIONS**

**Table 8. OPERATION CONDITIONS FOR DEFECT TESTING AT 40°C**

| Description                 | Condition   | Notes |
|-----------------------------|---|-------|
| Operational Mode            | Two Outputs, Using VOUTa and VOUTc, Continuous Readout  |       |
| HCCD Clock Frequency        | 10 MHz  |       |
| Pixels per Line             | 1840  | 1     |
| Lines per Frame             | 720   | 2     |
| Line Time                   | 186.9 μs  |       |
| Frame Time                  | 134.6 ms  |       |
| Photodiode Integration Time | Mode A: PD_Tint = Frame Time = 134.6 ms, No Electronic Shutter Used<br>Mode B: PD_Tint = 33 ms, Electronic Shutter Used |       |
| VCCD Integration Time       | 118.1 ms  | 3     |
| Temperature                 | 40°C  |       |
| Light Source                | Continuous Red, Green and Blue LED Illumination   | 4     |
| Operation                   | Nominal Operating Voltages and Timing   |       |

1. Horizontal overclocking used.
2. Vertical overclocking used.
3. VCCD Integration Time = 632 lines × Line Time, which is the total time a pixel will spend in the VCCD registers.
4. For monochrome sensor, only the green LED is used.

**Table 9. DEFECT DEFINITIONS FOR TESTING AT 40°C**

| Description                             | Definition  | Standard Grade | Grade 2 | Notes |
|---|---|----------------|---------|-------|
| Major Dark Field Defective Bright Pixel | PD_Tint = Mode A → Defect ≥ 47 mV<br>or<br>PD_Tint = Mode B → Defect ≥ 12 mV                            | 20             | 20      | 1     |
| Major Bright Field Defective Dark Pixel | Defect ≥ 12%  | 20             | 20      | 1     |
| Minor Dark Field Defective Bright Pixel | PD_Tint = Mode A → Defect ≥ 24 mV<br>or<br>PD_Tint = Mode B → Defect ≥ 6 mV                             | 200            | 200     |       |
| Cluster Defect (Standard Grade)         | A group of 2 to 10 contiguous major defective pixels, but no more than 2 adjacent defects horizontally. | 8              | N/A     | 2     |
| Cluster Defect (Grade 2)                | A group of 2 to 10 contiguous major defective pixels.   | N/A            | 8       | 2     |
| Column Defect                           | A group of more than 10 contiguous major defective pixels along a single column.                        | 0              | 0       | 2     |

1. For the color device (KAI-02050-FBA or KAI-02050-CBA), a bright field defective pixel deviates by 12% with respect to pixels of the same color.
2. Column and cluster defects are separated by no less than two (2) good pixels in any direction (excluding single pixel defects).

**Table 10. OPERATION CONDITIONS FOR DEFECT TESTING AT 27°C**

| Description                           | Condition  | Notes |
|---------------------------------------|--|-------|
| Operational Mode                      | Two Outputs, Using VOUTa and VOUTc, Continuous Readout   |       |
| HCCD Clock Frequency                  | 20 MHz   |       |
| Pixels per Line                       | 1840   | 1     |
| Lines per Frame                       | 720  | 2     |
| Line Time                             | 93.8 $\mu$ s   |       |
| Frame Time                            | 67.5 ms  |       |
| Photodiode Integration Time (PD_Tint) | Mode A: PD_Tint = Frame Time = 67.5 ms, No Electronic Shutter Used<br>Mode B: PD_Tint = 33 ms, Electronic Shutter Used |       |
| VCCD Integration Time                 | 59.3 ms  | 3     |
| Temperature                           | 27°C   |       |
| Light Source                          | Continuous Red, Green and Blue LED Illumination  | 4     |
| Operation                             | Nominal Operating Voltages and Timing  |       |

1. Horizontal overclocking used.
2. Vertical overclocking used.
3. VCCD Integration Time = 632 lines  $\times$  Line Time, which is the total time a pixel will spend in the VCCD registers.
4. For monochrome sensor, only the green LED is used.

**Table 11. DEFECT DEFINITIONS FOR TESTING AT 40°C**

| Description                             | Definition   | Standard Grade | Grade 2 | Notes |
|---|--|----------------|---------|-------|
| Major Dark Field Defective Bright Pixel | PD_Tint = Mode A $\rightarrow$ Defect $\geq$ 8 mV<br>or<br>PD_Tint = Mode B $\rightarrow$ Defect $\geq$ 4 mV | 20             | 20      | 1     |
| Major Bright Field Defective Dark Pixel | Defect $\geq$ 12%  | 20             | 20      | 1     |
| Cluster Defect (Standard Grade)         | A group of 2 to 10 contiguous major defective pixels, but no more than 2 adjacent defects horizontally.      | 8              | N/A     | 2     |
| Cluster Defect (Grade 2)                | A group of 2 to 10 contiguous major defective pixels.  | N/A            | 8       | 2     |
| Column Defect                           | A group of more than 10 contiguous major defective pixels along a single column.                             | 0              | 0       | 2     |

1. For the color device (KAI-02050-FBA or KAI-02050-CBA), a bright field defective pixel deviates by 12% with respect to pixels of the same color.
2. Column and cluster defects are separated by no less than two (2) good pixels in any direction (excluding single pixel defects).

### Defect Map

The defect map supplied with each sensor is based upon testing at an ambient (27°C) temperature. Minor point defects are not included in the defect map. All defective

pixels are reference to pixel 1, 1 in the defect maps. See Figure 13: Regions of Interest for the location of pixel 1, 1.



**TEST DEFINITIONS**

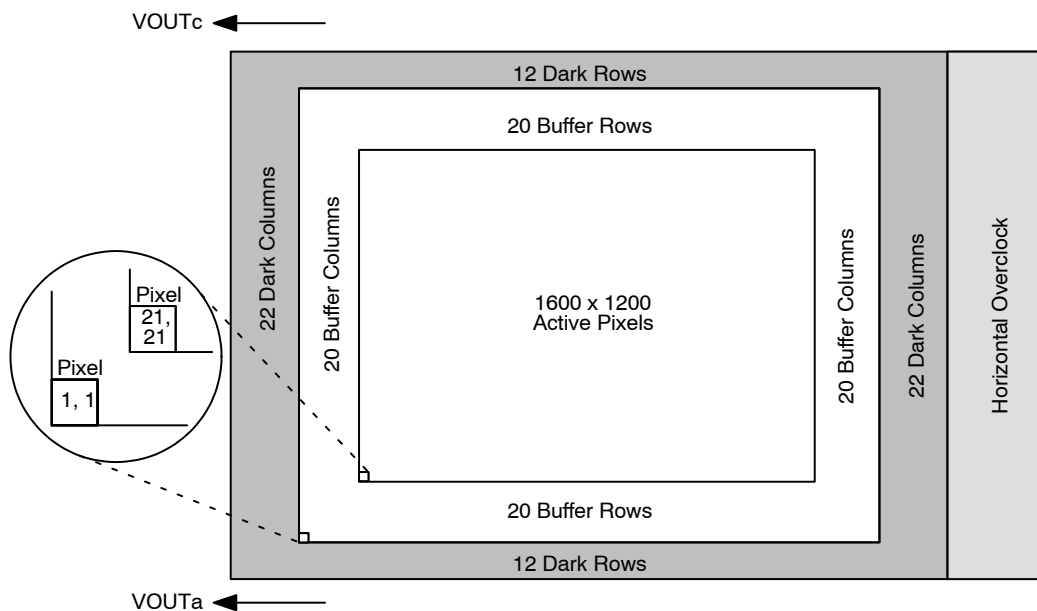
**Test Regions of Interest**

Image Area ROI: Pixel (1, 1) to Pixel (1640, 1240)  
 Active Area ROI: Pixel (21, 21) to Pixel (1620, 1220)  
 Center ROI: Pixel (771, 571) to Pixel (870, 670)

Only the Active Area ROI pixels are used for performance and defect tests.

**Overclocking**

The test system timing is configured such that the sensor is overclocked in both the vertical and horizontal directions. See Figure 13 for a pictorial representation of the regions of interest.



**Figure 13. Regions of Interest**

**Tests**

*Dark Field Global Non-Uniformity*

This test is performed under dark field conditions. The sensor is partitioned into 192 sub regions of interest, each of which is 100 by 100 pixels in size. See Figure 14: Test Sub Regions of Interest. The average signal level of each of the 192 sub regions of interest is calculated. The signal level of each of the sub regions of interest is calculated using the following formula:

$$\text{Signal of ROI}[i] = (\text{ROI Average in Counts} - \text{Horizontal Overclock Average in Counts}) \cdot \text{mV per Count}$$

Units : mVpp (millivolts Peak to Peak)

Where i = 1 to 192. During this calculation on the 192 sub regions of interest, the maximum and minimum signal levels are found. The dark field global uniformity is then calculated as the maximum signal found minus the minimum signal level found.

*Global Non-Uniformity*

This test is performed with the imager illuminated to a level such that the output is at 70% of saturation (approximately 476 mV). Prior to this test being performed the substrate

voltage has been set such that the charge capacity of the sensor is 680 mV. Global non-uniformity is defined as

$$\text{Global Non-Uniformity} = 100 \cdot \left( \frac{\text{Active Area Standard Deviation}}{\text{Active Area Signal}} \right)$$

Units : % rms

Active Area Signal = Active Area Average – Dark Column Average

*Global Peak to Peak Non-Uniformity*

This test is performed with the imager illuminated to a level such that the output is at 70% of saturation (approximately 476 mV). Prior to this test being performed the substrate voltage has been set such that the charge capacity of the sensor is 680 mV. The sensor is partitioned into 192 sub regions of interest, each of which is 100 by 100 pixels in size. See Figure 14: Test Sub Regions of Interest. The average signal level of each of the 192 sub regions of interest (ROI) is calculated. The signal level of each of the sub regions of interest is calculated using the following formula:

$$\text{Signal of ROI}[i] = (\text{ROI Average in Counts} - \text{Horizontal Overclock Average in Counts}) \cdot \text{mV per Count}$$

Where  $i = 1$  to 192. During this calculation on the 192 sub regions of interest, the maximum and minimum signal levels are found. The global peak to peak uniformity is then calculated as:

$$\text{Global Uniformity} = 100 \cdot \left( \frac{\text{Max. Signal} - \text{Min. Signal}}{\text{Active Area Signal}} \right)$$

Units : % pp

#### *Center Non-Uniformity*

This test is performed with the imager illuminated to a level such that the output is at 70% of saturation (approximately 476 mV). Prior to this test being performed the substrate voltage has been set such that the charge capacity of the sensor is 680 mV. Defects are excluded for the calculation of this test. This test is performed on the center 100 by 100 pixels of the sensor. Center uniformity is defined as:

$$\text{Center ROI Uniformity} = 100 \cdot \left( \frac{\text{Center ROI Standard Deviation}}{\text{Center ROI Signal}} \right)$$

Units : % rms

Center ROI Signal = Center ROI Average - Dark Column Average

#### *Dark Field Defect Test*

This test is performed under dark field conditions. The sensor is partitioned into 192 sub regions of interest, each of which is 100 by 100 pixels in size. In each region of interest, the median value of all pixels is found. For each region of interest, a pixel is marked defective if it is greater than or equal to the median value of that region of interest plus the defect threshold specified in the “Defect Definitions” section.

#### *Bright Field Defect Test*

This test is performed with the imager illuminated to a level such that the output is at approximately 476 mV. Prior to this test being performed the substrate voltage has been set such that the charge capacity of the sensor is 680 mV. The average signal level of all active pixels is found. The bright and dark thresholds are set as:

Dark Defect Threshold = Active Area Signal · Threshold

Bright Defect Threshold = Active Area Signal · Threshold

The sensor is then partitioned into 192 sub regions of interest, each of which is 100 by 100 pixels in size. In each region of interest, the average value of all pixels is found. For each region of interest, a pixel is marked defective if it is greater than or equal to the median value of that region of interest plus the bright threshold specified or if it is less than or equal to the median value of that region of interest minus the dark threshold specified.

Example for major bright field defective pixels:

- Average value of all active pixels is found to be 476 mV.
- Dark defect threshold:  $476 \text{ mV} \cdot 12 \% = 57 \text{ mV}$ .
- Bright defect threshold:  $476 \text{ mV} \cdot 12 \% = 57 \text{ mV}$ .
- Region of interest #1 selected. This region of interest is pixels 21, 21 to pixels 120, 120.
  - ♦ Median of this region of interest is found to be 470 mV.
  - ♦ Any pixel in this region of interest that is  $\geq (470 + 57 \text{ mV})$  527 mV in intensity will be marked defective.
  - ♦ Any pixel in this region of interest that is  $\leq (470 - 57 \text{ mV})$  413 mV in intensity will be marked defective.
- All remaining 192 sub regions of interest are analyzed for defective pixels in the same manner.

Test Sub Regions of Interest

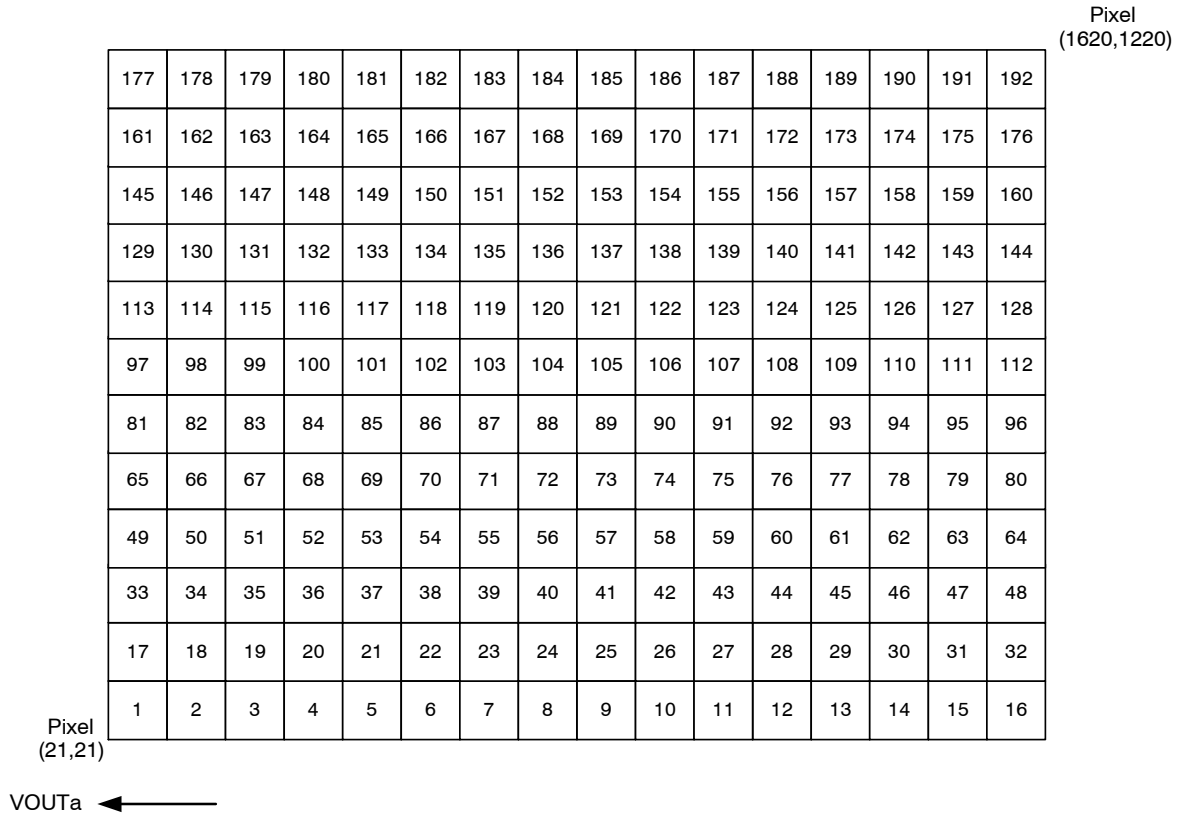


Figure 14. Test Sub Regions of Interest

## OPERATION

**Absolute Maximum Ratings**

Absolute maximum rating is defined as a level or condition that should not be exceeded at any time per the

description. If the level or the condition is exceeded, the device will be degraded and may be damaged. Operation at these values will reduce MTTF.

**Table 12. ABSOLUTE MAXIMUM RATINGS**

| Description           | Symbol           | Minimum | Maximum | Unit | Notes |
|-----------------------|------------------|---------|---------|------|-------|
| Operating Temperature | T <sub>OP</sub>  | -50     | 70      | °C   | 1     |
| Humidity              | RH               | 5       | 90      | %    | 2     |
| Output Bias Current   | I <sub>OUT</sub> | -       | 60      | mA   | 3     |
| Off-Chip Load         | C <sub>L</sub>   | -       | 10      | pF   |       |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

- Noise performance will degrade at higher temperatures.
- T = 25°C. Excessive humidity will degrade MTTF.
- Total for all outputs. Maximum current is -15 mA for each output. Avoid shorting output pins to ground or any low impedance source during operation. Amplifier bandwidth increases at higher current and lower load capacitance at the expense of reduced gain (sensitivity).

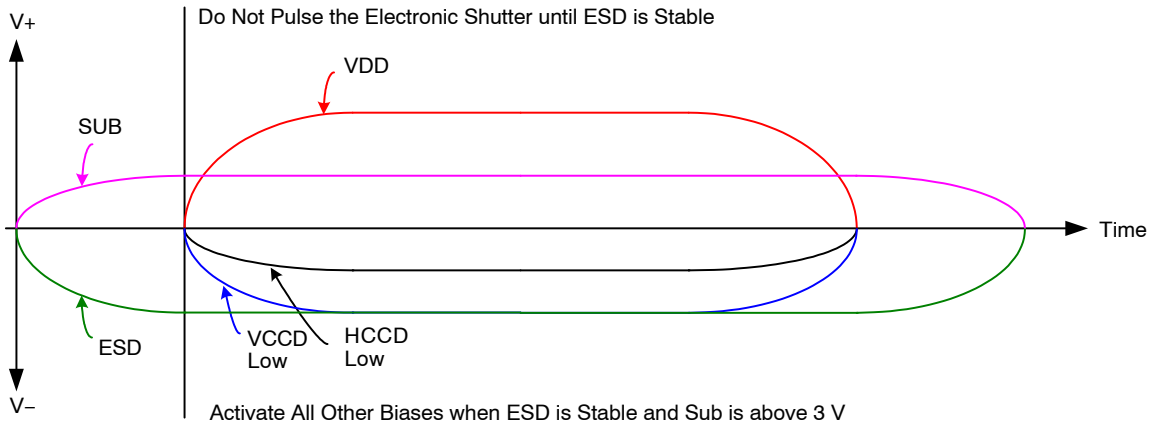
**Table 13. ABSOLUTE MAXIMUM VOLTAGE RATINGS BETWEEN PINS AND GROUND**

| Description  | Minimum   | Maximum    | Unit | Notes |
|--|-----------|------------|------|-------|
| VDD <sub>α</sub> , VOUT <sub>α</sub>   | -0.4      | 17.5       | V    | 1     |
| RD <sub>α</sub>  | -0.4      | 15.5       | V    | 1     |
| V1B, V1T   | ESD - 0.4 | ESD + 24.0 | V    |       |
| V2B, V2T, V3B, V3T, V4B, V4T   | ESD - 0.4 | ESD + 14.0 | V    |       |
| H1S <sub>α</sub> , H1B <sub>α</sub> , H2S <sub>α</sub> , H2B <sub>α</sub> , H2SL <sub>α</sub> , R <sub>α</sub> , OG <sub>α</sub> | ESD - 0.4 | ESD + 14.0 | V    | 1     |
| ESD  | -10.0     | 0.0        | V    |       |
| SUB  | -0.4      | 40.0       | V    | 2     |

- α denotes a, b, c or d.
- Refer to Application Note *Using Interline CCD Image Sensors in High Intensity Visible Lighting Conditions*

**Power-Up and Power-Down Sequence**

Adherence to the power-up and power-down sequence is critical. Failure to follow the proper power-up and power-down sequences may cause damage to the sensor.

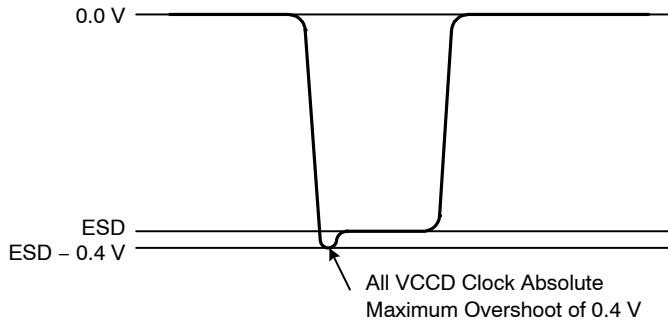


Notes:

1. Activate all other biases when ESD is stable and SUB is above 3 V.
2. Do not pulse the electronic shutter until ESD is stable.
3. VDD cannot be +15 V when SUB is 0 V.
4. The image sensor can be protected from an accidental improper ESD voltage by current limiting the SUB current to less than 10 mA. SUB and VDD must always be greater than GND. ESD must always be less than GND. Placing diodes between SUB, VDD, ESD and ground will protect the sensor from accidental overshoots of SUB, VDD and ESD during power on and power off. See the figure below.

**Figure 15. Power-Up and Power-Down Sequence**

The VCCD clock waveform must not have a negative overshoot more than 0.4 V below the ESD voltage.



**Figure 16. VCCD Clock Waveform**

Example of external diode protection for SUB, VDD and ESD.  $\alpha$  denotes a, b, c or d.



**Figure 17. Example of External Diode Protection**

DC Bias Operating Conditions

Table 14. DC BIAS OPERATING CONDITIONS

| Description             | Pins         | Symbol           | Min. | Nom.            | Max.             | Unit | Max. DC Current | Notes   |
|-------------------------|--------------|------------------|------|-----------------|------------------|------|-----------------|---------|
| Reset Drain             | RD $\alpha$  | RD               | 11.8 | 12.0            | 12.2             | V    | 10 $\mu$ A      | 1       |
| Output Gate             | OG $\alpha$  | OG               | -2.2 | -2.0            | -1.8             | V    | 10 $\mu$ A      | 1       |
| Output Amplifier Supply | VDD $\alpha$ | V <sub>DD</sub>  | 14.5 | 15.0            | 15.5             | V    | 11.0 mA         | 1, 2    |
| Ground                  | GND          | GND              | 0.0  | 0.0             | 0.0              | V    | -1.0 mA         |         |
| Substrate               | SUB          | V <sub>SUB</sub> | 5.0  | V <sub>AB</sub> | V <sub>DD</sub>  | V    | 50 $\mu$ A      | 3, 8    |
| ESD Protection Disable  | ESD          | ESD              | -9.5 | -9.0            | V <sub>X_L</sub> | V    | 50 $\mu$ A      | 6, 7, 9 |
| Output Bias Current     | VOU $\alpha$ | I <sub>OUT</sub> | -3.0 | -7.0            | -10.0            | mA   | -               | 1, 4, 5 |

- $\alpha$  denotes a, b, c or d.
- The maximum DC current is for one output. I<sub>DD</sub> = I<sub>OUT</sub> + I<sub>SS</sub>. See Figure 18.
- The operating value of the substrate voltage, V<sub>AB</sub>, will be marked on the shipping container for each device. The value of V<sub>AB</sub> is set such that the photodiode charge capacity is the nominal P<sub>Ne</sub> (see Specifications).
- An output load sink must be applied to each VOUT pin to activate each output amplifier.
- Nominal value required for 40 MHz operation per output. May be reduced for slower data rates and lower noise.
- Adherence to the power-up and power-down sequence is critical. See Power Up and Power Down Sequence section.
- ESD maximum value must be less than or equal to V1\_L + 0.4 V and V2\_L + 0.4 V.
- Refer to Application Note *Using Interline CCD Image Sensors in High Intensity Visible Lighting Conditions*.
- Where V<sub>x\_L</sub> is the level set for V1\_L, V2\_L, V3\_L, or V4\_L in the application.

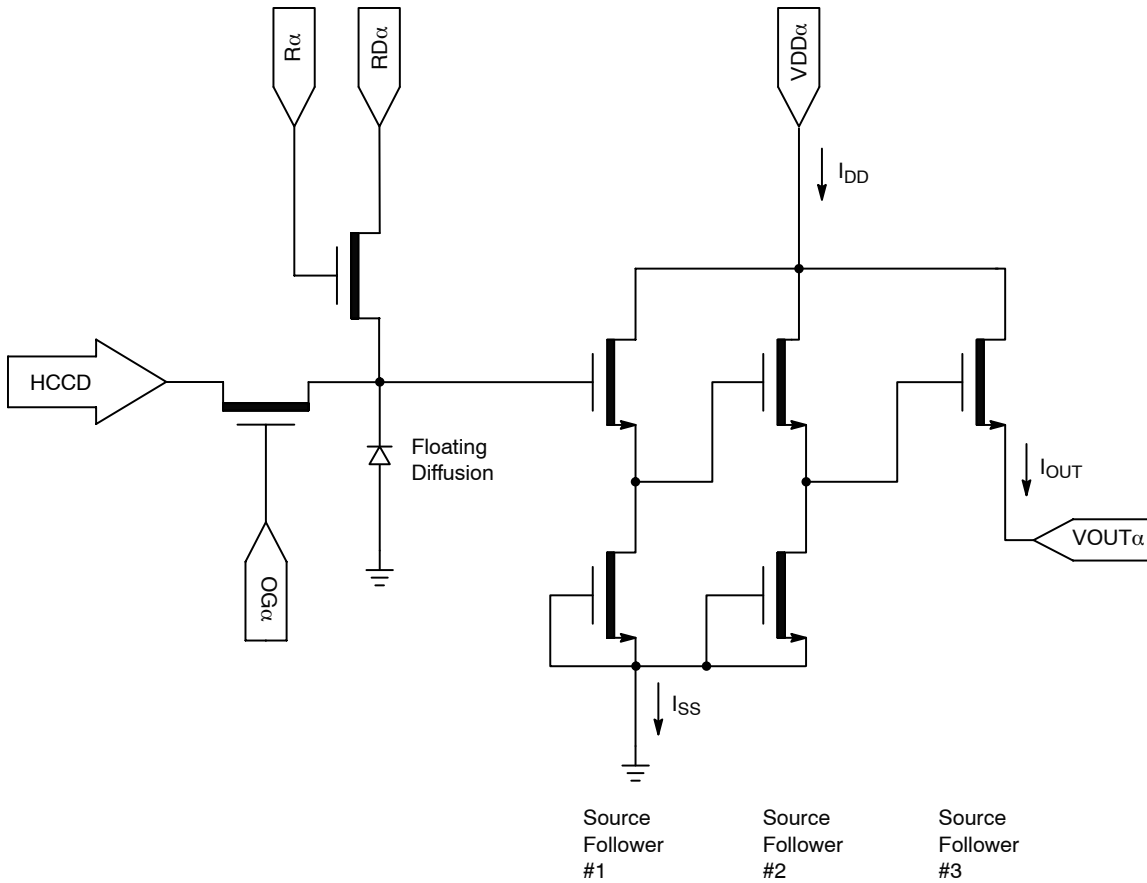


Figure 18. Output Amplifier

## AC Operating Conditions

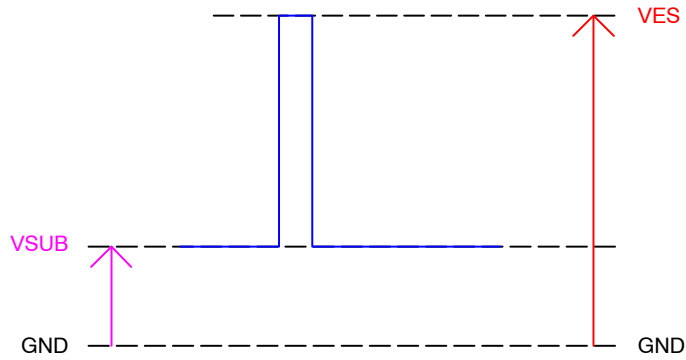
Table 15. CLOCK LEVELS

| Description  | Pins<br>(Note 1) | Symbol          | Level     | Min.             | Nom. | Max.            | Unit | Capacitance<br>(Note 2) |
|--|------------------|-----------------|-----------|------------------|------|-----------------|------|-------------------------|
| Vertical CCD Clock, Phase 1                          | V1B, V1T         | V1_L            | Low       | -8.2             | -8.0 | -7.8            | V    | 11 nF<br>(Note 6)       |
|  |                  | V1_M            | Mid       | -0.2             | 0.0  | 0.2             |      |                         |
|  |                  | V1_H            | High      | 11.5             | 12.0 | 12.5            |      |                         |
| Vertical CCD Clock, Phase 2                          | V2B, V2T         | V2_L            | Low       | -8.2             | -8.0 | -7.8            | V    | 11 nF<br>(Note 6)       |
|  |                  | V2_H            | High      | -0.2             | 0.0  | 0.2             |      |                         |
| Vertical CCD Clock, Phase 3                          | V3B, V3T         | V3_L            | Low       | -8.2             | -8.0 | -7.8            | V    | 11 nF<br>(Note 6)       |
|  |                  | V3_H            | High      | -0.2             | 0.0  | 0.2             |      |                         |
| Vertical CCD Clock, Phase 4                          | V4B, V4T         | V4_L            | Low       | -8.2             | -8.0 | -7.8            | V    | 11 nF<br>(Note 6)       |
|  |                  | V4_H            | High      | -0.2             | 0.0  | 0.2             |      |                         |
| Horizontal CCD Clock,<br>Phase 1 Storage             | H1S $\alpha$     | H1S_L           | Low       | -5.2<br>(Note 7) | -4.0 | -3.8            | V    | 140 pF<br>(Note 6)      |
|  |                  | H1S_A           | Amplitude | 3.8              | 4.0  | 5.2<br>(Note 7) |      |                         |
| Horizontal CCD Clock,<br>Phase 1 Barrier             | H1B $\alpha$     | H1B_L           | Low       | -5.2<br>(Note 7) | -4.0 | -3.8            | V    | 93 pF<br>(Note 6)       |
|  |                  | H1B_A           | Amplitude | 3.8              | 4.0  | 5.2<br>(Note 7) |      |                         |
| Horizontal CCD Clock,<br>Phase 2 Storage             | H2S $\alpha$     | H2S_L           | Low       | -5.2<br>(Note 7) | -4.0 | -3.8            | V    | 140 pF<br>(Note 6)      |
|  |                  | H2S_A           | Amplitude | 3.8              | 4.0  | 5.2<br>(Note 7) |      |                         |
| Horizontal CCD Clock,<br>Phase 2 Barrier             | H2B $\alpha$     | H2B_L           | Low       | -5.2<br>(Note 7) | -4.0 | -3.8            | V    | 93 pF<br>(Note 6)       |
|  |                  | H2B_A           | Amplitude | 3.8              | 4.0  | 5.2<br>(Note 7) |      |                         |
| Horizontal CCD Clock,<br>Phase 2 Last Phase (Note 3) | H2SL $\alpha$    | H2SL_L          | Low       | -5.2             | -5.0 | -4.8            | V    | 20 pF<br>(Note 6)       |
|  |                  | H2SL_A          | Amplitude | 4.8              | 5.0  | 5.2             |      |                         |
| Reset Gate   | R $\alpha$       | R_L<br>(Note 4) | Low       | -3.5             | -2.0 | -1.5            | V    | 16 pF<br>(Note 6)       |
|  |                  | R_H             | High      | 2.5              | 3.0  | 4.0             |      |                         |
| Electronic Shutter (Note 5)                          | SUB              | VES             | High      | 29.0             | 30.0 | 40.0            | V    | 700 pF<br>(Note 6)      |

- $\alpha$  denotes a, b, c or d.
- Capacitance is total for all like named pins.
- Use separate clock driver for improved speed performance.
- Reset low should be set to -3 V for signal levels greater than 40,000 electrons.
- Refer to Application Note *Using Interline CCD Image Sensors in High Intensity Visible Lighting Conditions*.
- Capacitance values are estimated.
- If the minimum horizontal clock low level is used (-5.2 V), then the maximum horizontal clock amplitude should be used (5.2 V amplitude) to create a -5.2 V to 0.0 V clock. If a 5 V clock driver is used, the horizontal low level should be set to -5.0 V and the high level should be a set to 0.0 V.

# KAI-02050

The figure below shows the DC bias (V<sub>SUB</sub>) and AC clock (V<sub>ES</sub>) applied to the SUB pin. Both the DC bias and AC clock are referenced to ground.



**Figure 19. DC Bias and AC Clock Applied to the SUB Pin**

## Device Identification

The device identification pin (DevID) may be used to determine which 5.5 micron pixel interline CCD sensor is being used.

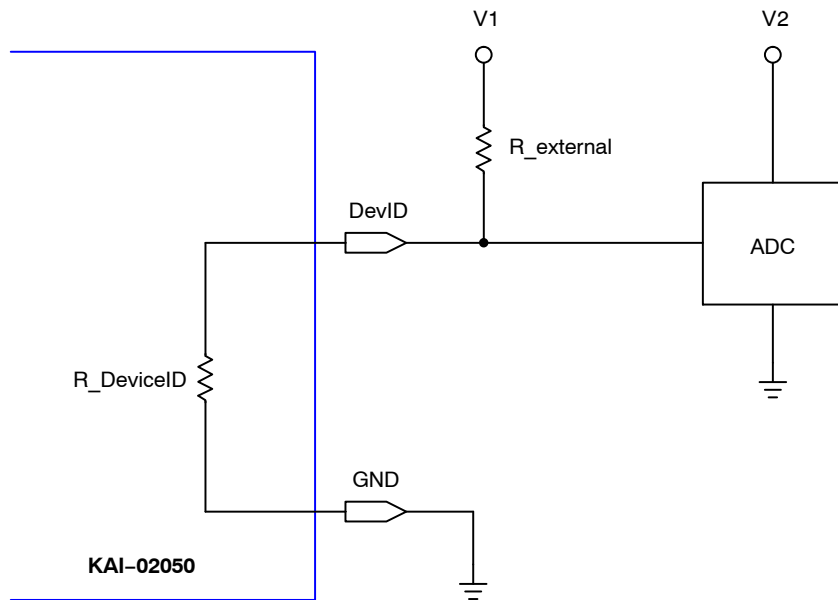
**Table 16.**

| Description           | Pins  | Symbol | Min.   | Nom.    | Max.    | Unit | Max. DC Current | Notes   |
|-----------------------|-------|--------|--------|---------|---------|------|-----------------|---------|
| Device Identification | DevID | DevID  | 86,000 | 108,000 | 130,000 | Ω    | 50 μA           | 1, 2, 3 |

1. Nominal value subject to verification and/or change during release of preliminary specifications.
2. If the Device Identification is not used, it may be left disconnected.
3. After Device Identification resistance has been read during camera initialization, it is recommended that the circuit be disabled to prevent localized heating of the sensor due to current flow through the R<sub>DevID</sub> resistor.

## Recommended Circuit

Note that V1 must be a different value than V2.



**Figure 20. Device Identification Recommended Circuit**



## TIMING

Table 17. REQUIREMENTS AND CHARACTERISTICS (Note 1)

| Description            | Symbol           | Min. | Nom. | Max. | Unit          | Notes               |
|------------------------|------------------|------|------|------|---------------|---------------------|
| Photodiode Transfer    | $t_{PD}$         | 1.0  | -    | -    | $\mu\text{s}$ |                     |
| VCCD Leading Pedestal  | $t_{3P}$         | 4.0  | -    | -    | $\mu\text{s}$ |                     |
| VCCD Trailing Pedestal | $t_{3D}$         | 4.0  | -    | -    | $\mu\text{s}$ |                     |
| VCCD Transfer Delay    | $t_D$            | 1.0  | -    | -    | $\mu\text{s}$ |                     |
| VCCD Transfer          | $t_V$            | 1.0  | -    | -    | $\mu\text{s}$ |                     |
| VCCD Clock Cross-Over  | $V_{VCR}$        | 75   | -    | 100  | %             |                     |
| VCCD Rise, Fall Times  | $t_{VR}, t_{VF}$ | 5    | -    | 10   | %             | 2, 3                |
| HCCD Delay             | $t_{HS}$         | 0.2  | -    | -    | $\mu\text{s}$ |                     |
| HCCD Transfer          | $t_e$            | 25.0 | -    | -    | ns            |                     |
| Shutter Transfer       | $t_{SUB}$        | 1.0  | -    | -    | $\mu\text{s}$ |                     |
| Shutter Delay          | $t_{HD}$         | 1.0  | -    | -    | $\mu\text{s}$ |                     |
| Reset Pulse            | $t_R$            | 2.5  | -    | -    | ns            |                     |
| Reset – Video Delay    | $t_{RV}$         | -    | 2.2  | -    | ns            |                     |
| H2SL – Video Delay     | $t_{HV}$         | -    | 3.1  | -    | ns            |                     |
| Line Time              | $t_{LINE}$       | 23.0 | -    | -    | $\mu\text{s}$ | Dual HCCD Readout   |
|                        |                  | 44.1 | -    | -    | $\mu\text{s}$ | Single HCCD Readout |
| Frame Time             | $t_{FRAME}$      | 14.6 | -    | -    | ms            | Quad HCCD Readout   |
|                        |                  | 29.1 | -    | -    | ms            | Dual HCCD Readout   |
|                        |                  | 55.7 | -    | -    | ms            | Single HCCD Readout |

1. Refer to timing diagrams as shown in Figure 21, Figure 22, Figure 23, Figure 24 and Figure 25.
2. Refer to Figure 25: VCCD Clock Edge Alignment.
3. Relative to the pulse width.

**Timing Diagrams**

The timing sequence for the clocked device pins may be represented as one of seven patterns (P1–P7) as shown in the table below. The patterns are defined in Figure 21 and

Figure 22. Contact ON Semiconductor Application Engineering for other readout modes.

**Table 18. TIMING DIAGRAMS**

| Device Pin    | Quad Readout | Dual Readout<br>VOUTa, VOUTb | Dual Readout<br>VOUTa, VOUTc | Single Readout<br>VOUTa     |
|---------------|--------------|------------------------------|------------------------------|-----------------------------|
| V1T           | P1T          | P1B                          | P1T                          | P1B                         |
| V2T           | P2T          | P4B                          | P2T                          | P4B                         |
| V3T           | P3T          | P3B                          | P3T                          | P3B                         |
| V4T           | P4T          | P2B                          | P4T                          | P2B                         |
| V1B           | P1B          |                              |                              |                             |
| V2B           | P2B          |                              |                              |                             |
| V3B           | P3B          |                              |                              |                             |
| V4B           | P4B          |                              |                              |                             |
| H1Sa          | P5           |                              |                              |                             |
| H1Ba          | P5           |                              |                              |                             |
| H2Sa (Note 2) | P6           |                              |                              |                             |
| H2Ba          | P6           |                              |                              |                             |
| Ra            | P7           |                              |                              |                             |
| H1Sb          | P5           | P5                           |                              |                             |
| H1Bb          | P5           | P6                           |                              |                             |
| H2Sb (Note 2) | P6           | P6                           |                              |                             |
| H2Bb          | P6           | P5                           |                              |                             |
| Rb            | P7           | P7 (Note 1) or Off (Note 3)  |                              | P7 (Note 1) or Off (Note 3) |
| H1Sc          | P5           | P5 (Note 1) or Off (Note 3)  | P5                           | P5 (Note 1) or Off (Note 3) |
| H1Bc          | P5           | P5 (Note 1) or Off (Note 3)  | P5                           | P5 (Note 1) or Off (Note 3) |
| H2Sc (Note 2) | P6           | P6 (Note 1) or Off (Note 3)  | P6                           | P6 (Note 1) or Off (Note 3) |
| H2Bc          | P6           | P6 (Note 1) or Off (Note 3)  | P6                           | P6 (Note 1) or Off (Note 3) |
| Rc            | P7           | P7 (Note 1) or Off (Note 3)  | P7                           | P7 (Note 1) or Off (Note 3) |
| H1Sd          | P5           | P5 (Note 1) or Off (Note 3)  | P5                           | P5 (Note 1) or Off (Note 3) |
| H1Bd          | P5           | P5 (Note 1) or Off (Note 3)  | P6                           | P5 (Note 1) or Off (Note 3) |
| H2Sd (Note 2) | P6           | P6 (Note 1) or Off (Note 3)  | P6                           | P6 (Note 1) or Off (Note 3) |
| H2Bd          | P6           | P6 (Note 1) or Off (Note 3)  | P5                           | P6 (Note 1) or Off (Note 3) |
| Rd            | P7           | P7 (Note 1) or Off (Note 3)  | P7 (Note 1) or Off (Note 3)  | P7 (Note 1) or Off (Note 3) |

|                        |     |      |      |      |
|------------------------|-----|------|------|------|
| #Lines/Frame (Minimum) | 632 | 1264 | 632  | 1264 |
| #Pixels/Line (Minimum) | 853 |      | 1706 |      |

1. For optimal performance of the sensor. May be clocked at a lower frequency. If clocked at a lower frequency, the frequency selected should be a multiple of the frequency used on the a and b register.
2. H2SLx follows the same pattern as H2Sx For optimal speed performance, use a separate clock driver.
3. Off = +5 V. Note that there may be operating conditions (high temperature and/or very bright light sources) that will cause blooming from the unused c/d register into the image area.

**Photodiode Transfer Timing**

A row of charge is transferred to the HCCD on the falling edge of V1 as indicated in the P1 pattern below. Using this timing sequence, the leading dummy row or line is combined with the first dark row in the HCCD. The “Last Line” is dependent on readout mode – either 632 or 1264 minimum counts required. It is important to note that, in

general, the rising edge of a vertical clock (patterns P1-P4) should be coincident or slightly leading a falling edge at the same time interval. This is particularly true at the point where P1 returns from the high (3<sup>rd</sup> level) state to the mid-state when P4 transitions from the low state to the high state.

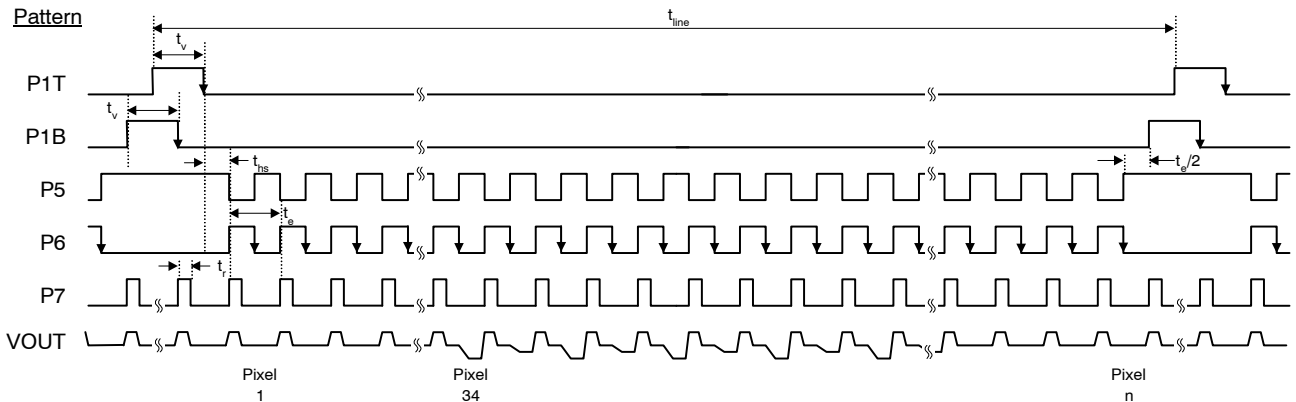


**Figure 21. Photodiode Transfer Timing**

**Line and Pixel Timing**

Each row of charge is transferred to the output, as illustrated below, on the falling edge of H2SL (indicated as

P6 pattern). The number of pixels in a row is dependent on readout mode – either 853 or 1706 minimum counts required.



**Figure 22. Line and Pixel Timing**

Pixel Timing Detail

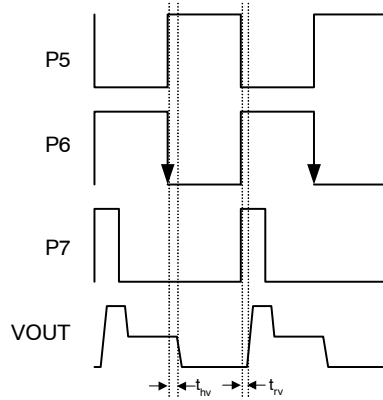


Figure 23. Pixel Timing Detail

Frame/Electronic Shutter Timing

The SUB pin may be optionally clocked to provide electronic shuttering capability as shown below. The resulting photodiode integration time is defined from the falling edge of SUB to the falling edge of V1 (P1 pattern).

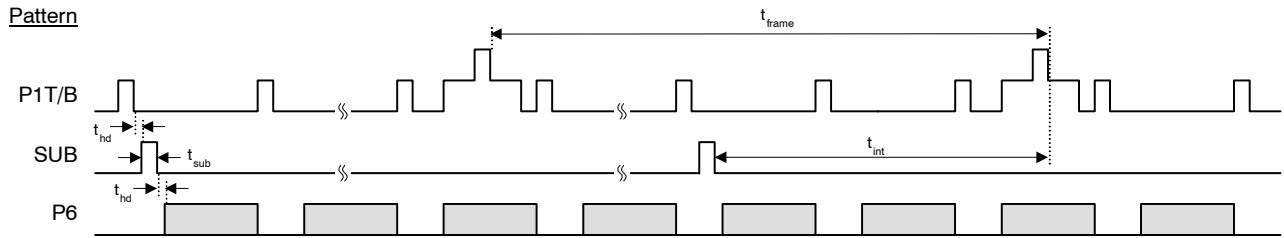


Figure 24. Frame/Electronic Shutter Timing

VCCD Clock Edge Alignment

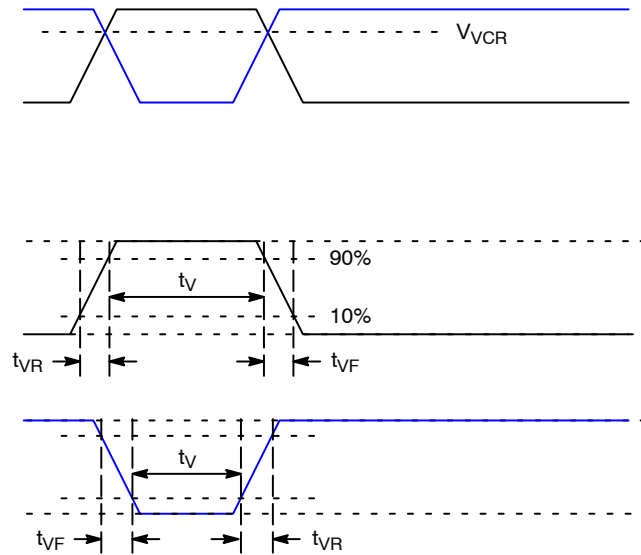


Figure 25. VCCD Clock Edge Alignment

Line and Pixel Timing – Vertical Binning by 2

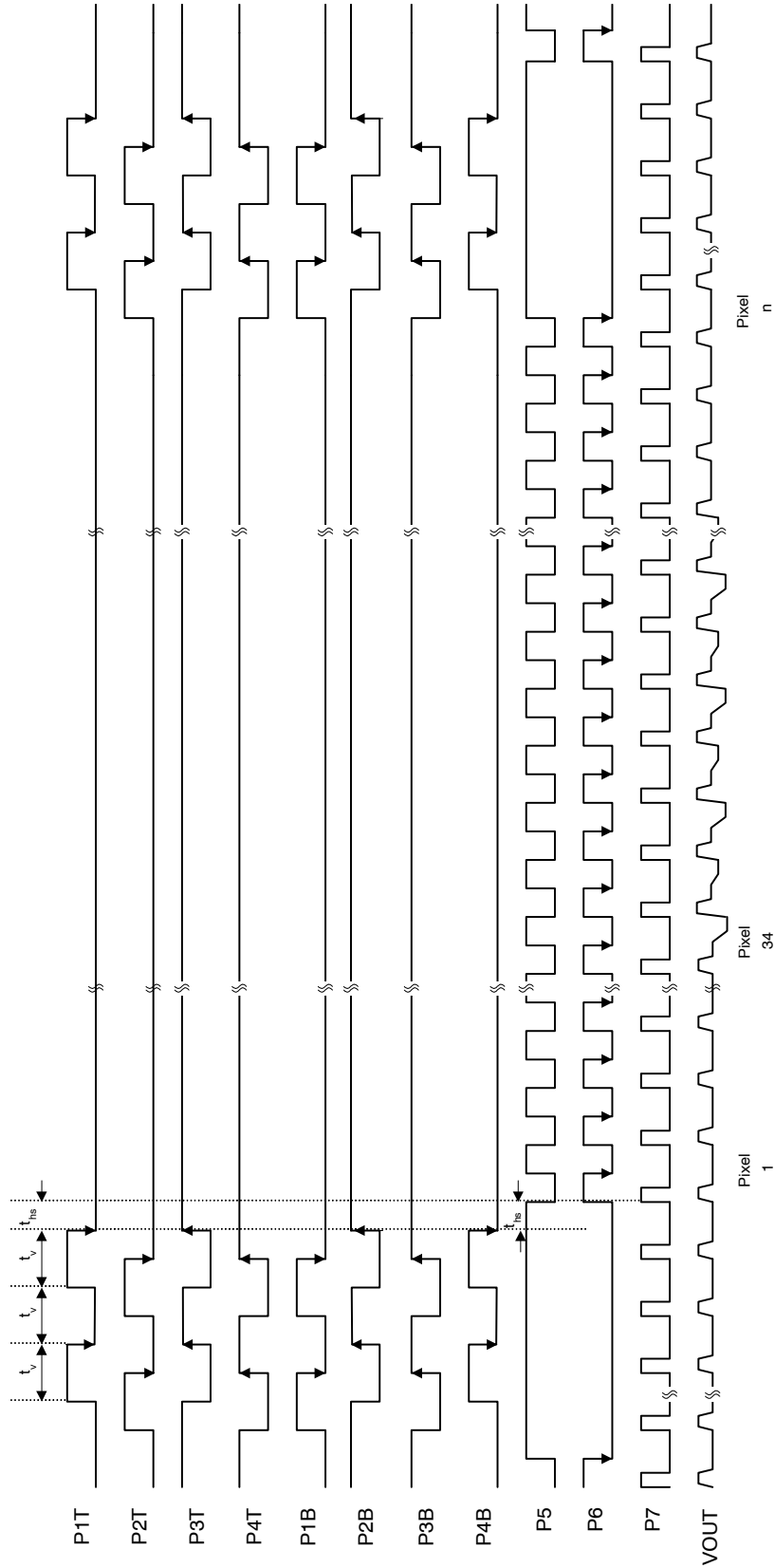


Figure 26. Line and Pixel Timing – Vertical Binning by 2

## STORAGE AND HANDLING

Table 19. STORAGE CONDITIONS

| Description         | Symbol          | Minimum | Maximum | Unit | Notes |
|---------------------|-----------------|---------|---------|------|-------|
| Storage Temperature | T <sub>ST</sub> | -55     | 80      | °C   | 1     |
| Humidity            | RH              | 5       | 90      | %    | 2     |

1. Long-term storage toward the maximum temperature will accelerate color filter degradation.
2. T = 25°C. Excessive humidity will degrade MTTF.

For information on ESD and cover glass care and cleanliness, please download the *Image Sensor Handling and Best Practices* Application Note (AN52561/D) from [www.onsemi.com](http://www.onsemi.com).

For information on environmental exposure, please download the *Using Interline CCD Image Sensors in High Intensity Lighting Conditions* Application Note (AND9183/D) from [www.onsemi.com](http://www.onsemi.com).

For information on soldering recommendations, please download the *Soldering and Mounting Techniques Reference Manual* (SOLDERRM/D) from [www.onsemi.com](http://www.onsemi.com).

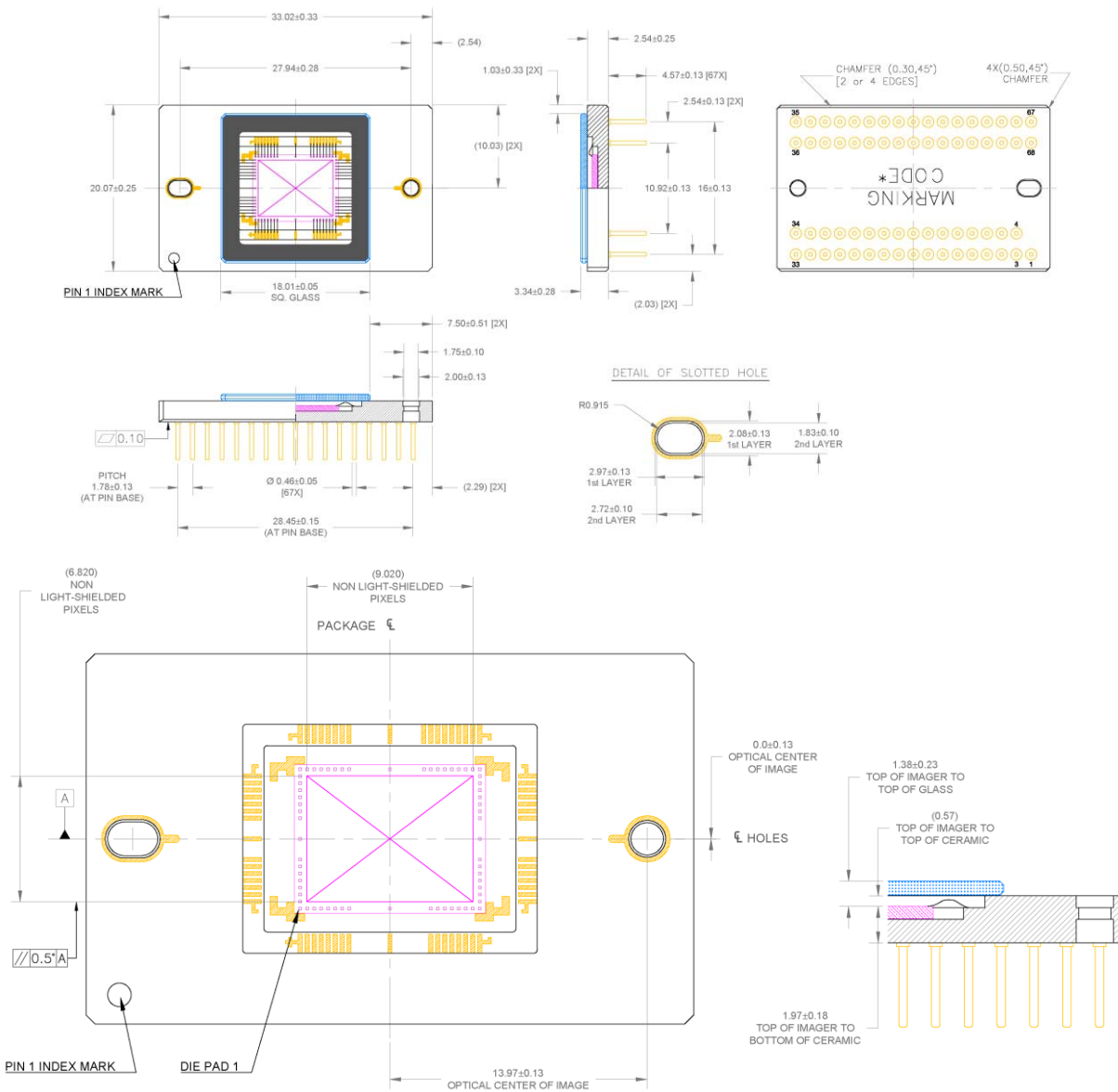
For quality and reliability information, please download the *Quality & Reliability Handbook* (HBD851/D) from [www.onsemi.com](http://www.onsemi.com).

For information on device numbering and ordering codes, please download the *Device Nomenclature* technical note (TND310/D) from [www.onsemi.com](http://www.onsemi.com).

For information on Standard terms and Conditions of Sale, please download [Terms and Conditions](http://www.onsemi.com) from [www.onsemi.com](http://www.onsemi.com).

MECHANICAL INFORMATION

PGA Completed Assembly

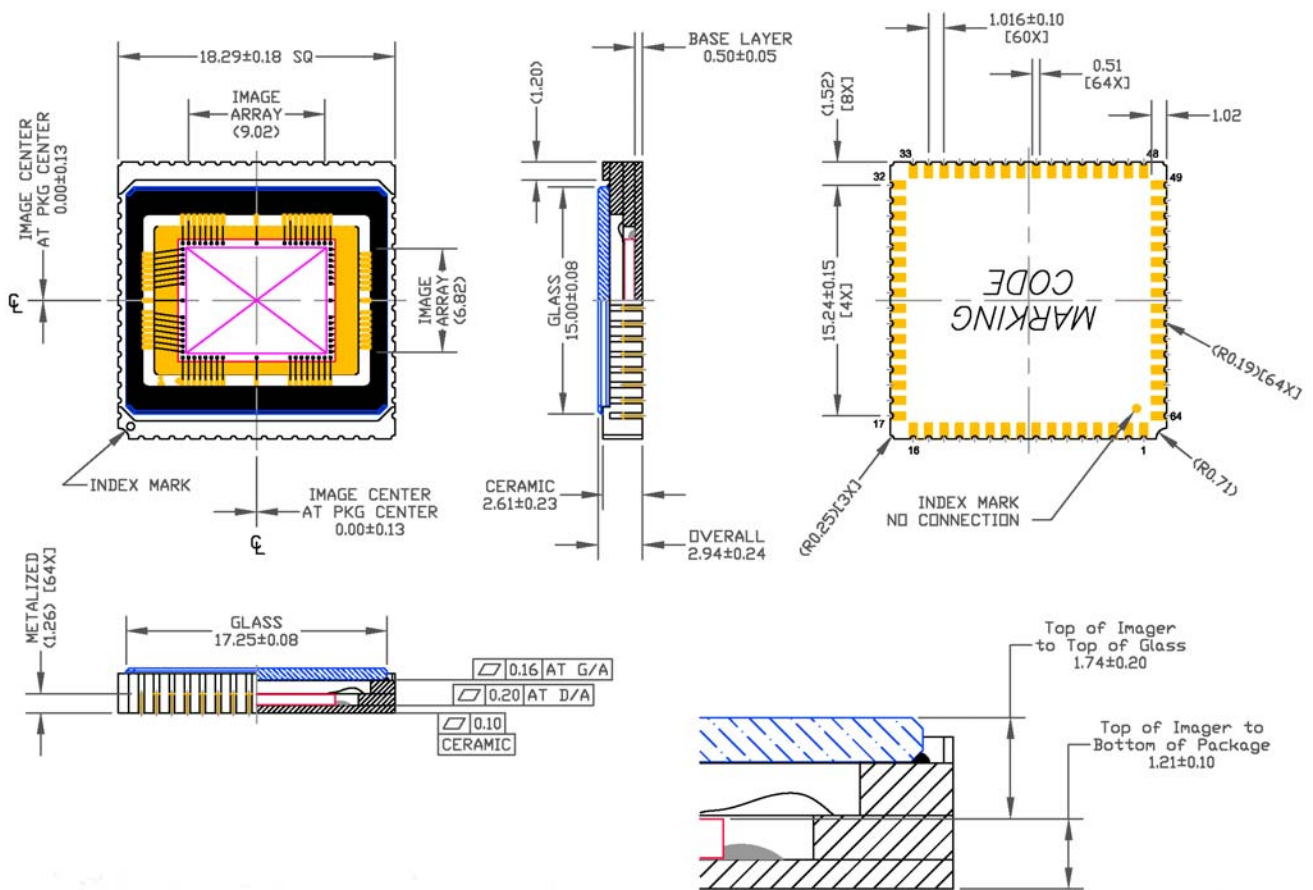


Notes:

1. See Ordering Information for marking code.
2. No materials to interfere with clearance through guide holes.
3. The center of the active image is nominally at the center of the package.
4. Die rotation < 0.5 degrees.
5. Glass rotation < 1.5 degrees with respect to package outer edges for all sealed configurations.
6. Internal traces may be exposed on sides of package. Do not allow metal to contact sides of ceramic package.
7. Recommended mounting screws: 1.6 × 0.35 mm (ISO Standard); 0-80 (Unified Fine Thread Standard).
8. Units: millimeters.

Figure 27. PGA Completed Assembly

CLCC Completed Assembly



Notes:

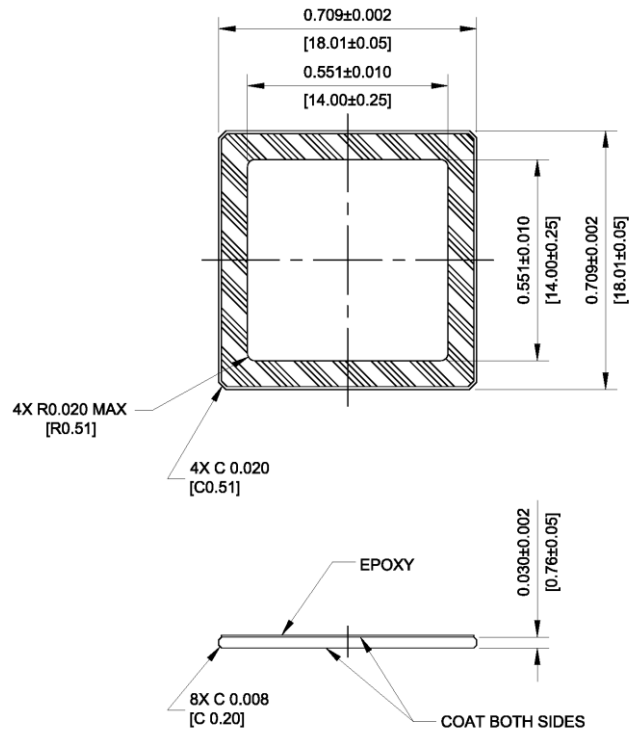
1. See Ordering Information for marking code.
2. Die rotation  $< 0.5$  degrees.
3. Units: millimeters.

Figure 28. CLCC Completed Assembly



# KAI-02050

## PGA MAR Cover Glass

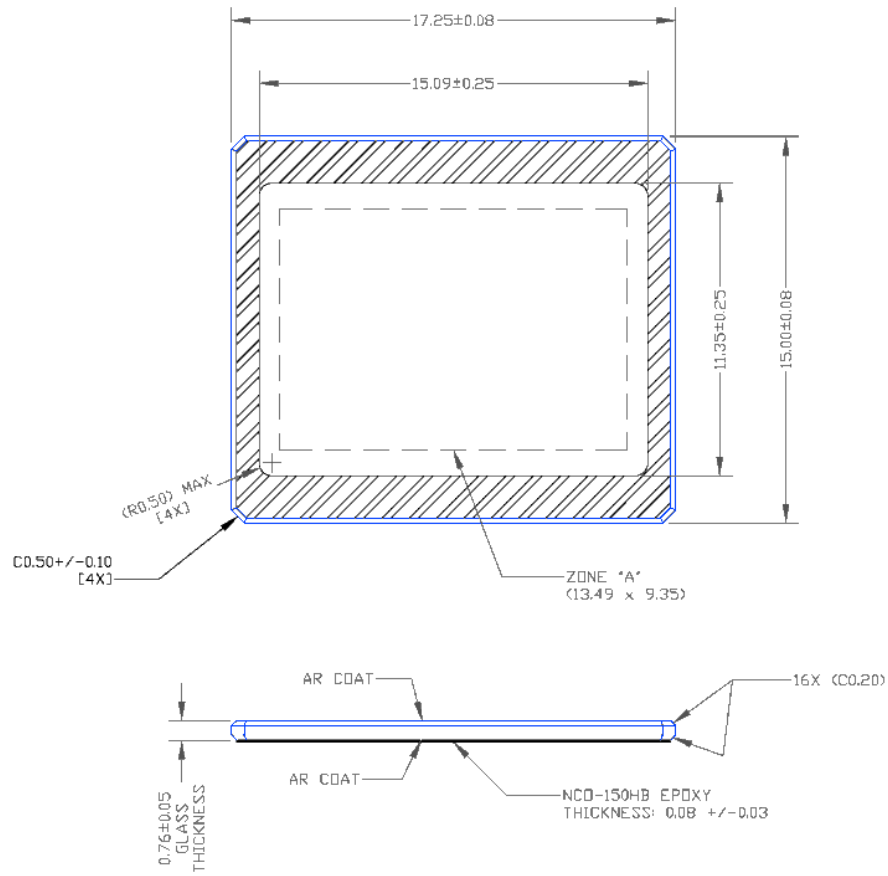


### Notes:

1. Dust/Scratch Count – 12 micron maximum
2. Units: IN [MM]
3. Reflectance Specification
  - a. 420 nm to 435 nm < 2.0%
  - b. 435 nm to 630 nm < 0.8%
  - c. 630 nm to 680 nm < 2.0%

Figure 29. PGA MAR Cover Glass

CLCC MAR Cover Glass

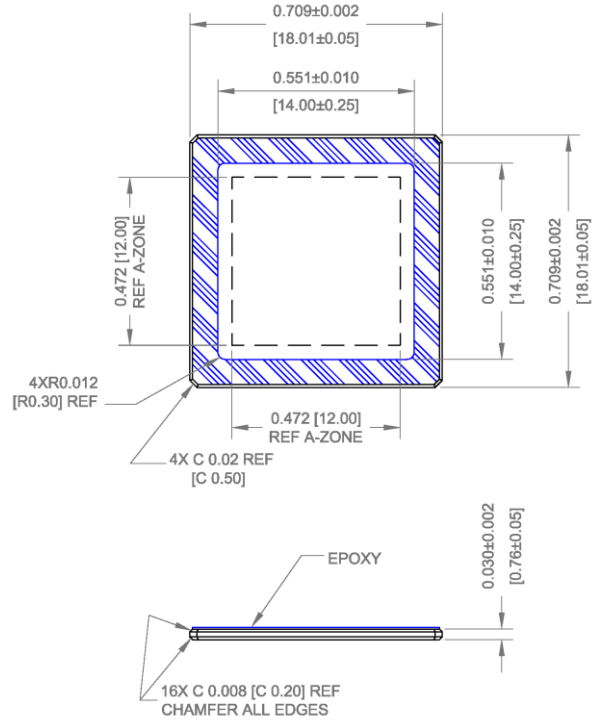


Notes:

1. Dust/Scratch Count – 12 micron maximum
2. Units: millimeter
3. Reflectance Specification
  - a. 420 nm to 435 nm < 2.0%
  - b. 435 nm to 630 nm < 0.8%
  - c. 630 nm to 680 nm < 2.0%

Figure 30. CLCC MAR Cover Glass

PGA Clear Cover Glass

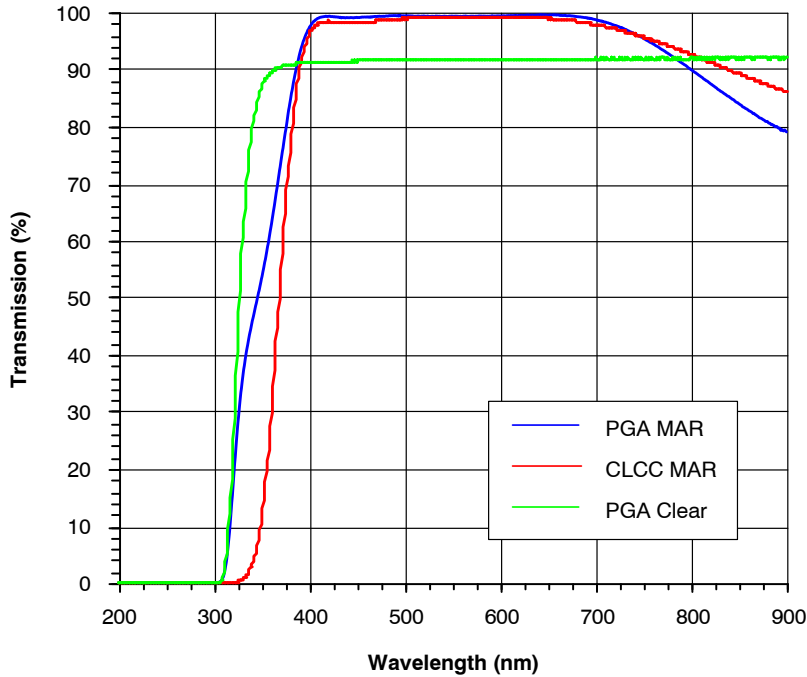


Notes:

1. Dust/Scratch Count – 12 micron maximum
2. Units: IN

Figure 31. PGA Clear Cover Glass

Cover Glass Transmission



NOTE: PGA and CLCC MAR transmission data differ due to in-spec differences from glass vendor.

Figure 32. Cover Glass Transmission

**SHIPPING CONFIGURATION**

**Cover Glass Protective Tape**

Cover glass protective tape, as shown in Figure 33, is utilized to help ensure the cleanliness of the cover glass during transportation and camera manufacturing. This protective tape is not intended to be optically correct, and

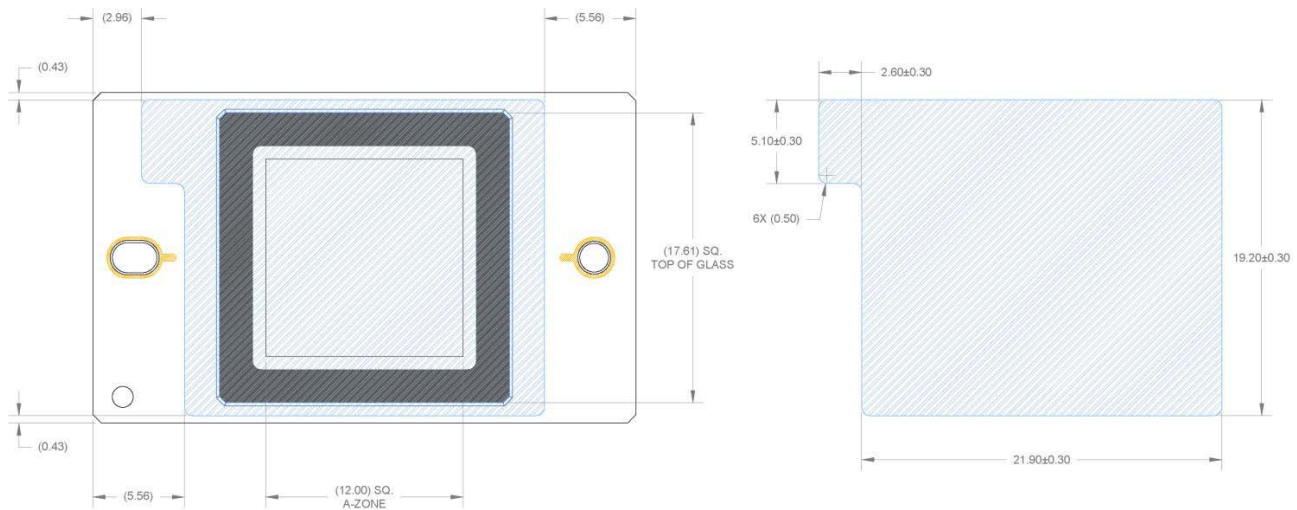
should be removed prior to any image testing. The protective tape should be removed in an ionized air stream to prevent static build-up and the attraction of particles. The following part numbers will have the protective tape applied:

**Table 20.**

| Part Number           | Description   |
|-----------------------|---|
| KAI-02050-CBA-JB-B2   | Color (Bayer RGB), Telecentric Microlens, PGA Package, Sealed Clear Cover Glass (No Coatings), Grade 2                  |
| KAI-02050-CBA-JB-AE   | Color (Bayer RGB), Telecentric Microlens, PGA Package, Sealed Clear Cover Glass (No Coatings), Engineering Grade        |
| KAI-02050-CBA-JB-B2-T | Color (Bayer RGB), Telecentric Microlens, PGA Package, Sealed Clear Cover Glass (No Coatings), Grade 2, Packed in Trays |

**Table 21.**

| Criteria     | Description   |
|--------------|---|
| Placement    | Per the drawing. The lid tape shall not overhang the edge of the package or mounting holes. The lid tape always overhangs the top of the glass (chamfers not included). |
| Tab Location | The tape tab is located near pin 68.  |
| Scratches    | The tape application equipment will make slight scratches on the lid tape. This is allowed.   |



**Figure 33. Cover Glass Protective Tape**

# KAI-02050

## Tray Packing

The following part numbers are packed in bricks of 6 trays, each tray containing 32 image sensors, for a total of

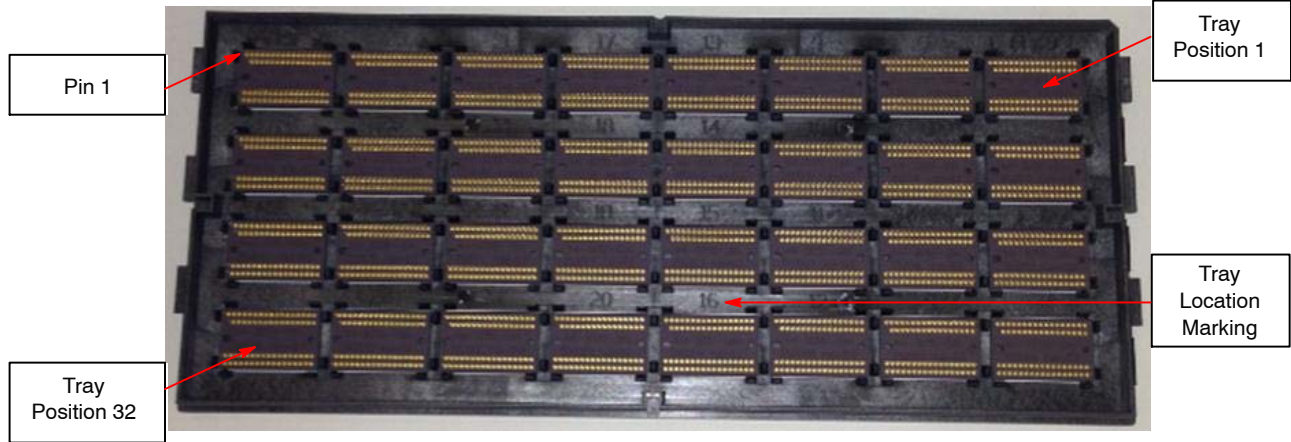
192 image sensors per brick. The minimum order and multiple quantities for this configuration are 192 image sensors.

**Table 22.**

| Part Number           | Description   |
|-----------------------|---|
| KAI-02050-CBA-JB-B2-T | Color (Bayer RGB), Telecentric Microlens, PGA Package, Sealed Clear Cover Glass (No Coatings), Grade 2, Packed in Trays |

## Tray Configuration

### Pin-Up View



**Figure 34. Tray Pin-Up View**

### Pin-Down View



**Figure 35. Tray Pin-Down View**

# KAI-02050

## Brick Configuration

Bricks consist of 6 full trays and 1 empty tray. Each tray contains 32 image sensors. There are a total of 192 image

sensors in the brick. The ID label is applied to the top of the brick. Tray 1 is at the bottom of the brick and the empty tray is at the top of the brick.

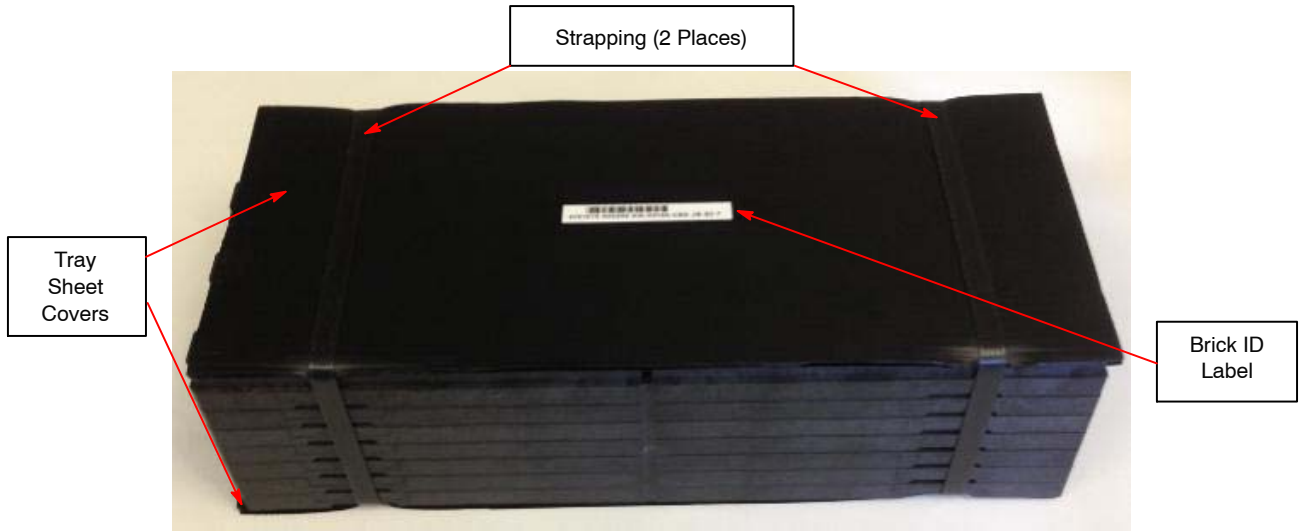


Figure 36. Brick

The Brick ID is Encoded in the Bar Code.



Figure 37. Brick ID Label

## Brick in Vacuum Sealed Bag



Figure 38. Sealed Brick

*Shipping Container*

Brick Loaded in Shipping Container



**Figure 39. Brick Loaded in Shipping Container**

Open Shipping Container with Parts List

The parts list (see Figure 43) details information for each sensor in the brick. The parts list includes the serial number, tray and location, and VAB value for each sensor.



**Figure 40. Open Shipping Container with Parts List**

Sealed Shipping Container

The Brick Label (see Figure 42) is applied to both ends of the shipping container.



**Figure 41. Sealed Shipping Container**



Brick Label



Figure 42. Brick Label

*Parts List*

The parts list details information for each sensor in the brick. The parts list includes the serial number, tray and location, and VAB value for each sensor. Additionally, the VAB value and serial number are encoded in the bar code.

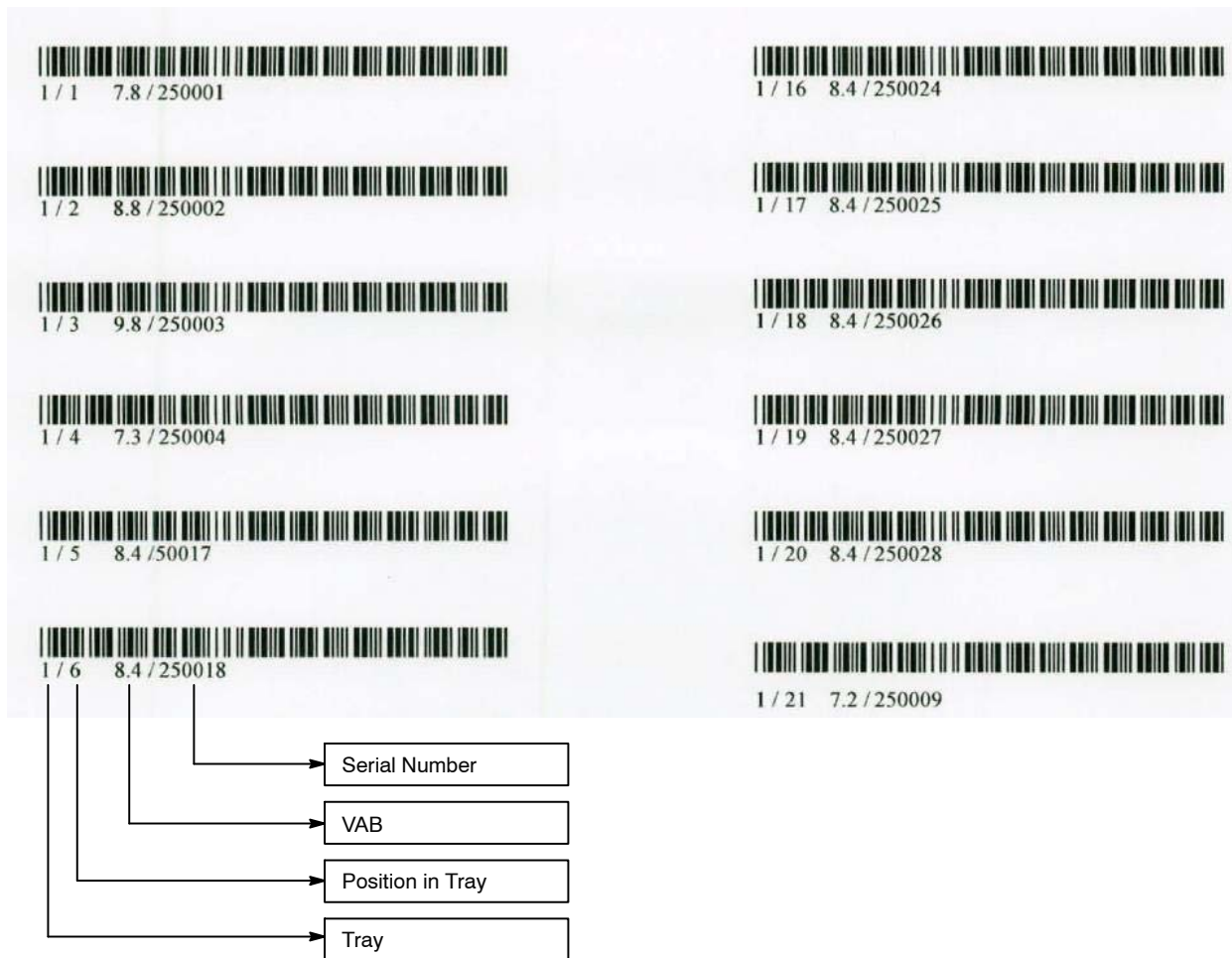



Figure 43. Parts List



ON Semiconductor and the  are registered trademarks of Semiconductor Components Industries, LLC (SCILLC) or its subsidiaries in the United States and/or other countries. SCILLC owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of SCILLC's product/patent coverage may be accessed at [www.onsemi.com/site/pdf/Patent-Marking.pdf](http://www.onsemi.com/site/pdf/Patent-Marking.pdf). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

## PUBLICATION ORDERING INFORMATION

### LITERATURE FULFILLMENT:

Literature Distribution Center for ON Semiconductor  
19521 E. 32nd Pkwy, Aurora, Colorado 80011 USA  
**Phone:** 303-675-2175 or 800-344-3860 Toll Free USA/Canada  
**Fax:** 303-675-2176 or 800-344-3867 Toll Free USA/Canada  
**Email:** [orderlit@onsemi.com](mailto:orderlit@onsemi.com)

**N. American Technical Support:** 800-282-9855 Toll Free  
USA/Canada  
**Europe, Middle East and Africa Technical Support:**  
Phone: 421 33 790 2910  
**Japan Customer Focus Center**  
Phone: 81-3-5817-1050

**ON Semiconductor Website:** [www.onsemi.com](http://www.onsemi.com)  
**Order Literature:** <http://www.onsemi.com/orderlit>  
For additional information, please contact your local  
Sales Representative

## Данный компонент на территории Российской Федерации

### Вы можете приобрести в компании MosChip.

Для оперативного оформления запроса Вам необходимо перейти по данной ссылке:

<http://moschip.ru/get-element>

Вы можете разместить у нас заказ для любого Вашего проекта, будь то серийное производство или разработка единичного прибора.

В нашем ассортименте представлены ведущие мировые производители активных и пассивных электронных компонентов.

Нашей специализацией является поставка электронной компонентной базы двойного назначения, продукции таких производителей как XILINX, Intel (ex.ALTERA), Vicor, Microchip, Texas Instruments, Analog Devices, Mini-Circuits, Amphenol, Glenair.

Сотрудничество с глобальными дистрибьюторами электронных компонентов, предоставляет возможность заказывать и получать с международных складов практически любой перечень компонентов в оптимальные для Вас сроки.

На всех этапах разработки и производства наши партнеры могут получить квалифицированную поддержку опытных инженеров.

Система менеджмента качества компании отвечает требованиям в соответствии с ГОСТ Р ИСО 9001, ГОСТ РВ 0015-002 и ЭС РД 009

### Офис по работе с юридическими лицами:

105318, г.Москва, ул.Щербаковская д.3, офис 1107, 1118, ДЦ «Щербаковский»

Телефон: +7 495 668-12-70 (многоканальный)

Факс: +7 495 668-12-70 (доб.304)

E-mail: [info@moschip.ru](mailto:info@moschip.ru)

Skype отдела продаж:

moschip.ru

moschip.ru\_4

moschip.ru\_6

moschip.ru\_9