Si3462 Evaluation Board User's Guide

1. Introduction

This document is intended to be used in conjunction with the Si3462 data sheet for designers interested in the following:

- An introduction to Power over Ethernet (PoE) and Power Sourcing Equipment (PSE) design considerations
- Operation of the Si3462 PSE controller in the Si3462-EVB reference design
- Configuration and operation of the Si3462-EVB

2. Overview of the Si3462 and Evaluation Board

The Si3462 is a single-port power management controller for IEEE 802.3at PoE/PoE+ compliant Power Sourcing Equipment (PSE). The Si3462 operates directly from a 50 V (nominal) isolated input for PoE or 54 V (nominal) isolated input for PoE+. The complete Si3462 reference design (i.e., the Si3462-EVB) also provides full IEEE-compliant classification and detection as well as a robust disconnect algorithm. Intelligent protection circuitry includes input under-voltage and over-voltage lockout (UVLO/OVLO), current limiting, and output short-circuit protection.

The Si3462 is designed to operate completely independently of host processor control. A reset button and an optional LED status signal are provided to indicate port status including detect, power good, and output fault event information.

The Si3462 is pin-programmable to support:

- No classification mode reduces bill of materials for 15.4 W operation and also for non-standard powered devices that do not present a proper classification signature
- Endpoint and midspan applications with support for either 10/100BASE-T or 10/100/1000BASE-T
- All PoE/PoE+ classification power levels
- Classification-based current limiting
- Automatic or manual restart after various fault events are detected

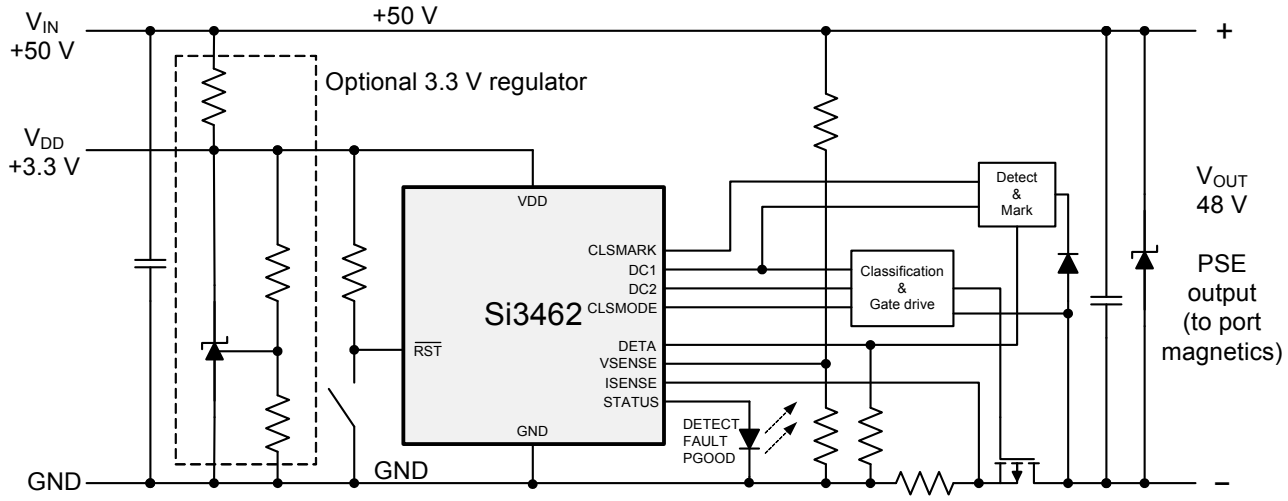

Figure 1. Typical Application Circuit
(Example is for PoE; for PoE+, use +54 V nominal V_{IN})

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3. Connectors and Switches

The Si3462-EVB is equipped with two banana jacks and an optional third banana jack on one side and two RJ-45 connectors on the other side.

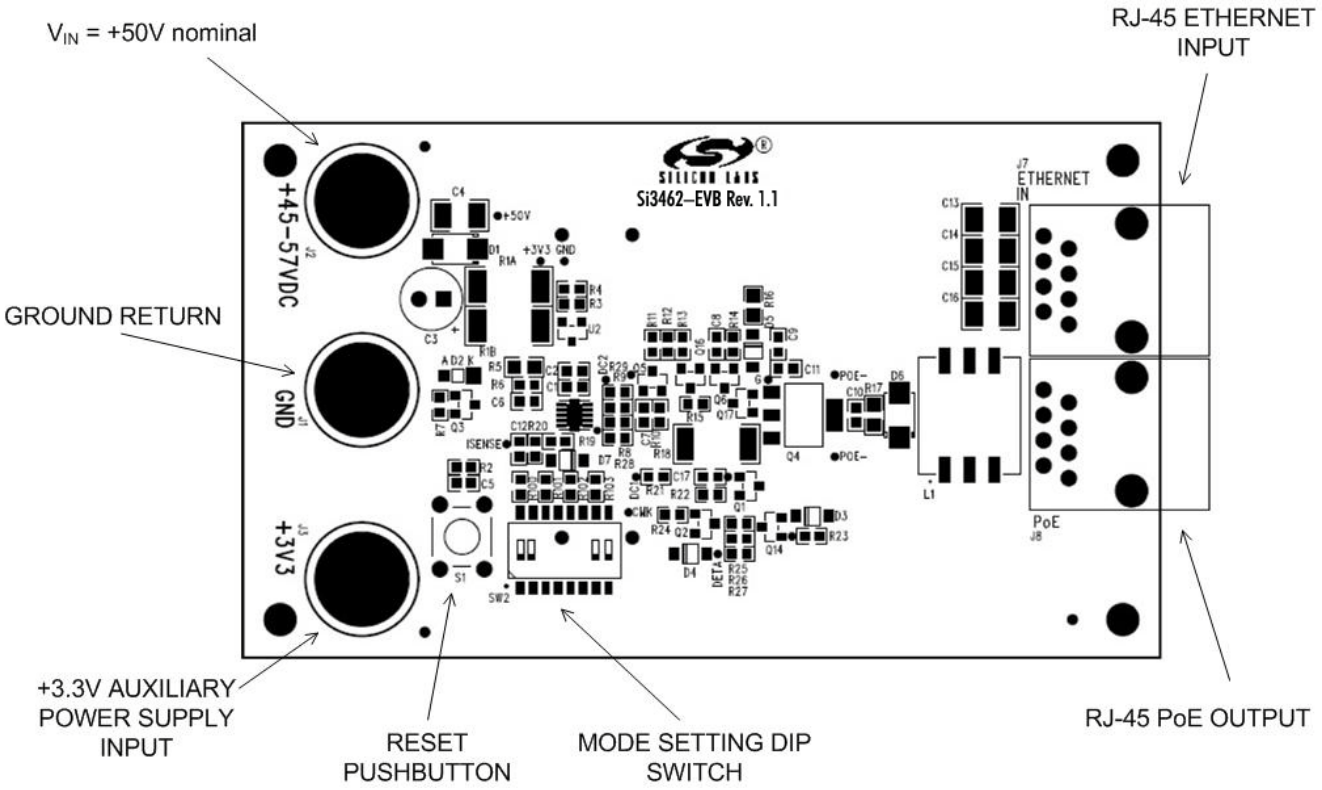

Figure 2. Placement of Connectors and Switches

The board receives power through the banana jacks:

- J1 BLACK banana jack: GND
- J2 RED banana jack: +50 V nominal input (+45 V to +57 V) for PoE;
  +54 V nominal input (+51 V to +57 V) for PoE+
- J3 Optional banana jack: +3.3 V input

An optional onboard +3.3 V shunt regulator generates the supply voltage for the Si3462 from the +50 V input voltage. The +3.3 V supply voltage may also be provided by an external source through the optional banana jack if higher efficiency is desired. In this case, the regulator and its associated resistors (including the series resistors) should be removed.

The RJ-45 Ethernet connectors:

- J7 ETHERNET IN input
- J8 PoE output

Reset pushbutton:

- SW1

Mode setting DIP switch:

- SW2 These switches set the operating mode according to Table 2 on page 7 including the following:
  - Available power level (4 W, 7 W, 15.4 W, and 30 W)
  - Midspan or Endpoint configuration
  - Automatic restart or restart after disconnection modes of operation

Refer to "6.1. Initialization and Operating Mode Configuration" on page 7 for more details.

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4. Quick Check of the Si3462 Evaluation Board

The only items needed to operate the Si3462 are an isolated 50 V power supply and connection cables (the Si3462-EVB comes with the optional onboard 3.3 V shunt regulator).

For a quick check of the board, perform the following steps:

- Ensure that the configuration DIP switch settings are in line with the powered device (PD) to be used (refer to "6.1. Initialization and Operating Mode Configuration" on page 7). Alternatively, for the purpose of this quick check, use the settings shown in Figure 3.
  - 30 W of available power
  - Midspan configuration
  - Automatic retry

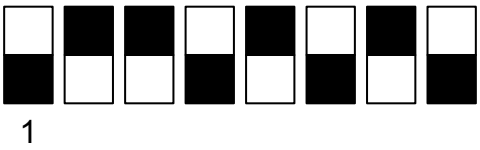

Figure 3. DIP Switch Settings

- Connect the 50 V power supply to the banana inputs observing the correct polarity (a series diode protects the board from damage in case of polarity reversal).
- Switch on the 50 V power supply. The status LED should flash at a 1.5 Hz rate signaling that the Si3462 is trying to detect a PD.
- Connect a PD to the PoE labeled RJ-45 connector. After a short time, power should be applied to the PD, and the status LED should turn continuously on. If the PD requests more power than the Si3462-EVB is configured for, power will be denied, or, if once powered and an overload condition occurs, power will be shut down, and the status LED will flash rapidly. Depending on initial configuration, the device may then automatically start detection after 2.2 seconds or wait until the Ethernet cable is removed (and plugged in again).

5. Introduction to PoE

IEEE 802.3 clause 33 is the standard for providing power to a remote Ethernet device on the same cable that is carrying data. The draft standard for higher power situations, often referred to as POE+, is 802.3at. The power is either carried common-mode on one of the data pairs (for 10/100/1000BASE-T) or on the spare pairs for 10/100BASE-T only applications. There are various different connection schemes depending on the pairs used to carry the power (Alternative A or B), the location of power insertion (Endpoint or Midspan), and 10BASE-T/100BASE-TX or 1000BASE-T compatibility.

The Si3462-EVB implements the configuration shown in Figure 4. Midspan PSE connection (Alternative B), but the Si3462 controller can be configured to operate in either Midspan or Endpoint applications and may be designed in applications using any pairs.

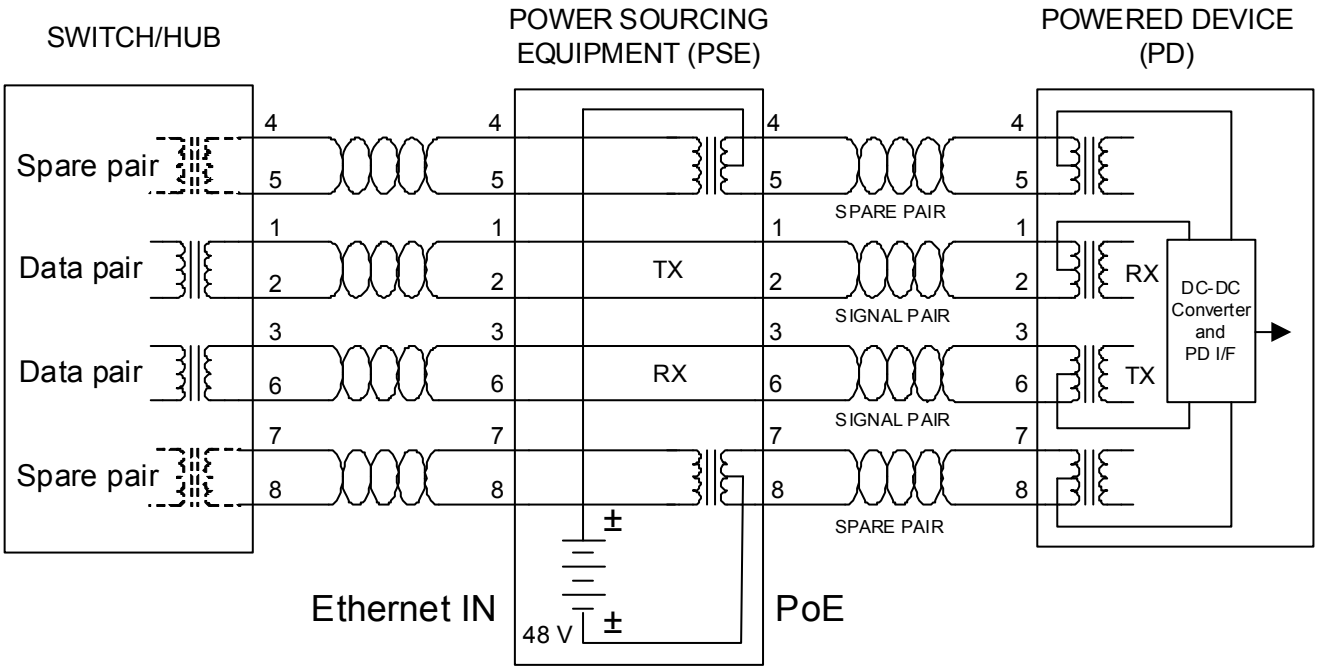

Figure 4. Midspan PSE Connection (Alternative B)*

***Note:** This is the connection scheme implemented on the Si3462-EVB reference design.

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5.1. PSE Detection, Classification, Power-Up, and Power Removal

The basic sequence for applying power is shown in Figure 5. The following is a description of the functions that must be performed in each phase.

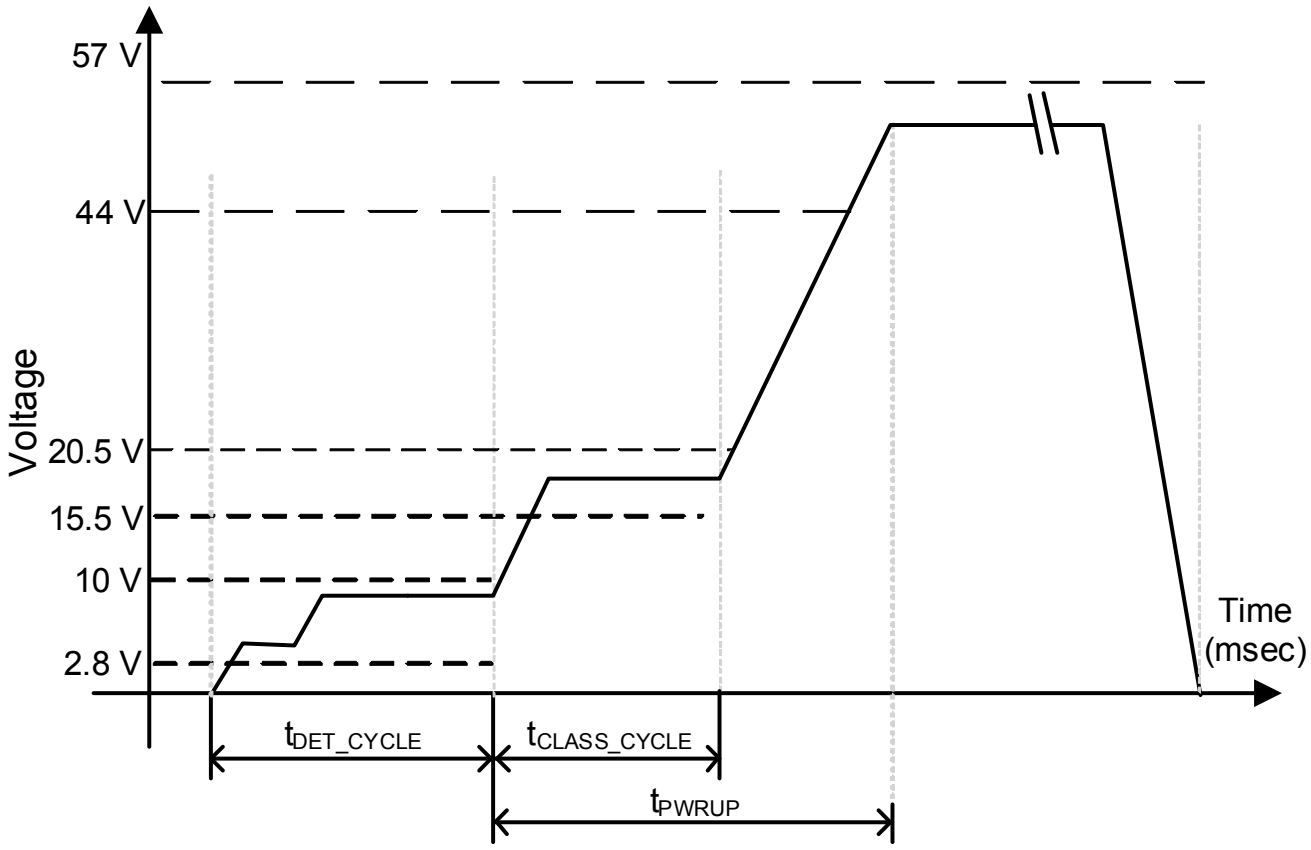

Figure 5. Detection, Classification, Power-Up, and Disconnect Sequence

5.1.1. Detection

During the detection phase, the PSE probes with limited current and voltage to determine if a 25 kΩ signature is present. A valid PD must present between 23.75 and 26.25 kΩ in the range of 2.8 to 10 V with an offset (due to the bridge diodes) of up to 1.9 V and a parallel capacitance of between 0.05 and 0.12 µF.

The Si3462-EVB uses a robust 3-point detection sequence to avoid inadvertently powering and damaging a non-PoE-enabled device.

For endpoint applications, detection must be completed within 500 ms of applying a valid signature. When configured as a midspan, there is a possibility that the PSE circuit will compete with an endpoint PSE, and, as required by the IEEE specifications, the Si3462 waits at least two seconds after an unsuccessful detection cycle to repeat the detection process.

5.1.2. Classification

Classification is performed by applying a voltage between 15.5 V and 20.5 V to the PD and measuring the current. The maximum power level that can be drawn by the PD is determined based on the current measured according to the information in Table 1.

Table 1. Classification Levels

ISENSE Current (Nominal)	Classification Level	Minimum Power Level
< 6.5 mA	Class 0	15.4 W
6.5 mA to 14.5 mA	Class 1	4 W
14.5 mA to 23 mA	Class 2	7 W
23 mA to 33 mA	Class 3	15.4 W
33 mA to 48 mA*	Class 4	26.4 W
***Note:** Currents above 45 mA may be treated as class level 0, which is 15.4 W.		

To save bill of materials cost, the Si3462 does not perform classification when configured for 15.4 W of output power. There is also a programmable mode for no classification and 30 W of output power to support non-standard PDs. If no classification is done, the classification components of the bill of materials do not need to be populated. The classification mark components only need to be populated for 30 W mode with classification.

5.1.3. Power-Up

After successful classification (i.e. the PSE has enough available power to satisfy the PD's needs), power is applied to V_{OUT} as long as there is not an overcurrent fault, disconnect, or input undervoltage (UVLO) or overvoltage (OVLO) condition. The status LED is continuously on while power is applied.

The Si3462 implements a two-level overload protection scheme. The output current is limited to ILIM, and, additionally, the output is shut down if the current exceeds I_{CUT} for longer than 60 ms (for further details, refer to “6.4. Power-Up” or to the Si3462data sheet). An overload condition is signaled by a rapidly-flashing status LED.

If power is removed due to an overload condition, detection may automatically restart after a 2.2 s delay, or removing and plugging the Ethernet cable might be necessary depending on the initial configuration (see “6.1. Initialization and Operating Mode Configuration”). The start of a new detection phase is signaled by the LED flashing at a lower rate.

5.1.4. Disconnect (Power Removal)

Removal of a PD can be sensed by determining that the dc current is less than 5 mA for more than 350 ms. If the current then exceeds 10 mA before reaching the timeout for at least 60 ms, the power must not be removed.

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6. Detailed Description of the Si3462 PSE Controller

The Si3462 is a fully IEEE compliant PoE/PoE+ PSE power management controller. The Si3462 is specifically designed and configured to work with an applications circuit (Si3462-EVB) with which it implements a single port PSE solution for either Midspan or Endpoint PoE applications.

Refer to the detailed evaluation board schematics in "9. Si3462-EVB Schematics" on page 17 and "11. Si3462-EVB PCB Layouts" on page 23; the overall functionality is described below. Representative waveforms are shown in "8. Output Voltage and Load Current Waveforms" on page 13.

6.1. Initialization and Operating Mode Configuration

The Si3462 is initialized at powerup or whenever Pin 8 (RST) is held low and then allowed to transition high. Upon reset (RST asserted low), the voltage at the STATUS pin (as determined by the DIP switch and the associated resistor network) is sensed to determine the operating mode of the Si3462. The detection process begins immediately after initialization.

The following operating mode parameters can be set with the DIP switches:

- Endpoint or Midspan mode controls the back off timing per IEEE specifications.
- Restart action on Fault or Overload determines whether the Si3462 automatically restarts after 2 s when a fault or overload condition (e.g., input UVLO, output short-circuit event, classification power level exceeded) is detected or waits to restart until an open-circuit condition is sensed.
- Available power level (and PSE Type specifying the classification method used).

Table 2. Operating Modes[1,2,3,4,5]

DIP Switch Configuration	Status Pin Voltage (V)	Operating Mode					
		PSE Type	Midspan/ Endpoint	Restart Action on Fault or Overload Event Condition	Available Power	Classification BOM[5,6]	Classification Mark BOM[5,7]
	< 0.122	2	Midspan	Restart after disconnection	30 W	No	No
	0.122 to 0.338	1	Midspan	Restart after disconnection	7 W	Yes	No
	0.338 to 0.548	1	Midspan	Restart after disconnection	15.4 W	No	No
	0.548 to 0.756	2	Midspan	Restart after disconnection	30 W	Yes	Yes

Notes:

1. After power-up, the STATUS pin drives the base of an NPN transistor that controls an LED.
2. There is a trade-off in selecting the mode setting resistor values between voltage step accuracy and additional worst-case supply current. For high-value resistors, the base current will alter the voltage steps while low-value resistors may place higher load on the STATUS pin while driving the LED. The suggested resulting parallel resistance used by the Si3462-EVB is 2.0 kΩ.
3. Each mode setting resistor should be connected either to GND or +3.3 V through the DIP switch. Care should be taken not to short the +3.3 V supply to GND.
4. A reset is required after a DIP switch position change for the new mode to take effect.
5. Refer to the Si3462-EVB User Guide to understand the components required to support Classification and Mark.
6. Classification components are R14,R15,R16C8, D5, Q6, and Q17.
7. Classification mark components are Q2, R24, and R25.

Table 2. Operating Modes[1,2,3,4,5] (Continued)

DIP Switch Configuration	Status Pin Voltage (V)	Operating Mode					
		PSE Type	Midspan/ Endpoint	Restart Action on Fault or Overload Event Condition	Available Power	Classification BOM[5,6]	Classification Mark BOM[5,7]
	0.756 to 0.961	2	Midspan	Auto restart after 2 s	30 W	No	No
	0.961 to 1.162	1	Midspan	Auto restart after 2 s	7 W	Yes	No
	1.162 to 1.366	1	Midspan	Auto restart after 2 s	15.4 W	No	No
	1.366 to 1.575	2	Midspan	Auto restart after 2 s	30 W	Yes	Yes
	1.575 to 1.784	2	Endpoint	Restart after disconnection	30 W	No	No
	1.784 to 1.990	1	Endpoint	Restart after disconnection	7 W	Yes	No
	1.990 to 2.196	1	Endpoint	Restart after disconnection	15.4 W	No	No
	2.196 to 2.407	2	Endpoint	Restart after disconnection	30 W	Yes	Yes
	2.407 to 2.618	2	Endpoint	Auto restart after 2 s	30 W	No	No
	2.618 to 2.838	1	Endpoint	Auto restart after 2 s	7 W	Yes	No
	2.838 to 3.044	1	Endpoint	Auto restart after 2 s	15.4 W	No	No
	>3.044	2	Endpoint	Auto restart after 2 s	30 W	Yes	Yes

Notes:

1. After power-up, the STATUS pin drives the base of an NPN transistor that controls an LED.
2. There is a trade-off in selecting the mode setting resistor values between voltage step accuracy and additional worst-case supply current. For high-value resistors, the base current will alter the voltage steps while low-value resistors may place higher load on the STATUS pin while driving the LED. The suggested resulting parallel resistance used by the Si3462-EVB is 2.0 kΩ.
3. Each mode setting resistor should be connected either to GND or +3.3 V through the DIP switch. Care should be taken not to short the +3.3 V supply to GND.
4. A reset is required after a DIP switch position change for the new mode to take effect.
5. Refer to the Si3462-EVB User Guide to understand the components required to support Classification and Mark.
6. Classification components are R14,R15,R16C8, D5, Q6, and Q17.
7. Classification mark components are Q2, R24, and R25.

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After power-up, the STATUS pin of the Si3462 is in a high-impedance state and is used for measuring the voltage set by the DIP switch and the associated resistor network. Then, during normal operation, this pin drives the status LED via transistor Q3.

The mode setting voltage steps are provided by a simple 4-bit DAC. Each mode setting resistor should be connected either to GND or +3.3 V for proper operation. Take care not to short the +3.3 V supply to GND, and remember to activate the reset button for the new configuration to take effect.

The voltage thresholds found in Table 2 on page 7 take into account the slight loading effect of Q3's base current; therefore, it is recommended to use the same source resistance (around 2.0 kΩ) as that of the Si3462-EVB network when providing the status pin voltage from a different voltage source, such as a simple voltage divider or a DAC. Different resistor values may be used in the mode setting network, but the trade-off between voltage step accuracy and the additional worst-case supply current should be considered. For high value resistors, the base current will alter the voltage steps, while low value resistors may place higher loads on the STATUS pin when driving the LED.

6.2. Detection

The detection process consists of sensing a nominal 25 kΩ signature resistance in parallel with up to 0.15 µF of capacitance. The signature resistance measurement has to be carried out in the 2.8 to 10 V output voltage range with a 5 mA current limit.

To eliminate the possibility of false detection events, the Si3462-EVB reference design performs a robust 3-point detection sequence by varying the voltage across the load and sensing the load current changes. This minimizes effects, such as those caused by the diode bridges present in powered devices (PDs).

At the beginning of the detection sequence, V_{OUT} is at zero; then, it is varied from 4 to 8 V and back to 4 V for 20+20+50 ms at each respective level. If the PD's signature resistance is in the RGOOD range of 17 to 29 kΩ, the Si3462 proceeds to classification and powerup. If the PD resistance is not in this range, the detection sequence repeats continuously.

Detection is sequenced approximately every 360 ms until RGOOD is sensed, indicating a valid PD has been detected. The STATUS LED (D2) is flashed at an approximate rate of 1.5 Hz to indicate that the PSE is searching for a valid PD.

6.3. Classification

To save bill of materials cost, the Si3462 does not perform classification when configured for 15.4 W of output power. There is also a pin-programmable mode for no classification and 30 W of output power to support non-standard PDs. If no classification is done, the classification components of the bill of materials do not need to be populated. The classification mark components only need to be populated for 30 W mode with classification.

The Si3462 implements both the one-event and two-event physical layer classification methods. For one-event classification, the pass FET Q4 is turned on and programmed for an output voltage of 18 V with a current limit of 75 mA for 30 ms. For the two-event classification, the 18 V pulse is output twice with an 8.5 V amplitude mark pulse for 10 ms between the two classification pulses.

If the class level of the PD is not within the supported level as set by the initial voltage on the Si3462's STATUS pin (refer to the Operating Mode Configuration section above), an error is declared, and the LED blinks rapidly at a rate of 10 Hz for two seconds before the Si3462 goes back to the detection cycle. This is referred to as classification-based power denial. If the class level is in the supported range, the Si3462 proceeds to powerup. This is referred to as classification-based power granting. Classification level is determined according to the current measured at the ISENSE input as shown in Table 3.

Table 3. Classification Levels

ISENSE Current (Nominal)	Classification Level	PSE Type	Minimum Power Level	Overload Current Threshold I_{CUT} (Typ) [mA]*	Overload Current Limit I_{LIM} (Typ) [mA]
< 6.5 mA	Class 0	1	15.4 W	16,500/Vout	425
14.5 mA to 23 mA	Class 2	1	7 W	7,500/Vout	425
23 mA to 33 mA	Class 3	1	15.4 W	16,500/Vout	425
33 mA to 48 mA	Class 4	2	26.4 W	33,200/Vout	885
***Note:** The I_{CUT} overload thresholds are dynamically calculated as a function of the granted power and the effective output voltage.					

6.4. Power-Up

After successful classification, the pass FET is turned on with a current limit corresponding to the classification results as indicated in Table 3. After powerup, power is applied to V_{OUT} as long as there is no overcurrent fault, disconnect, or input under-voltage (UVLO) or over-voltage condition. The STATUS LED is continuously lit when power is applied.

If the output power exceeds the level of the power requested during classification, the Si3462 will declare an error and shut down the port, flashing the LED rapidly to indicate the error (for either two seconds or until an open-circuit condition is detected as determined by the initial voltage on the STATUS pin).

The Si3462-EVB implements two levels of overload protection:

- The output current is limited to the ILIM value corresponding to the classification level detected (refer to Table 3). During the powerup transient, phase output current is limited to 425 mA, independent of the classification level.
- If the output current exceeds I_{CUT} for longer than 60 ms, the output is shut down (refer to Table 3 for the I_{CUT} values). Additionally, for Class 4 devices, if current limitation persists longer than 15 ms, power will also be shut down to protect the pass FET.

If the Si3462 was configured to operate in the automatic retry mode, it will retry detection and power up after an overload. In this case, the status LED will flash rapidly for two seconds to show the error condition, and then the Si3462 will automatically initiate a new detection cycle while the status LED flashes at a rate of 1.5 Hz.

Alternatively, the Si3462 can be programmed to signal that an error condition has occurred, in which case the user must disconnect the Ethernet cable and plug it in again (or push the reset switch on the Si3462-EVB) to start a new detection and powerup cycle. In this case, the status LED flashes rapidly until an open-circuit is detected and then flashes at a rate of 1.5 Hz to show that a new detection cycle is in progress. Power is provided again only after successful detection and classification. The Si3462-EVB does not regulate the output voltage during the power-on state. Input voltage changes will be transmitted to the output directly.

6.5. Disconnect (Power Removal)

The Si3462 supports a robust disconnect algorithm. If the output current drops below 7.5 mA, a timer is started to count towards a time-out of 350 ms. If the output current again exceeds the 7.5 mA threshold, the timer is decremented at 10 times the increment rate towards zero. Power is removed from the output if the timer reaches the 350 ms limit, but the Si3462 will continue to provide power if the output current is above the 7.5 mA limit for at least a fraction of the 350 ms timeout (unless an overload condition is sensed). The only other way to force the Si3462 to disconnect power is by doing a reset.

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6.6. Current Limit Control

The Si3462's overcurrent trip point, I_{CUT}, is determined by the output power set during the classification stage power granting process and the actual output voltage. If the output current exceeds the threshold, a timer counts up towards a timeout of 60 ms. If the current drops below the set threshold, the timer counts down towards zero at 1/16th the rate. If the timer reaches the set timeout, an overcurrent fault is declared, and the channel is shut down by turning off the pass FET. Additionally, for Class 4 devices, if the output current reaches the ILIM level, the output is shut down after 15 ms to protect the pass FET. After an overcurrent fault event, the LED will flash rapidly. As set by the initial voltage on the STATUS pin at powerup, the Si3462 then automatically resumes the detection process for “automatic restart configuration” unless the Si3462 is configured in a “restart after a disconnect condition” mode.

For the automatic restart configuration, the LED will flash rapidly after an overcurrent event for 2.2 seconds, and a new detection cycle will be initiated. The LED will then flash at a 1.5 Hz rate to show that the detection is in progress.

In the restart on disconnect configuration, the LED will flash rapidly until an open-circuit condition is detected before a new detection cycle will start. Normally, an open-circuit condition can be created by removing the Ethernet cable from the Si3462-EVB's RJ-45 jack labelled “PoE”. Power will not be provided until an open-circuit condition is detected. Once the Si3462-EVB detects an open-circuit condition, the detection process begins. The status LED blinks at a rate of 1.5 Hz, and the Si3462 is then allowed to go into classification and powerup mode if a valid PD signature resistance is detected.

6.7. UVLO/OVLO

The Si3462-EVB reference design is optimized for 50 V nominal input voltages (44 V minimum to 57 V maximum). If the input voltage drops below 42 V, a UVLO condition is declared, or, if it exceeds 60 V, an over-voltage condition is declared, and the output is shut down in both cases. An undervoltage or an overvoltage event is a fault condition reported through the status LED as a rapid blinking of 10 flashes per second. The UVLO and OVLO conditions are continuously monitored in all operating states.

6.8. Status LED Function

During the normal detection sequence, the STATUS LED flashes approximately 1.5 times per second as the detection process continues. After successful powerup, the LED glows continuously. If there is an error condition (i.e., class level is beyond the programmed value or a fault or overcurrent condition has been detected), the LED flashes rapidly at 10 times per second. This occurs for two seconds for normal error delay, and the detection process automatically starts again after 2.2 s unless a “restart after disconnect condition” was set during the initial configuration. Power will not be provided until an open-circuit condition is detected. Once the Si3462-EVB detects an open-circuit condition, the LED blinks at 1.5 times per second.

If the PD is disconnected so that a disconnect event occurs, the LED starts flashing at 1.5 times per second once the detect process resumes.

7. Design and Layout Considerations

7.1. General Recommendations

The Si3462-EVB schematic and layout are intended to be used as a reference for all customer designs. The Si3462-EVB has been tested by the University of New Hampshire Interoperability Lab (UNH IoL) to comply with the relevant IEEE 802.3 Clause 33 specifications. UNH test reports can be downloaded from http://www.silabs.com/PoE. Since the Si3462's performance in an application depends on external components and PCB layout, customers are ultimately responsible for validating their design's conformance to all relevant industry, safety, and customer-specific requirements. For applications support, visit the Silicon Labs Technical Support web page: https://www.silabs.com/support/pages/contacttechnicalsupport.aspx.

7.2. Isolation

The IEEE 802.3 specification requires that the PSE output power be isolated from earth ground*. To accomplish this, the input power source must be isolated from earth ground. Also, do not connect the Si3462's ground connection (Pin #11) to earth ground because this pin serves only as a circuit reference point in the Si3462-EVB.

***Note:** If the input power supply is referenced to earth ground and if one of the output pads is connected to ground, it can create a high-current fault condition that will not be protected.

7.3. SELV-Compliant Output Voltage

Since the output of the Si3462-EVB reference design is designed to be less than 57 Vdc under all conditions, it is considered an SELV circuit.

7.4. Surge Protection

The Si3462-EVB applications design includes a clamp diode, D6, to protect against 50 µs intra-building lightning surges as specified in IEEE 802.3. Additional protection, such as a 1 A fuse in the output circuit, may be required for applications in which the Ethernet cabling is not intra-building.

7.5. Thermal Considerations

The pass FET needs a cooling surface of adequate size. The Si3462 controller itself implements over-temperature protection, but this alone cannot effectively protect the pass FET in case of a sudden overload. Nevertheless, relatively tight thermal coupling between the two devices may be a good idea.

Some of the resistors, such as the current sensor and the series resistors of the shunt regulator (if used), also dissipate relatively large amounts of power. Care should be taken to select resistors with proper power ratings. Using a high-efficiency external 3.3 V supply instead of the onboard shunt regulator can save almost 1 W of power.

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8. Output Voltage and Load Current Waveforms

Figures 6 through 13 show the output voltage and load current waveforms during startup and fault conditions. Refer also to the Si3462-EVB schematics in Figures 14 through 16.

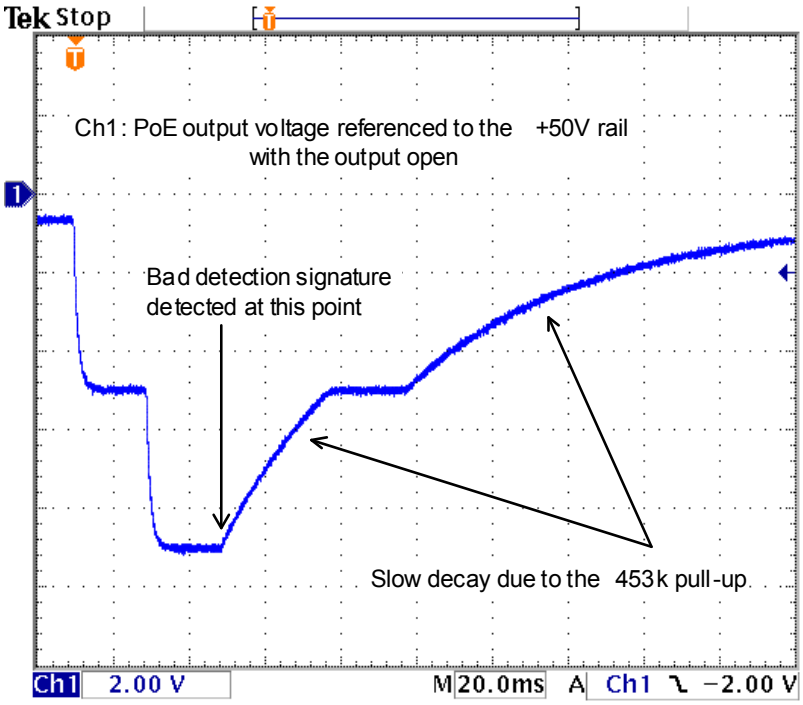

Figure 6. Detection Pulse into Open-Circuit

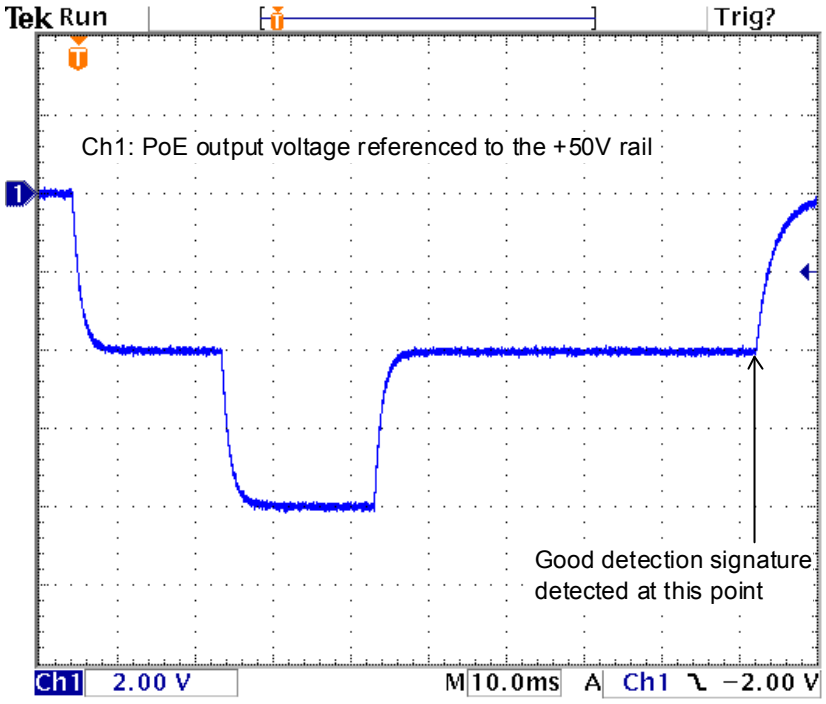

Figure 7. Successful Detection

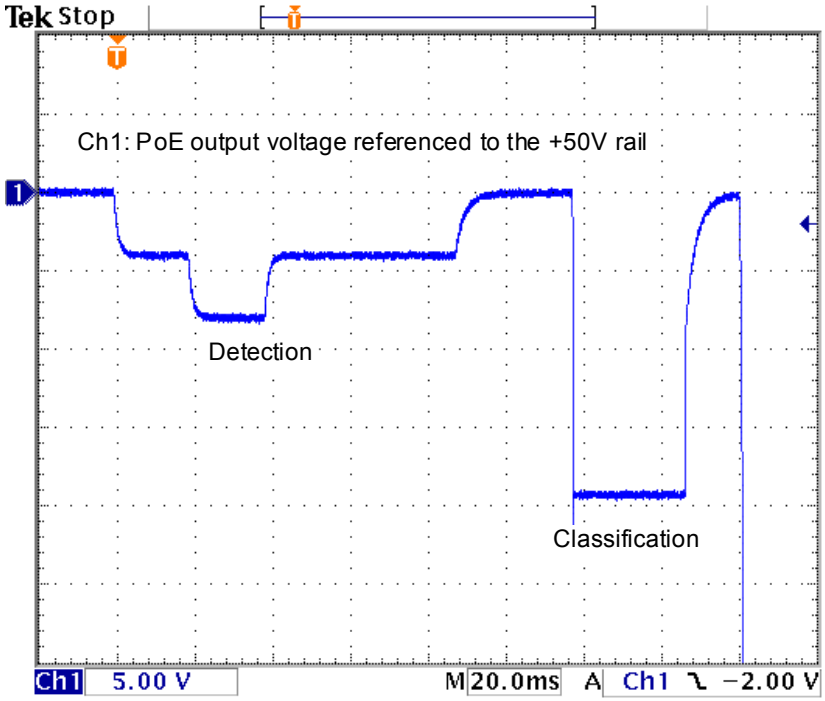

Figure 8. Detection and Classification Pulse for a Type-1 Device

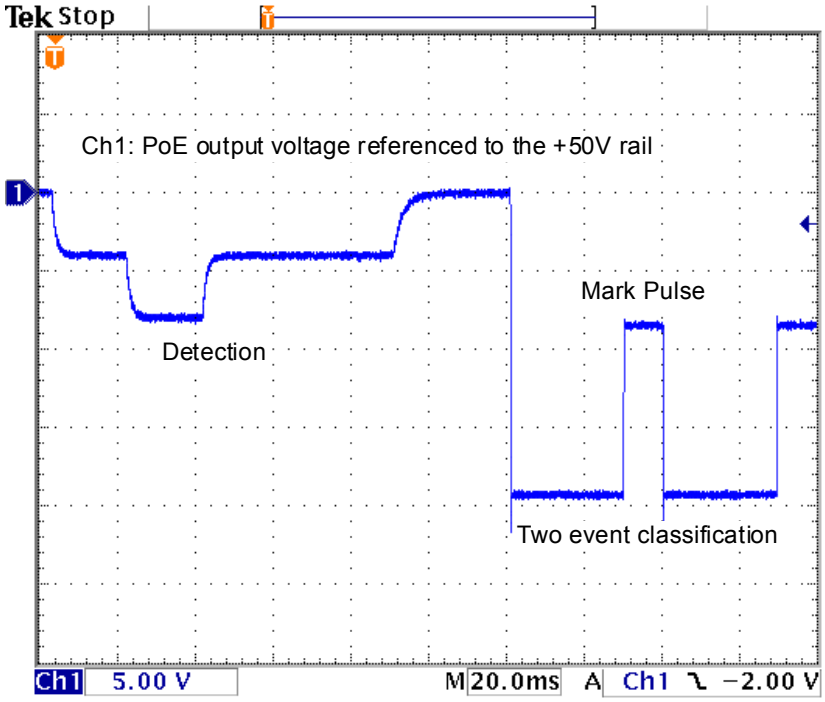

Figure 9. Detection and Classification Pulse for a Type-2 Device

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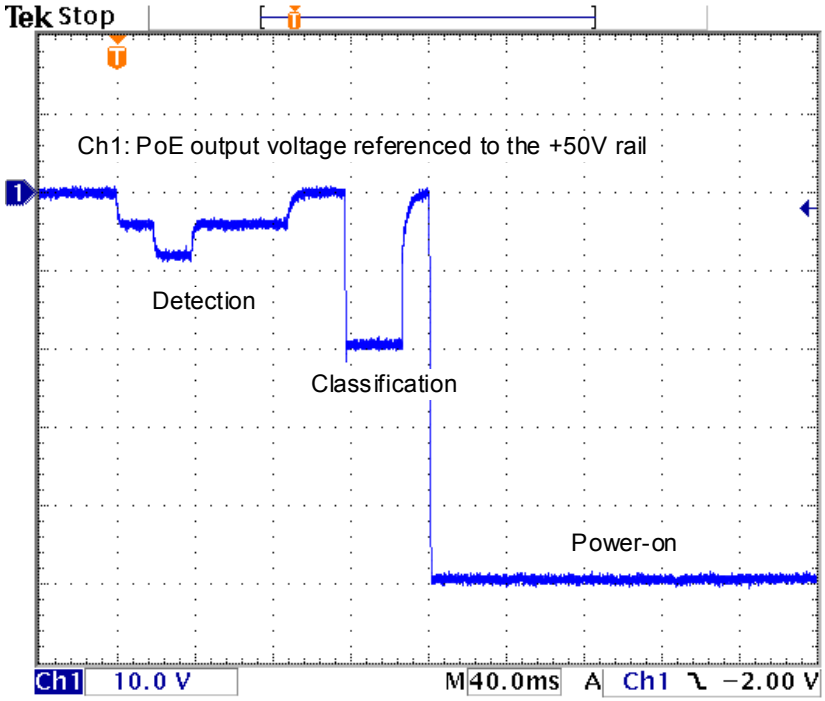

Figure 10. Detection, Classification, and Powerup for a Type-1 Device

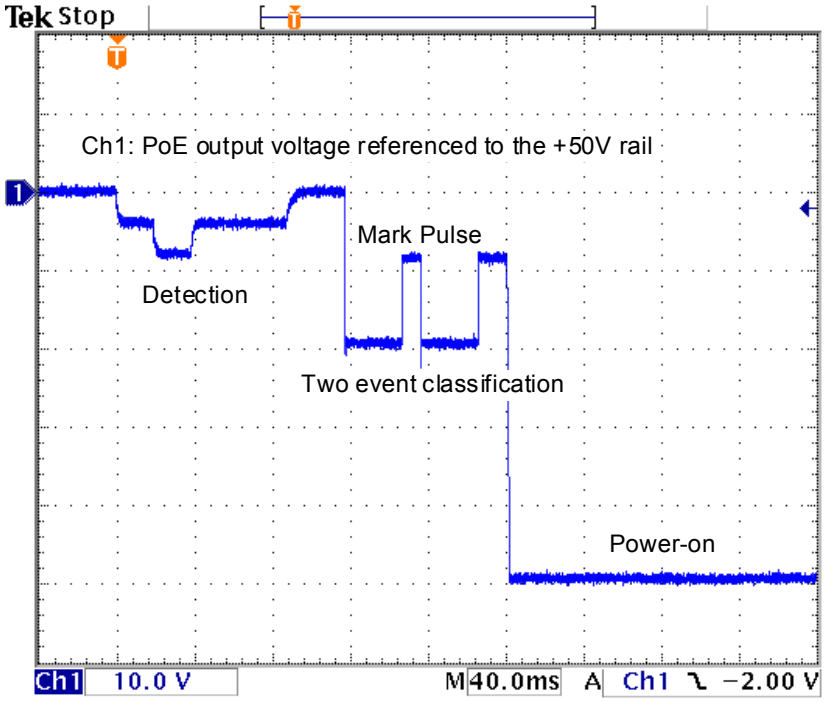

Figure 11. Detection, Classification, and Power-up for a Type-2 Device

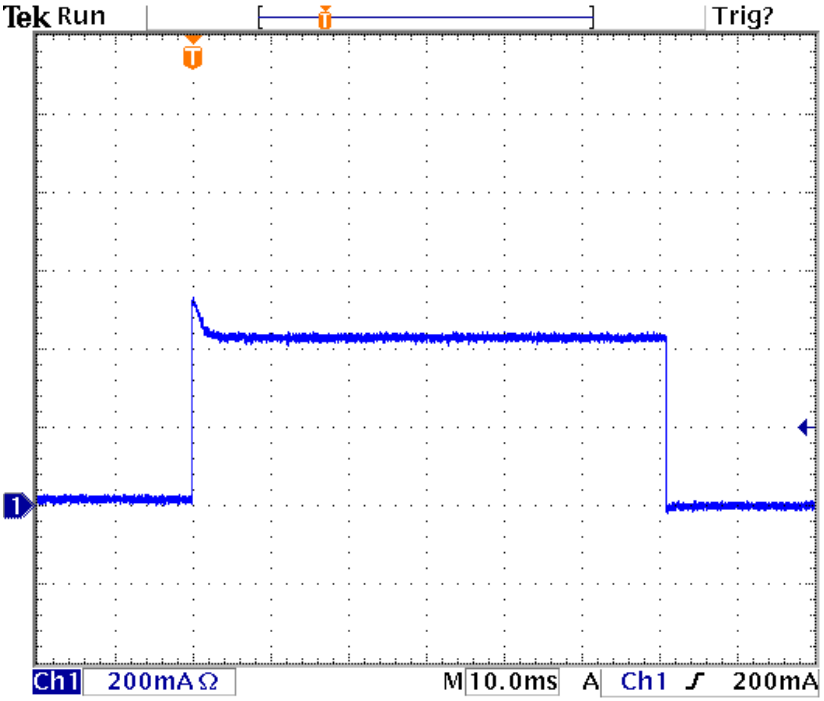

Figure 12. Overcurrent Disconnect Delay Time of 60 ms

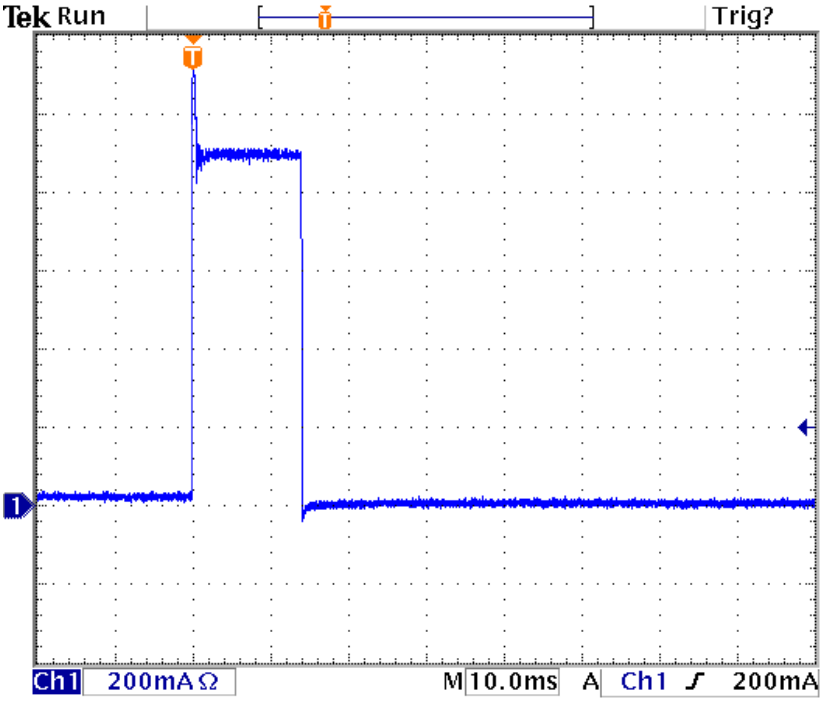

Figure 13. Overcurrent Disconnect Delay Time of 15 ms

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9. Si3462-EVB Schematics

Full schematics are provided in the following figures. To ensure you are using the latest schematic database revisions, you may download the zip file from the Silicon Laboratories Si3462 documentation page: http://www.silabs.com/products/power/poe/Pages/PowerSourcingEquipment.aspx

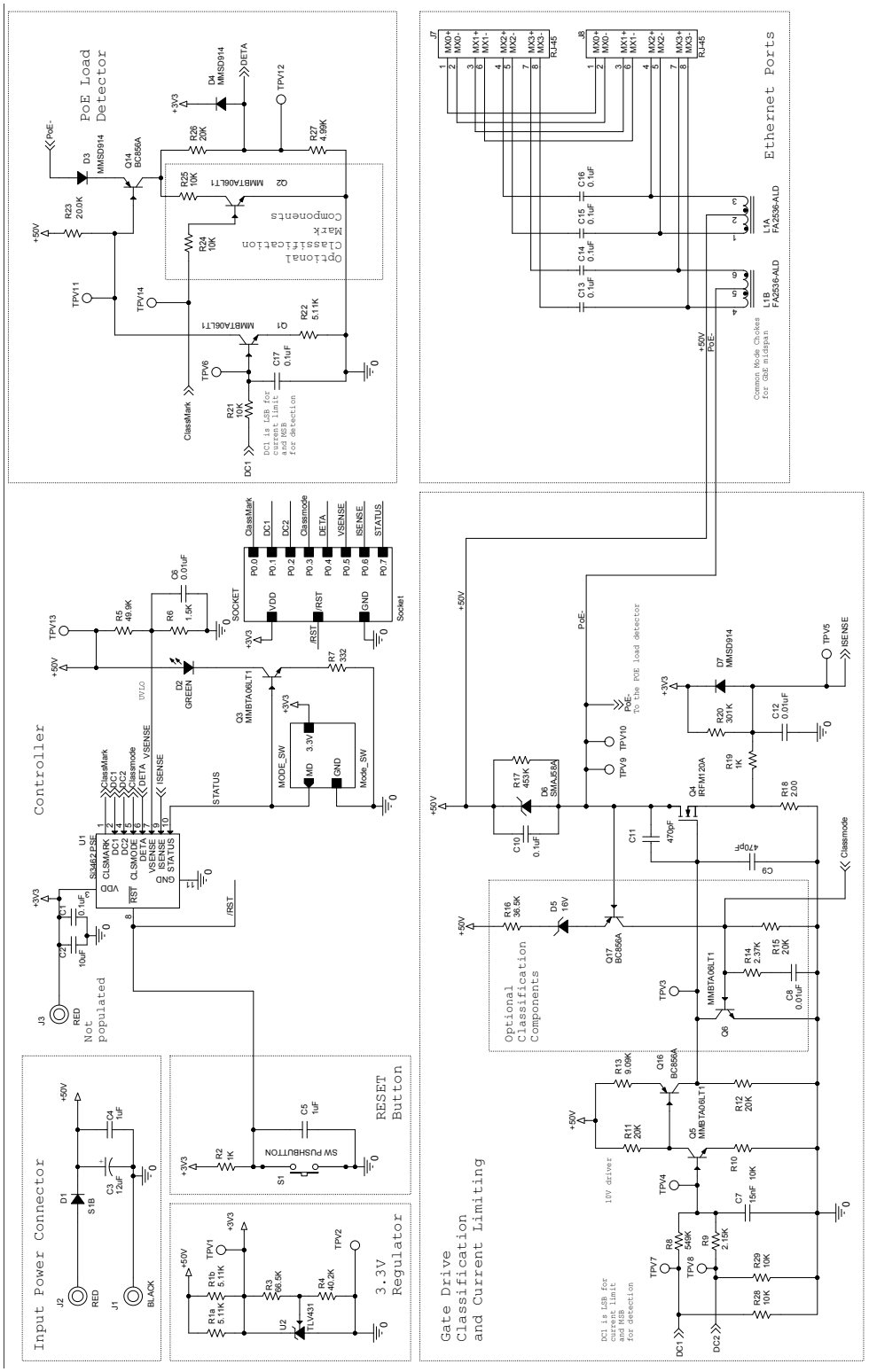

Figure 14. Si3462-EVB Schematic (1 of 3)

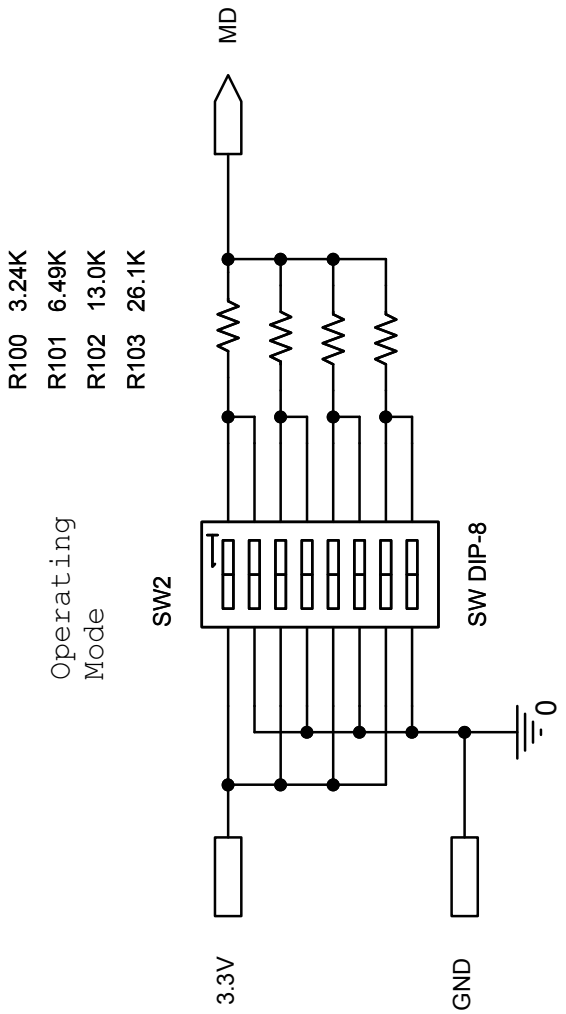

Figure 15. Si3462-EVB Schematic (2 of 3)

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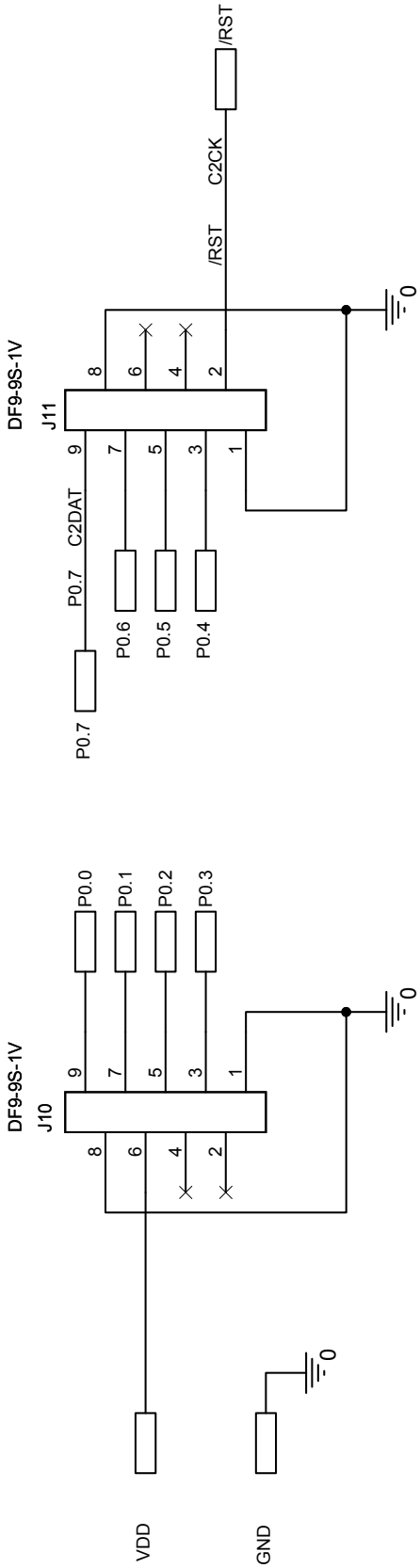

Figure 16. Si3462-EVB Schematic (3 of 3)

10. Si3462-EVB Bill of Materials

Table 4. Si3462-EVB Bill of Materials

Qty	Ref	Value	Rating	Tol	PCB Footprint	Mfr Part Number	Mfr
PoE BOM (Including Optional LED)							
2	C1, C10	0.1 µF		10 V	C0603	C0603X7R101-104K	Venkel
1	C2	10 µF		6.3 V	C0603	C0603X5R6R3-106M	Venkel
1	C5	1 µF		10 V	C0603	C0603X7R100-105K	Venkel
2	C6, C12	0.01 µF		100 V	C0603	C0603X7R101-103K	Venkel
1	C7	15 nF		16 V	C0603	C0603X7R160-153K	Venkel
2	C9, C11	470 pF		25 V	C0603	C0603X7R101-471K	Venkel
1	C17	0.1 µF		10 V	C0603	C0603X7R100-104K	Venkel
1	D2	GREEN	25 mA		LED-RT	551-0207	Dialight
3	D3, D4, D7	MMSD914	0.2 A		SOD-123	MMSD914	Fairchild
1	D6	SMAJ58A	400 W		DO-214AC	SMAJ58A	Littelfuse
4	Q1, Q2, Q3, Q5	MMBTA06LT1	500 mA		SOT23-BEC	MMBTA06LT1	On Semi
1	Q4	IRFM120A	2.3 A		SOT223-GDS	IRFM120A or FDT3612	Fairchild
2	Q14, Q16	BC856A	100 mA		SOT23-BEC	BC856A	Diodes Inc.
1	R19	1 kΩ	1/16 W	±1%	R0603	CR0603-10W-1001F	Venkel
1	R5	49.9 kΩ	1/8 W	±1%	R0805	CR0805-8W-4992F	Venkel
1	R6	1.5 kΩ	1/10 W	±1%	R0603	CR0603-10W-1501F	Venkel
1	R7	332 Ω	1/16 W	±1%	R0603	CR0603-10W-3320F	Venkel
1	R8	549 kΩ	1/16 W	±1%	R0603	CR0603-10W-5493F	Venkel
1	R9	2.15 kΩ	1/16 W	±1%	R0603	CR0603-10W-2151F	Venkel
3	R10, R21	10 kΩ	1/16 W	±1%	R0603	CR0603-10W-1002F	Venkel
4	R11, R12, R15, R26	20 kΩ	1/16 W	±1%	R0603	CR0603-10W-2002F	Venkel
1	R13	9.09 kΩ	1/16 W	±1%	R0603	CR0603-16W-9091F	Venkel
1	R17	453 kΩ	1/10 W	±1%	R0805	CR0805-10W-4533F	Venkel
1	R18	2 Ω	2 W	±1%	R2512	CR2512-2W-2R00F	Venkel
1	R20	301 kΩ	1/16 W	±1%	R0603	CR0603-10W-3013F	Venkel
1	R22	5.11 kΩ	1/16 W	±1%	R0603	CR0603-10W-5111F	Venkel

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Table 4. Si3462-EVB Bill of Materials (Continued)

Qty	Ref	Value	Rating	Tol	PCB Footprint	Mfr Part Number	Mfr
1	R23	20 kΩ	1/16 W	±1%	R0603	CR0603-16W-2002F	Venkel
1	R27	4.99 kΩ	1/16 W	±1%	R0603	CR0603-16W-4991F	Venkel
3	R28, R29, R100	10 kΩ	1/16 W	±1%	R0603	CR0603-16W-1002F	Venkel
1	R100	3.24 kΩ	1/16 W	±1%	R0603	CR0603-16W-3241F	Venkel
1	U1	Si3462 PSE			QFN10N3X3P0.5	Si3462XYY-GM	SiLabs
Basic BOM							
Optional Classification BOM							
1	R14	2.37 kΩ	1/16 W	±1%	R0603	CR0603-10W-2371F	Venkel
1	R15	20 kΩ	1/16 W	±1%	R0603	CR0603-10W-2002F	Venkel
1	R16	36.5 kΩ	1/10 W	±1%	R0805	CR0805-10W-3652F	Venkel
1	Q6	MMBTA06LT1	500 mA		SOT23-BEC	MMBTA06LT1	On Semi
1	Q17	BC856A	100 mA		SOT23-BEC	BC856A	Diodes Inc.
1	D5	16 V	500 mW	5%	SOD-123	MMSZ5246BT1G	On Semi
1	C8	0.01 µF		100 V	C0603	C0603X7R101-103K	Venkel
Optional Classification Mark BOM							
2	R24, R25	10 kΩ	1/16 W	±1%	R0603	CR0603-10W-1002F	Venkel
1	Q2	MMBTA06LT1	500 mA		SOT23-BEC	MMBTA06LT1	On Semi
System Dependent BOM							
Mode Selector							
1	SW2	SW DIP-8	0.025 A		SW8-DIP-SMT	TDA08H0SK1	CTS
1	R101	6.49 kΩ	1/16 W	±1%	R0603	CR0603-16W-6491F	Venkel
1	R102	13 kΩ	1/10 W	±1%	R0603	CR0603-10W-1302F	Venkel
1	R103	26.1 kΩ	1/16 W	±1%	R0603	CR0603-16W-2612F	Venkel
Reset							
1	R2	1 kΩ	1/10 W	±1%	R0603	CR0603-10W-1001F	Venkel
1	S1	SW Pushbutton	50 mA		SW-PB-MOM	101-0161-EV	Mountain Switch

Table 4. Si3462-EVB Bill of Materials (Continued)

Qty	Ref	Value	Rating	Tol	PCB Footprint	Mfr Part Number	Mfr
PoE Coupling Circuit for Midspan							
4	C13, C14, C15, C16	0.1 µF		±10%	C1210	C1210X7R251-104K	Venkel
1	L1	FA2536-ALD	675 µH		IND-FA2536	FA2536-ALD	COILCRAFT
Connectors							
1	J1	Black	15 A		BINDING-POST	111-0703-001	Johnson/Emerson
2	J2, J3	Red	15 A		BINDING-POST	111-0702-001	Johnson/Emerson
2	J7, J8	RJ-45			RJ-45	95001-2881	MOLEX
2	J10, J11	DF9-9S-1V	0.1 A		CONN-DF9-9S-1V	DF9-9S-1V	Hirose Electric Co. Ltd.
Power Input Filter							
1	D1	S1B	1.0 A		DO-214AC	S1B	Fairchild
1	C3	12 µF		±20%	C2.5X6.3MM-RAD	EEUFC2A120	Panasonic
1	C4	1 µF		±10%	C1210	C1210X7R101-105K	Venkel
3.3 V Supply							
2	R1b, R1a	5.11 kΩ	2 W	±1%	R2512	CR2512-2W-5111F	Venkel
1	U2	TLV431			TLV431-DBZ	TLV431BCDBZR	TI
1	R3	66.5 kΩ	1/10 W	±1%	R0603	CR0603-10W-6652F	Venkel
1	R4	40.2 kΩ	1/10 W	±1%	R0603	CR0603-10W-4022F	Venkel

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11. Si3462-EVB PCB Layouts

Full PCB layouts are provided in the following figures. To ensure you are using the latest layout database revisions, you may download the zip file from the Silicon Laboratories Si3462 documentation page: http://www.silabs.com/products/power/poe/Pages/PowerSourcingEquipment.aspx

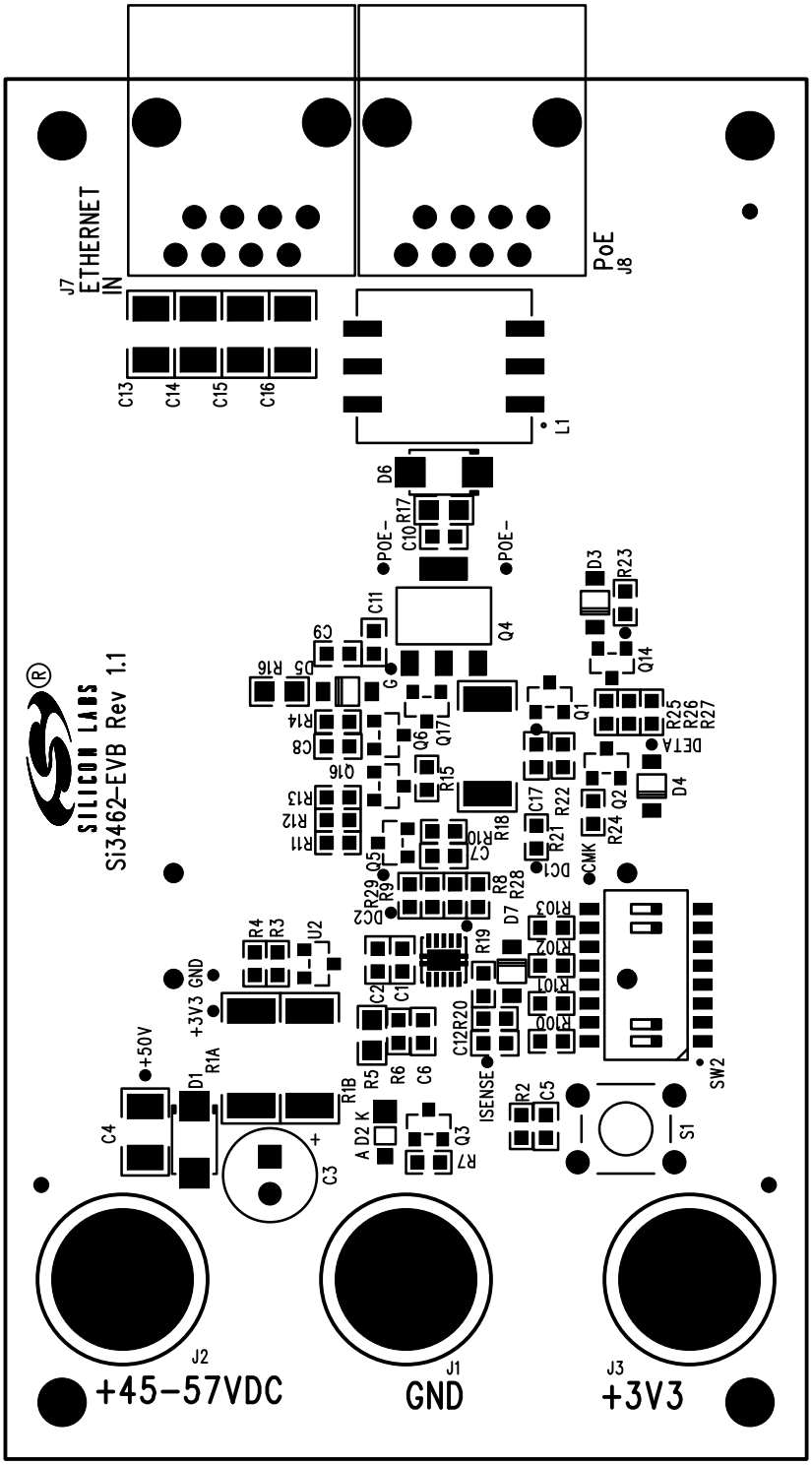

Figure 17. Si3462-EVB Top-Side Component Placement

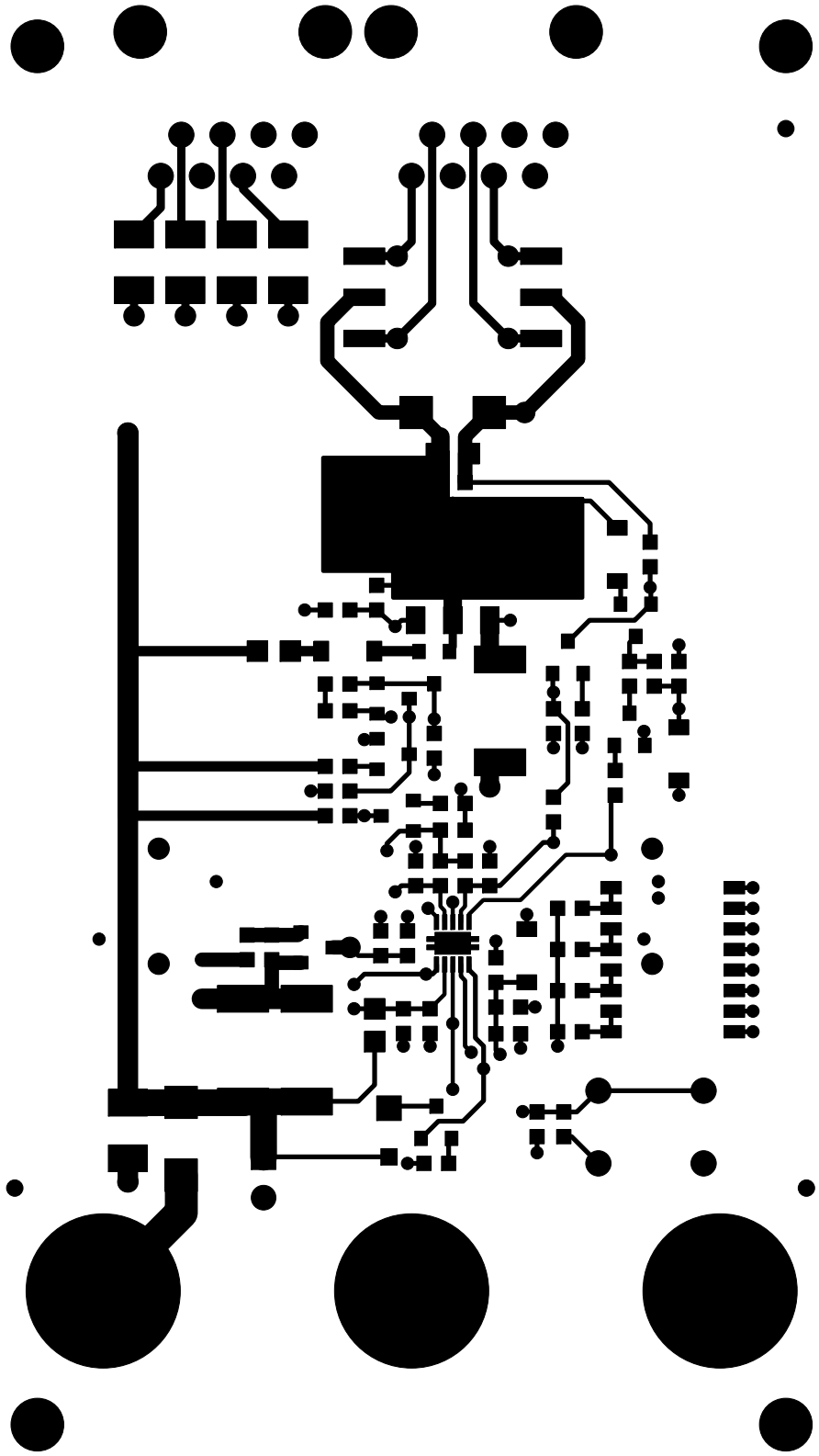

Figure 18. Si3462-EVB Top-Side Interconnect

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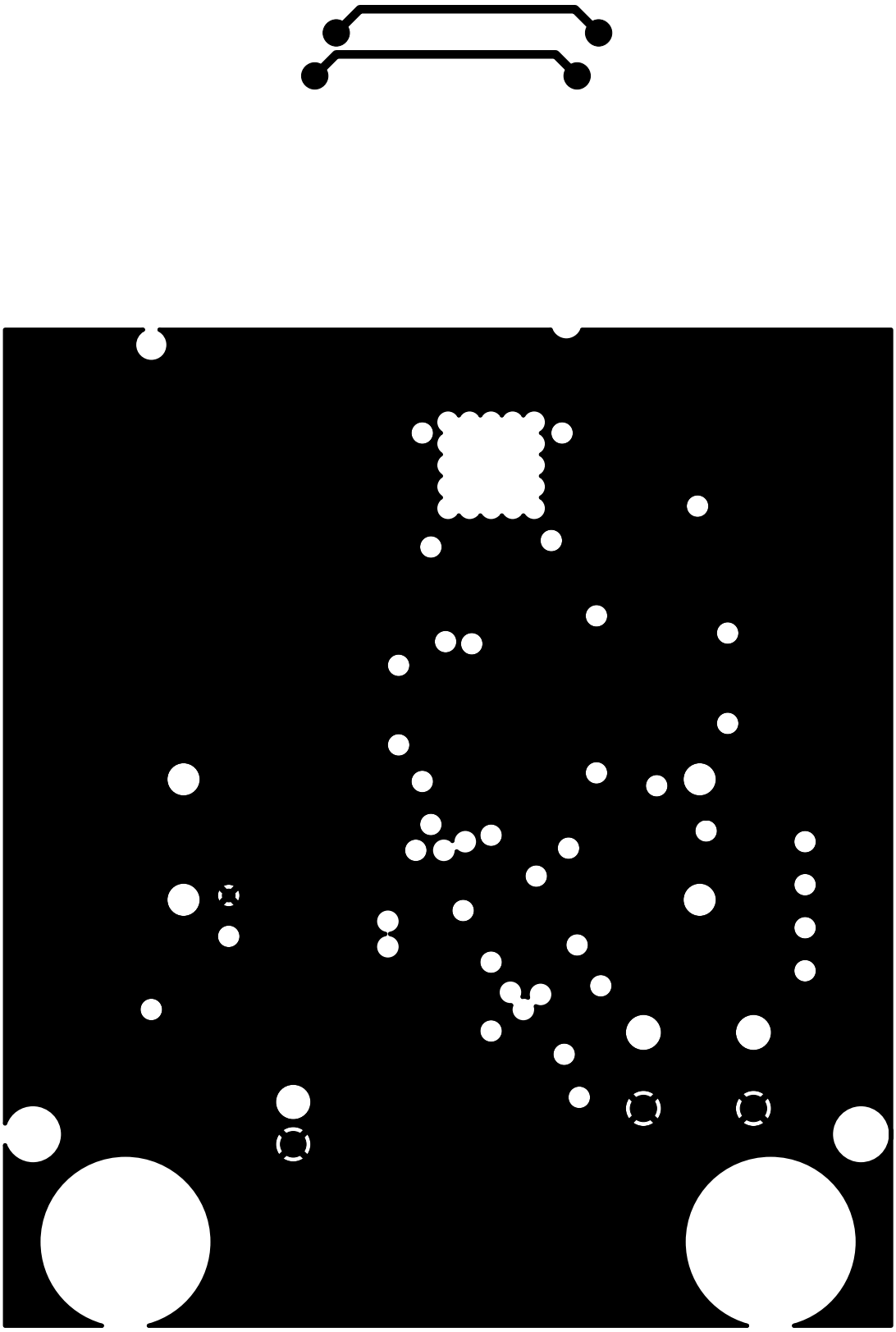

Figure 19. Si3462-EVB Ground Plane

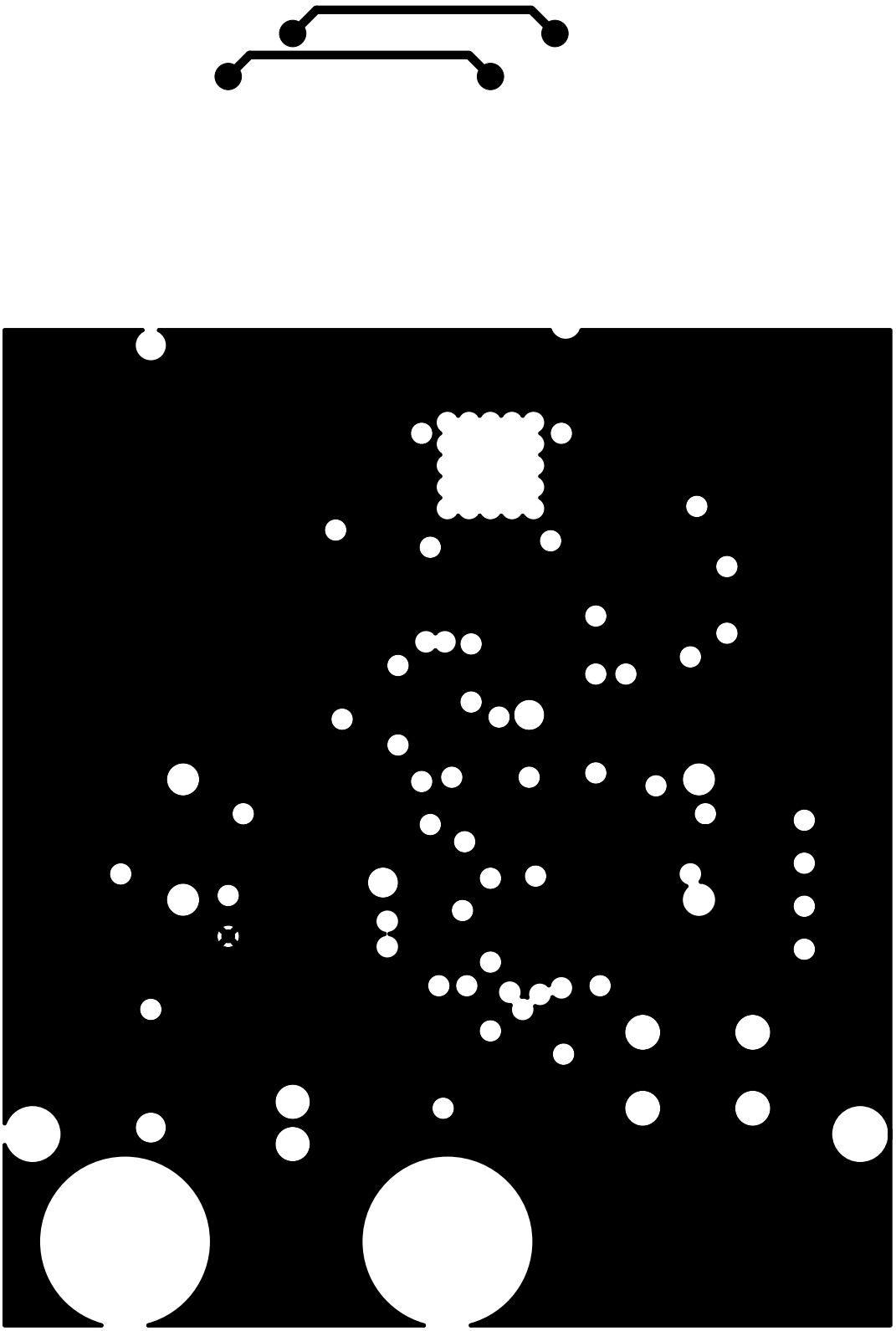

Figure 20. Si3462-EVB Power Plane

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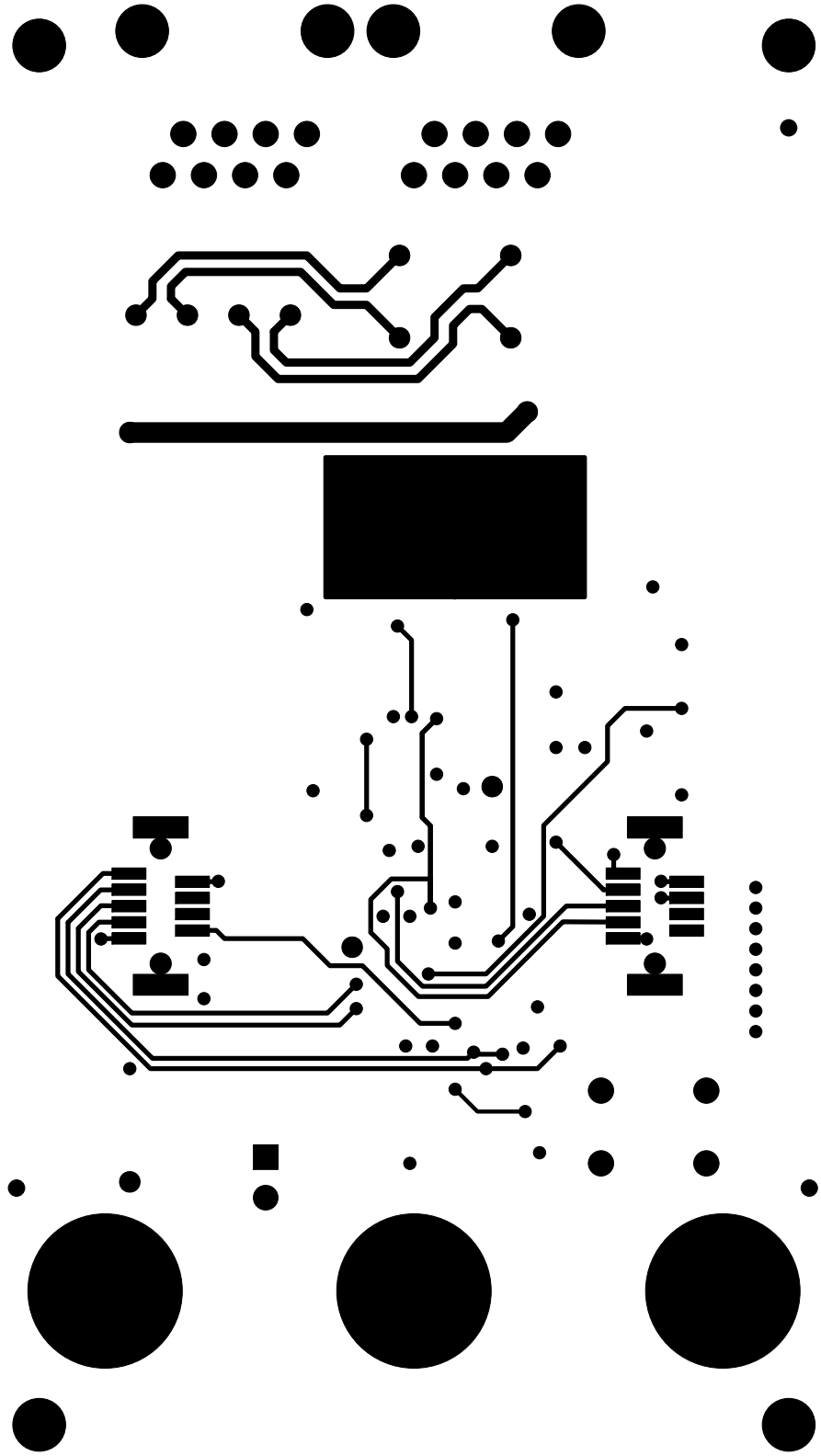

Figure 21. Si3462-EVB Bottom-Side Interconnect

12. BOM Component Considerations

To achieve optimal performance and full-specification compliance, Silicon Labs strongly encourages the use of the components and vendor part numbers listed in “10. Si3462-EVB Bill of Materials”. If alternate components must be substituted, note the following recommendations for components in the power section.

- Diode D6 must not clamp at 57 V and must clamp to <100 V under worst-case surge conditions.
- Heat dissipating components must be separated from each other and moved away from components that are heat-sensitive.

Other component considerations:

- Headers J10 and J11 are used for development purposes only. The Si3462 is not user-programmable, and it is not recommended that these components be included in actual layouts.
- The operating mode setting DIP switch and its associated resistors are probably not needed in a custom design. Replace them with a suitable voltage divider consisting of two resistors (preferably with a resulting 2.0 kΩ parallel resistance).
- Diode D1 protects the circuit from accidental polarity reversal. It may not be needed.
- The reset push button and its associated components (R2 and C5) are optional. If not needed, tie the /RST input high.
- A much higher-efficiency external supply may be substituted for the 3.3 V shunt regulator.

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13. Operating the Si3462-EVB

The Si3462-EVB itself is very simple to use. Only a 50 V dc power source is needed for connection to J2. A power rating of at least 35 W is recommended when the high-power PoE+ mode is used.

The Si3462 will automatically power up, detect the operational modes (midspan/endpoint, classification power level, and restart mode), and begin the detection process, during which the LED flashes at 1.5 times per second.

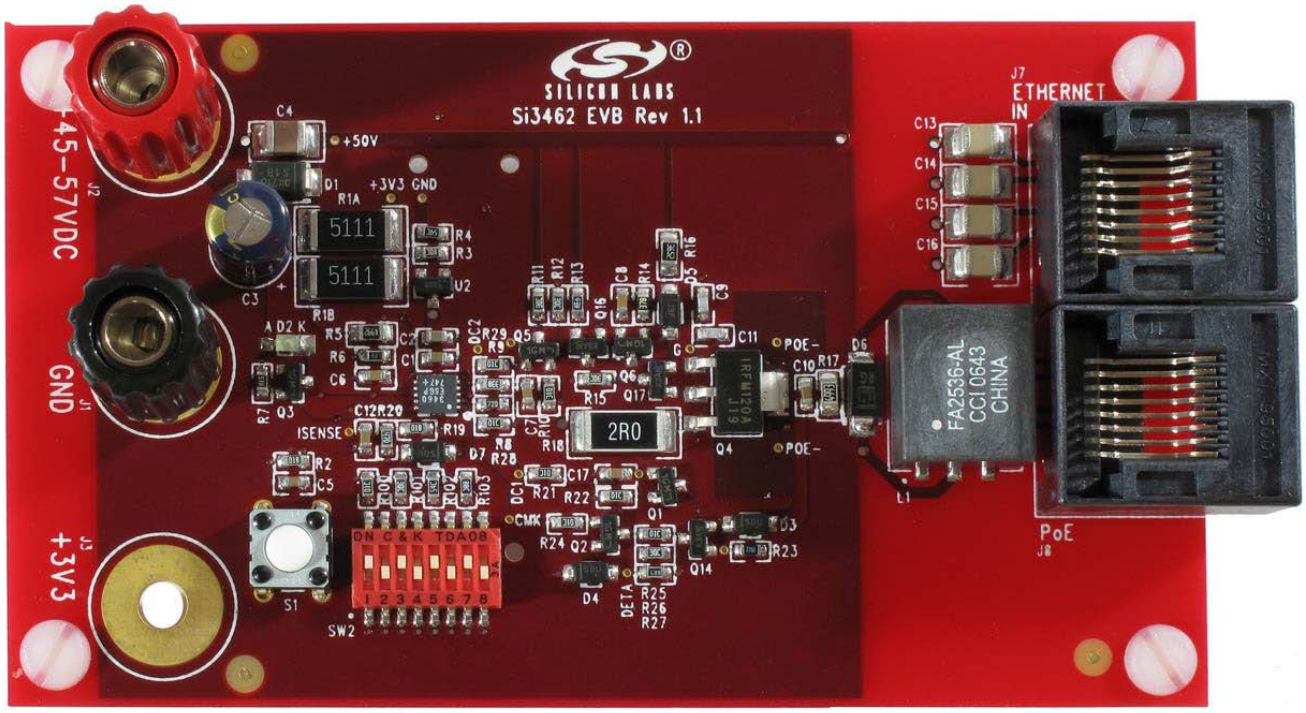

Figure 22. Si3462-EVB

To test the Si3462-EVB in a PoE environment, many commercial PDs are available, such as Wireless Access Points (WAPs), Voice over IP phones (VoIP), and IP-based security cameras. Any of these can be connected to the Si3462-EVB to receive PSE power while exchanging Ethernet traffic. One example of a POE+ PD is an 802.11n (multi-radio) wireless access point.

To test the Si3462-EVB in a PoE environment, many commercial PDs are available, such as Wireless Access Points (WAPs), Voice over IP phones (VoIP), and IP-based security cameras. Any of these can be connected to the Si3462-EVB to receive PSE power while exchanging Ethernet traffic.

Another PD option is to use the Si3462-EVB with one of the Si3400/01 or Si3402 evaluation boards configured to present a Class 4 load if POE+ is desired. If one of these boards is used, it should be configured to present a minimum load of > 0.25 W to ensure that it draws at least 10 mA to comply with the IEEE standard.

When the Si3462 is applying power to a valid PD, the LED is continuously lit. After an error condition (e.g., an UVLO or short-circuit event) is detected, the LED flashes at 10 times per second. The flashing will continue for 2.2 seconds or until an open circuit is detected as determined by the operating mode of the Si3462.

The Si3462 mode is set by the voltage levels provided by resistors R100 through R103 and DIP switch SW2 according to Table 2 on page 7. Note that each resistor should be connected to either the 3.3 V supply rail or to ground in order to generate correct voltages (i.e. the two corresponding switches should be in opposite positions). Odd-numbered switches connect the resistors to the 3.3 V supply, and even-numbered switches connect them to ground. The MSB is controlled by switches 1 and 2. After changing the settings, push the reset button for the new mode to take effect.

The reference board is shipped configured for midspan power injection with full power support and automatic retry after a fault (DIP switch setting 01101010).

14. Summary

With its fully-compliant PSE interface, the Si3462-EVB provides a simple and comprehensive applications solution for PSE system designers who require IEEE-compliant PSE functionality and safe operation with standard telephone interfaces and voltages.

15. Ordering Guide

Ordering Part Number	Description
Si3462-EVB	Evaluation board kit for Si3462-EVB reference design.
Si3462-XYY-GM	Ordering part number for Si3462 devices. X = device revision; YY = firmware revision. Refer to the Si3462 data sheet Ordering Guide for current ordering information.

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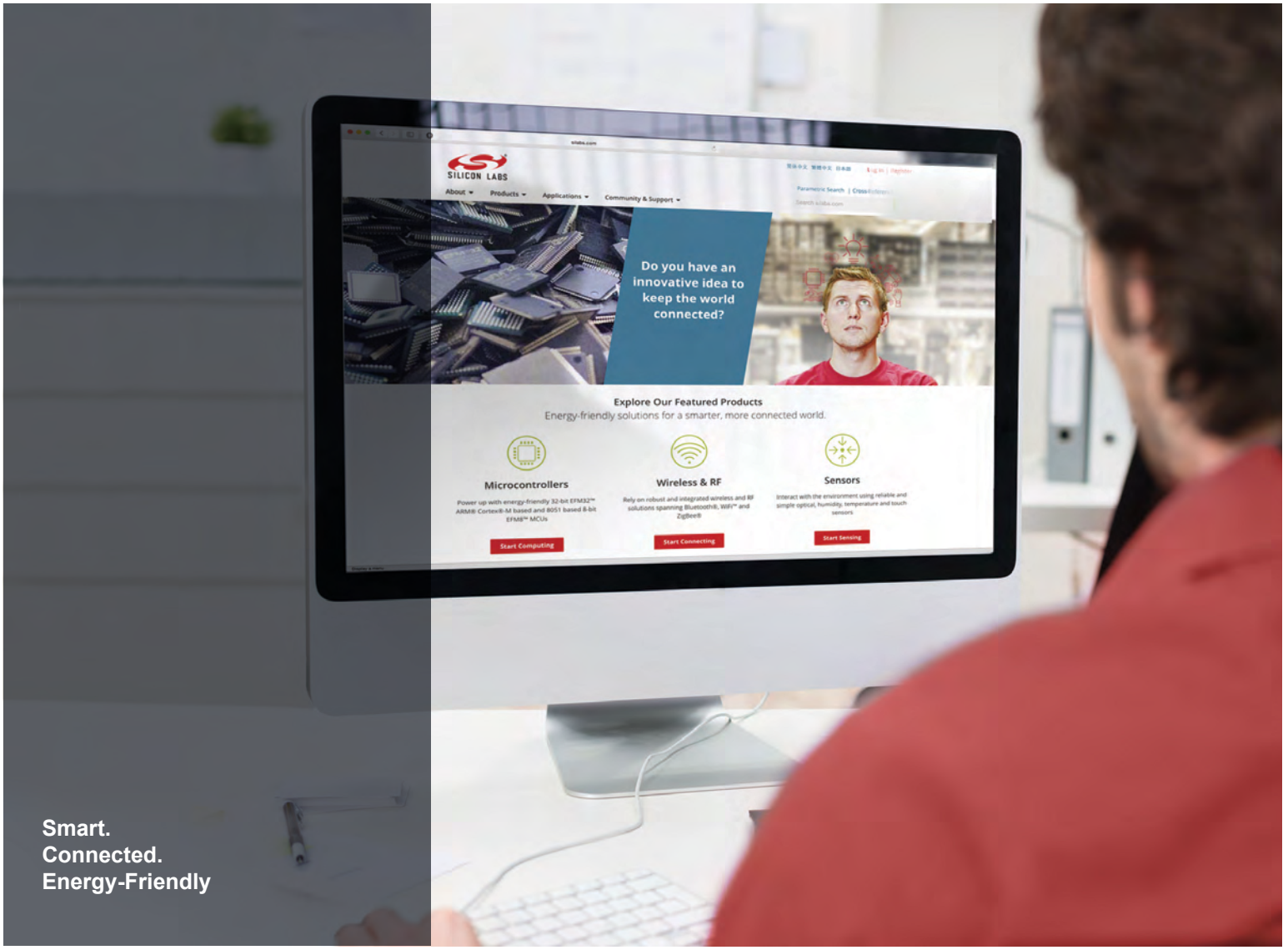
Document Change List

Revision 1.0 to Revision 1.1

- Updated "15. Ordering Guide" on page 30.
  - Updated ordering part number to Si3462-EVB.

Revision 1.1 to Revision 1.2

- Updated Figure 14 on page 17.



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