



STD20NF10

N-channel 100V - 0.038Ω - 100A - DPAK
Low gate charge STripFET™ II Power MOSFET

Features

Type	V _{DSS}	R _{DS(on)}	I _D
STD20NF10	100V	<0.045Ω	25A ⁽¹⁾

1. Current limited by package

- Exceptional dv/dt capability
- Application oriented characterization

Description

This MOSFET series realized with STMicroelectronics unique STripFET process has specifically been designed to minimize input capacitance and gate charge. It is therefore suitable as primary switch in advanced high-efficiency, high-frequency isolated DC-DC converters for Telecom and Computer applications. It is also intended for any applications with low gate drive requirements.

Applications

- Switching applications

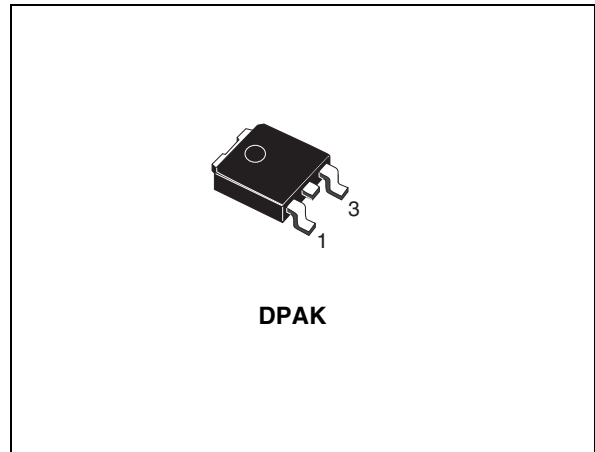


Figure 1. Internal schematic diagram

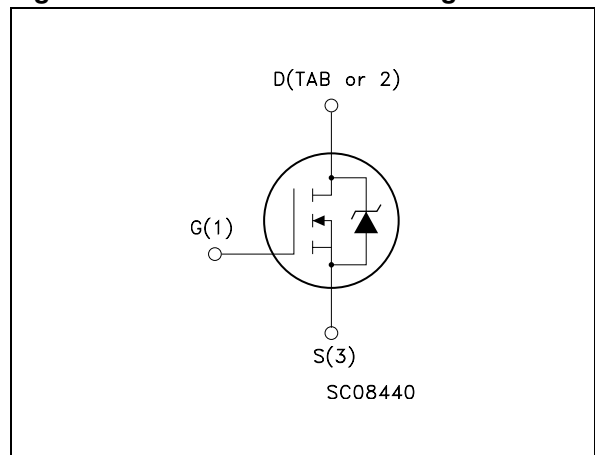


Table 1. Device summary

Part number	Marking	Package	Packaging
STD20NF10T4	D20NF10	DPAK	Tape & reel

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1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage ($V_{GS} = 0$)	100	V
V_{DGR}	Drain-gate voltage ($R_{GS} = 20\text{ k}\Omega$)	100	V
V_{GS}	Gate- source voltage	± 20	V
$I_D^{(1)}$	Drain current (continuous) at $T_C = 25^\circ\text{C}$	25	A
I_D	Drain current (continuous) at $T_C = 100^\circ\text{C}$	21	A
$I_{DM}^{(2)}$	Drain current (pulsed)	100	A
P_{tot}	Total dissipation at $T_C = 25^\circ\text{C}$	85	W
	Derating Factor	0.57	W/ $^\circ\text{C}$
$dv/dt^{(3)}$	Peak diode recovery avalanche energy	20	V/ns
$E_{AS}^{(4)}$	Single pulse avalanche energy	300	mJ
T_{stg}	Storage temperature	-55 to 175	$^\circ\text{C}$
T_j	Max. operating junction temperature		

1. Current limited by package
2. Pulse width limited by safe operating area.
3. $I_{SD} \leq 25\text{A}$, $di/dt \leq 300\text{A}/\mu\text{s}$, $V_{DD} = V_{(BR)DSS}$, $T_j \leq T_{JMAX}$
4. Starting $T_j = 25^\circ\text{C}$, $I_D = 10\text{A}$, $V_{DD} = 27\text{V}$

Table 3. Thermal data

$R_{thj-case}$	Thermal resistance junction-case max	1.76	$^\circ\text{C}/\text{W}$
$R_{thj-amb}$	Thermal resistance junction-ambient max	100	$^\circ\text{C}/\text{W}$
T_J	Maximum lead temperature for soldering purpose	300	$^\circ\text{C}$

2 Electrical characteristics

($T_{CASE}=25^{\circ}\text{C}$ unless otherwise specified)

Table 4. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 250\mu\text{A}$, $V_{GS} = 0$	100			V
I_{DSS}	Zero gate voltage drain current ($V_{GS} = 0$)	$V_{DS} = \text{Max rating}$ $V_{DS} = \text{Max rating}$, $T_C = 125^{\circ}\text{C}$			1 10	μA μA
I_{GSS}	Gate-body leakage current ($V_{DS} = 0$)	$V_{GS} = \pm 20\text{V}$			± 100	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$, $I_D = 250\mu\text{A}$	2	3	4	V
$R_{DS(on)}$	Static drain-source on resistance	$V_{GS} = 10\text{V}$, $I_D = 15\text{A}$		0.038	0.045	Ω

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$g_{fs}^{(1)}$	Forward transconductance	$V_{DS} = 15\text{V}$, $I_D = 15\text{A}$		10		S
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	$V_{DS} = 25\text{V}$, $f = 1\text{MHz}$, $V_{GS} = 0$		1200 180 80		pF pF pF
$t_{d(on)}$ t_r $t_{d(off)}$ t_f	Turn-on delay time Rise time Turn-off delay time Fall time	$V_{DD} = 50\text{V}$, $I_D = 15\text{A}$ $R_G = 4.7\Omega$, $V_{GS} = 10\text{V}$ (see Figure 14)		15 40 45 10		ns ns ns ns
Q_g Q_{gs} Q_{gd}	Total gate charge Gate-source charge Gate-drain charge	$V_{DD} = 80\text{V}$, $I_D = 30\text{A}$, $V_{GS} = 10\text{V}$, $R_G = 4.7\Omega$ (see Figure 15)		40 8 15	55	nC nC nC

1. Pulsed: Pulse duration = 300 μs , duty cycle 1.5%.

Table 6. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD} $I_{SDM}^{(1)}$	Source-drain current Source-drain current (pulsed)				30 120	A A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 20A$, $V_{GS} = 0$			1.3	V
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	$I_{SD} = 30A$, $di/dt = 100A/\mu s$, $V_{DD} = 55V$, $T_j = 150^\circ C$ (see Figure 16)		110 390 7.5		ns μC A

1. Pulse width limited by safe operating area.

2. Pulsed: Pulse duration = 300 μs , duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

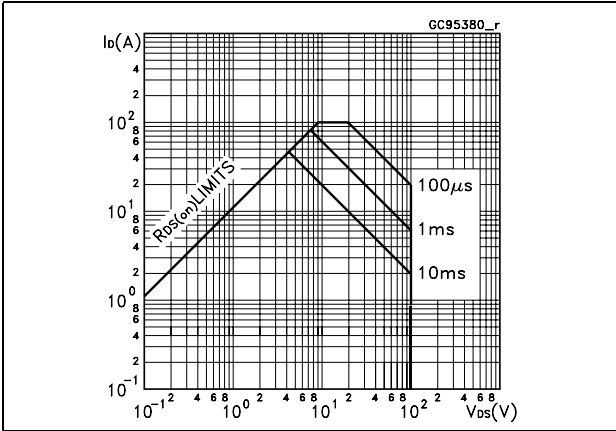


Figure 3. Thermal impedance

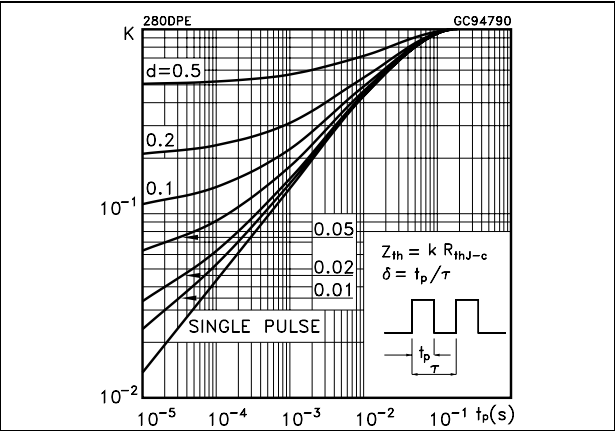


Figure 4. Output characteristics

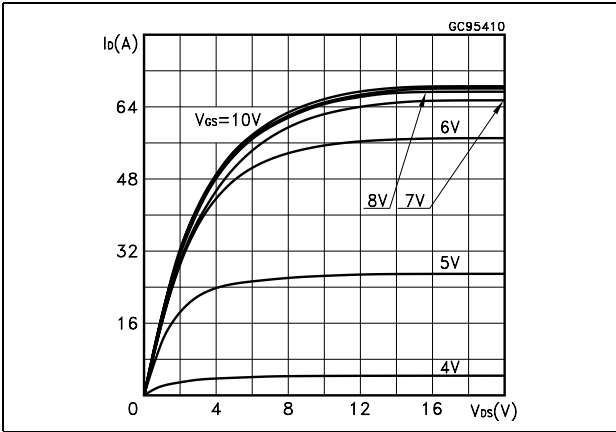


Figure 5. Transfer characteristics

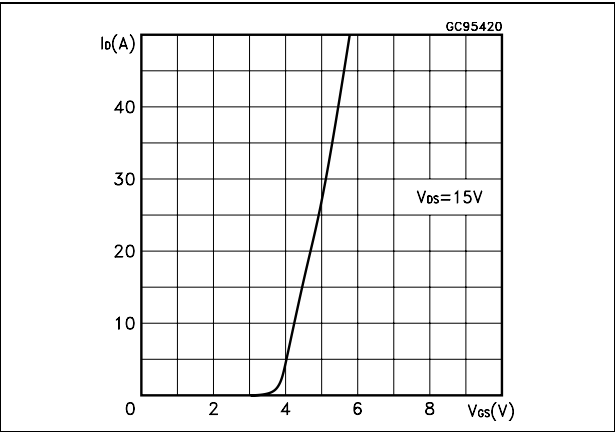


Figure 6. Transconductance

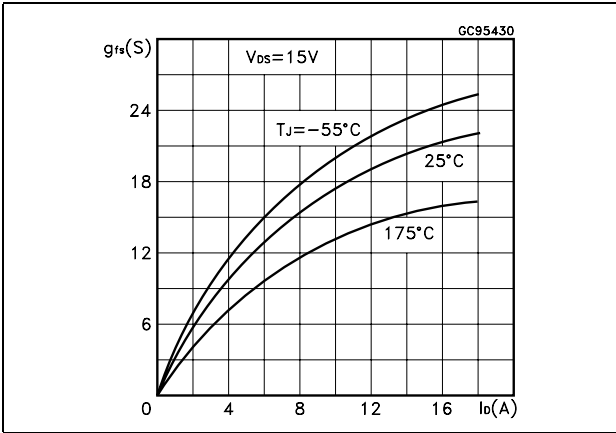


Figure 7. Static drain-source on resistance

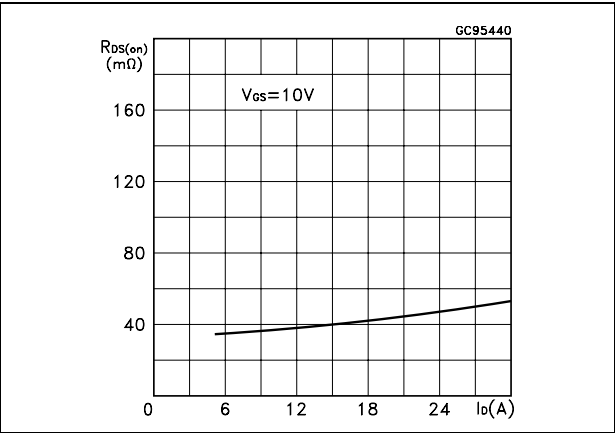


Figure 8. Gate charge vs. gate-source voltage Figure 9. Capacitance variations

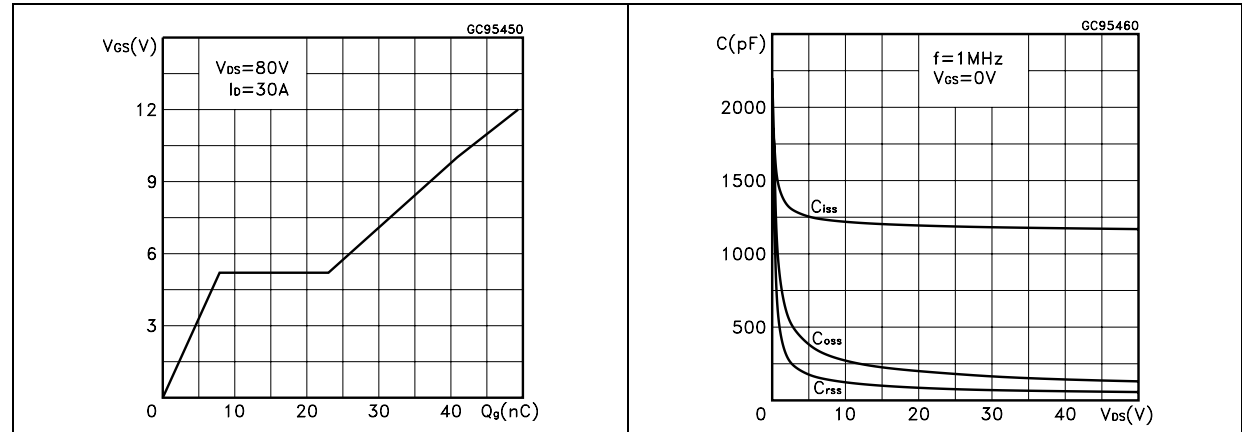


Figure 10. Normalized gate threshold voltage vs. temperature Figure 11. Normalized on resistance vs. temperature

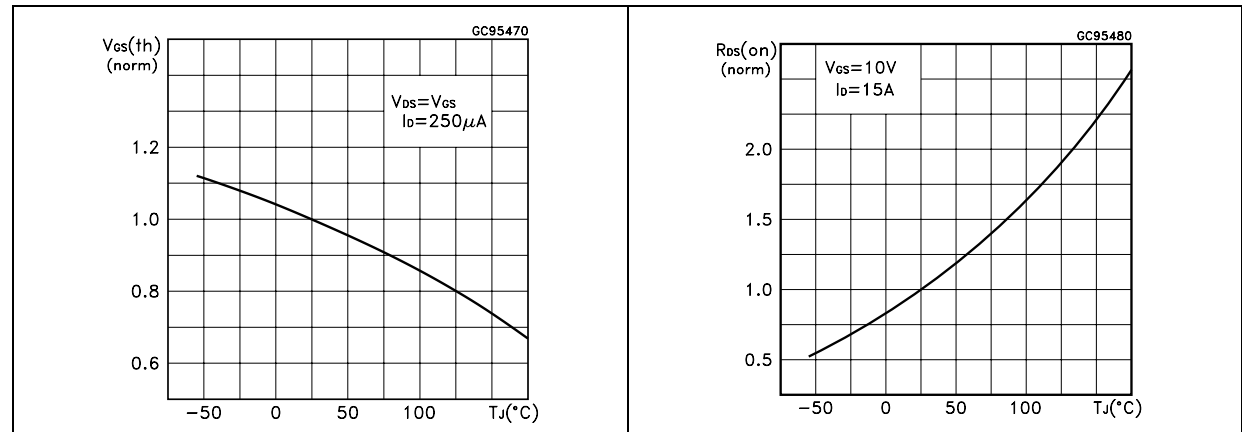
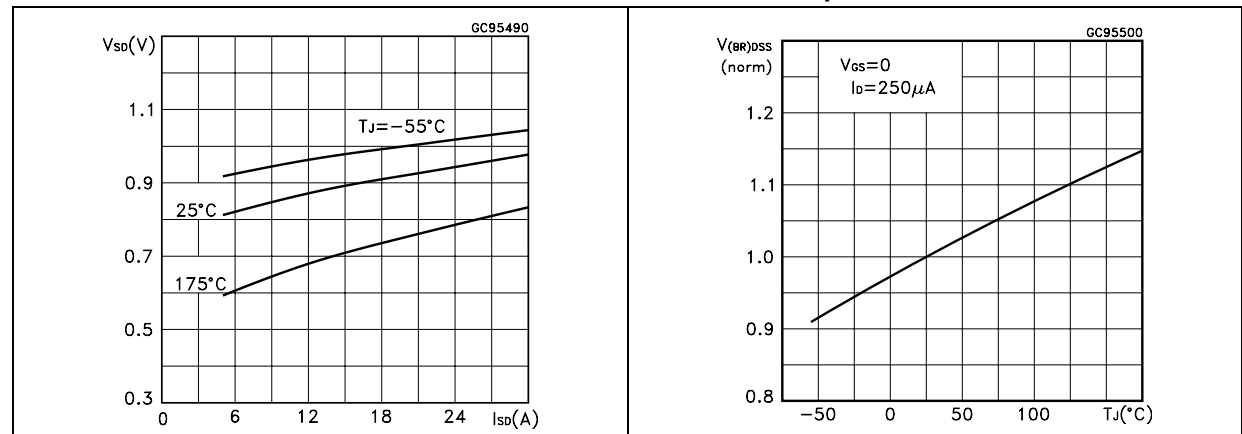


Figure 12. Source-drain diode forward characteristics Figure 13. Normalized breakdown voltage vs. temperature



3 Test circuit

Figure 14. Switching times test circuit for resistive load



Figure 15. Gate charge test circuit

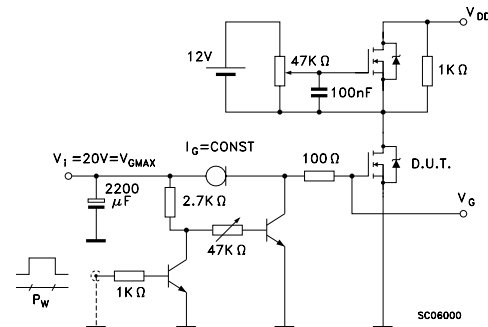


Figure 16. Test circuit for inductive load switching and diode recovery times



Figure 17. Unclamped Inductive load test circuit

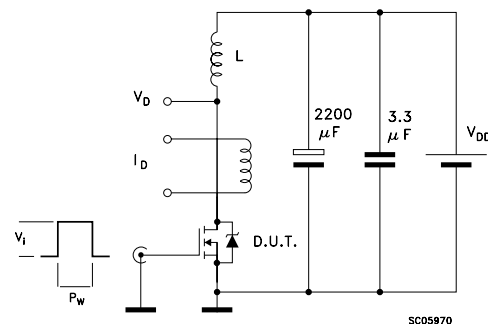


Figure 18. Unclamped inductive waveform

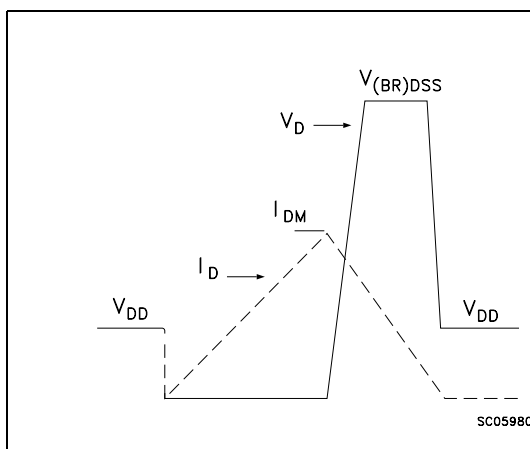
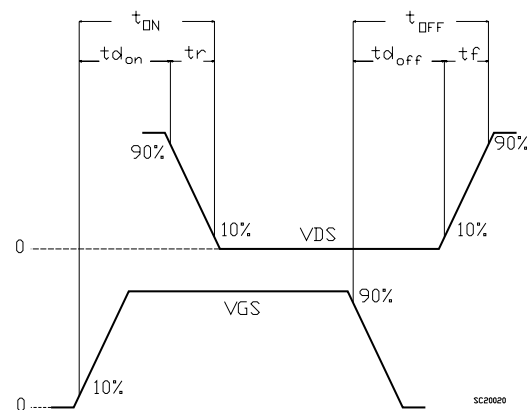


Figure 19. Switching time waveform



4 Package mechanical data

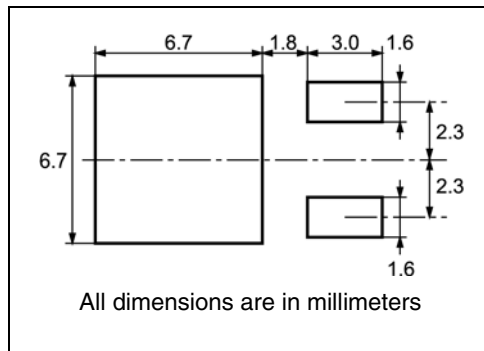
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DPAK MECHANICAL DATA						
DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	2.2		2.4	0.086		0.094
A1	0.9		1.1	0.035		0.043
A2	0.03		0.23	0.001		0.009
B	0.64		0.9	0.025		0.035
b4	5.2		5.4	0.204		0.212
C	0.45		0.6	0.017		0.023
C2	0.48		0.6	0.019		0.023
D	6		6.2	0.236		0.244
D1		5.1			0.200	
E	6.4		6.6	0.252		0.260
E1		4.7			0.185	
e		2.28			0.090	
e1	4.4		4.6	0.173		0.181
H	9.35		10.1	0.368		0.397
L	1			0.039		
(L1)		2.8			0.110	
L2		0.8			0.031	
L4	0.6		1	0.023		0.039
R		0.2			0.008	
V2	0°		8°	0°		8°

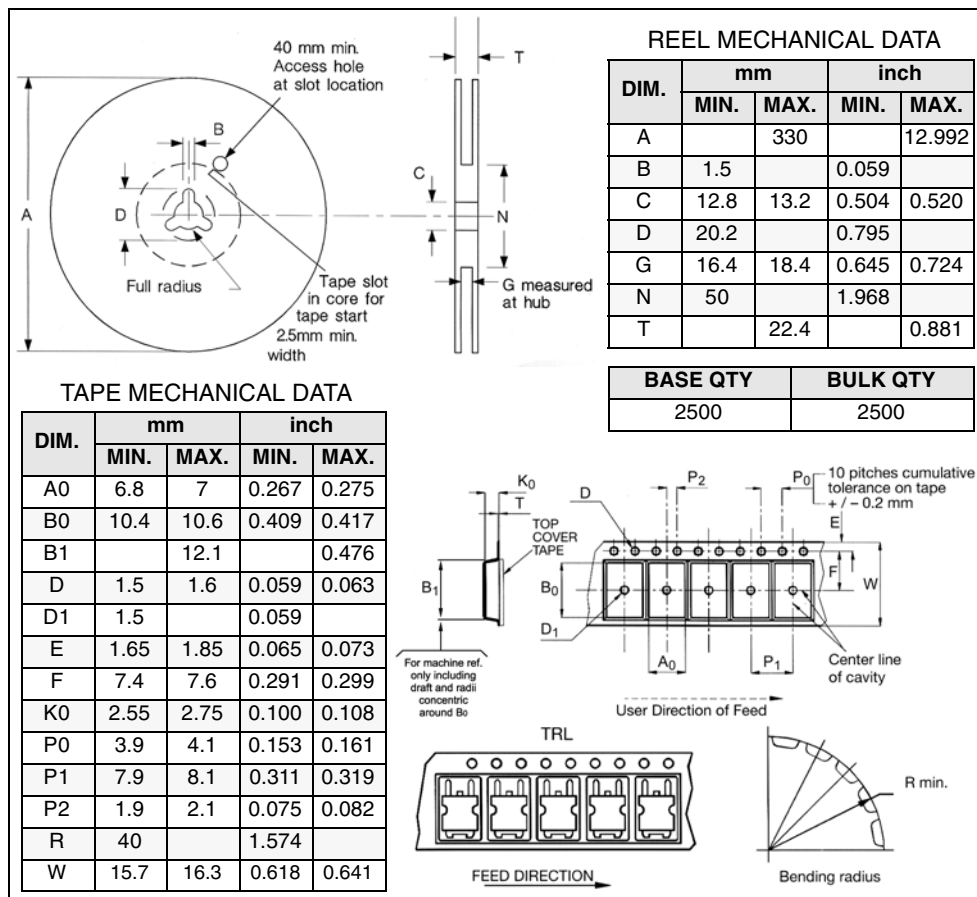
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5 Packing mechanical data

DPAK FOOTPRINT



TAPE AND REEL SHIPMENT



6 Revision history

Table 7. Revision history

Date	Revision	Changes
21-Jun-2004	3	Preliminary datasheet
03-Jul-2006	4	New template, no content change
13-Aug-2007	5	Updated marking on Table 1

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