# 1.5 A low-dropout linear regulator with programmable soft-start
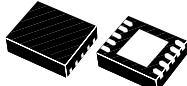
DFN10 3 x 3
wettable flanks

Features

- Designed for automotive applications
- Dual supply pins
    - V_{IN}: 0.8 V to 5.5 V
    - V_{BIAS}: 2.7 V to 5.5 V
- V_{OUT} range: 0.8 V to 3.6 V
- Ultra low-dropout: 65 mV typ. (125 mV max.) at 1.5 A
- High V_{OUT} accuracy
    - 0.5% typ. at T_{amb}
    - 2% max.
- Power Good function
- Programmable soft-start
- Thermal shutdown
- Current limitation circuit
- Adjustable output voltage
- Stable with low ESR output capacitor (> 2.2 μF)
- Available in DFN10 3 x 3 mm package with wettable flanks
- Operating temperature range: - 40 °C + 125 °C

Applications

- Automotive and industrial post regulation
- Generic POL
- Automotive and industrial ASICs and FPGA supply
- Telecom infrastructure
- A.D.A.S. (advanced driver-assistance systems)

Description

The LD59150 is a 1.5 A LDO regulator, designed for being used in various environments.

The NMOS topology allows $R_{DS(on)}$ of the pass-element to be reduced, which results in a very small dropout voltage even with very low input supply voltage.

Output voltage can be adjusted from 0.8 to 3.6 V, by means of an external resistor divider.

The programmable soft-start circuit offers the possibility to control the inrush current at startup providing a monotonic supply voltage to the load.

The LD59150 has enable pin to turn on/off (EN) the regulator and Power Good to monitor the regulated output voltage (PG).

Combination of both can be used to set a desired power sequence in case of multiple regulated rails.

The LD59150 embeds protection functions, such as: current limit and thermal shutdown.

| Maturity status link	
LD59150	
Device summary	
Order code	LD59150PURY
Marking	595A
Output voltage	Adjustable

1 Diagram

Figure 2. Block diagram
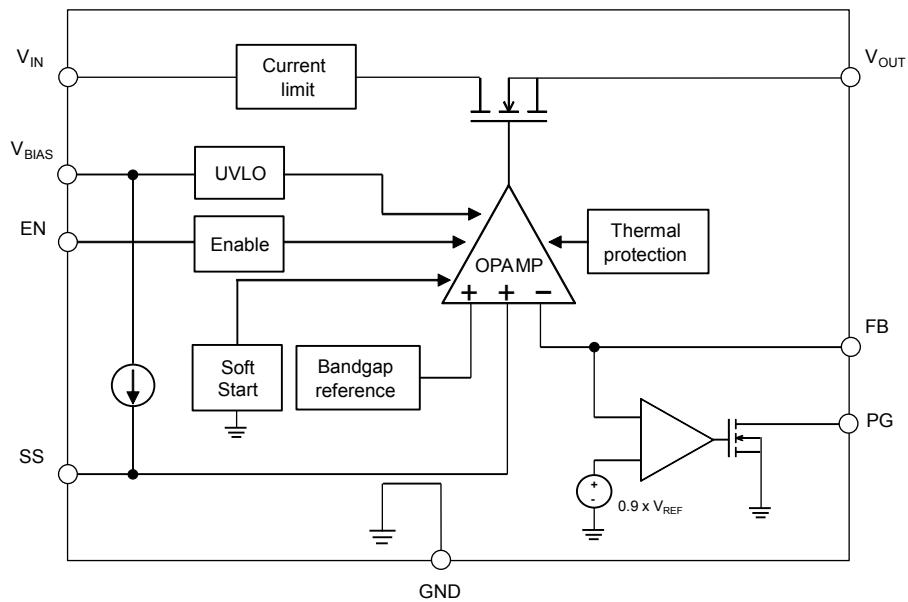
2 Pin configuration

**Figure 3. Pin connection (top view)**
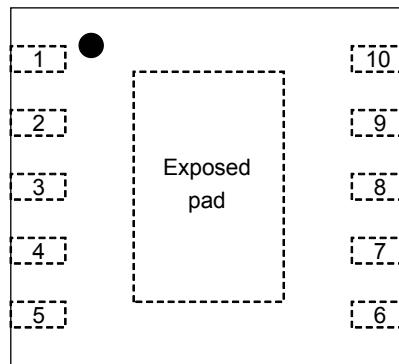
DFN10 - 3 x 3

Table 1. Pin description

Pin n°	Symbol	Function
1, 2	V_{IN}	Input pin
3	PG	Power Good
4	V_{BIAS}	Bias supply pin
5	EN	Enable pin logic input: low = shutdown, high = active Don't leave floating
6	GND	Ground
7	SS	Soft-start
8	FB	Feedback pin
9, 10	V_{OUT}	Regulated output
Exp. pad	Exposed pad	Must be connected to GND

3 Typical application

Figure 4. Typical application circuit
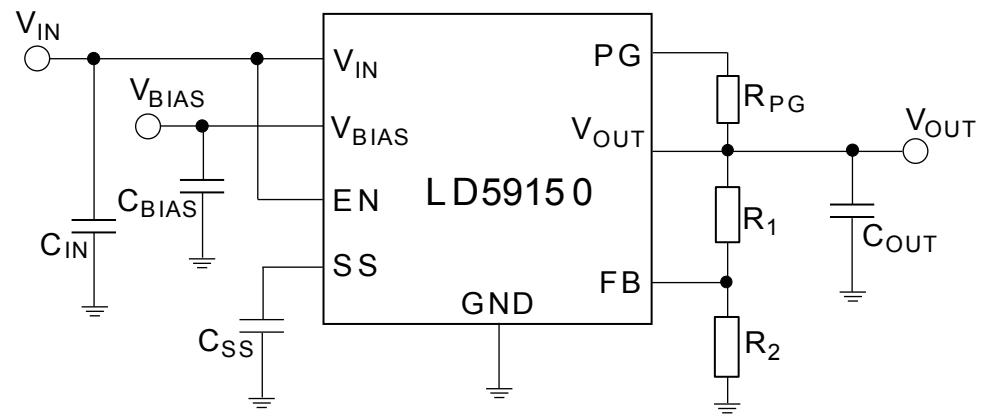
4   Maximum ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{IN}	Input voltage pin	-0.3 to 6	V
V_{BIAS}	Bias supply pin	- 0.3 to 6	V
V_{OUT}	DC output voltage	-0.3 to V_{IN} + 0.3	V
V_{EN}	Enable input voltage	-0.3 to 6	V
V_{ADJ}	Adjustable pin voltage	-0.3 to 6	V
V_{SS}	Soft-start pin	-0.3 to 6	V
V_{PG}	Power Good pin	-0.3 to 6	V
I_{OUT}	Output current	Internally limited	mA
P_{DIS}	Maximum power dissipation	Refer to table 3	W
I_{PG}	Power Good sink current	0 to 1.5	mA
T_{ST}	Storage temperature range	-55 to 150	°C
T_J	Operating junction temperature range	-40 to 150	°C

Note: *Absolute maximum ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. All values are referred to GND.*

Table 3. Thermal data

Symbol	Parameter	Value	Unit
R_{thJA}	Thermal resistance junction-ambient	47.5	°C/W
R_{thJC}	Thermal resistance junction-case	8	°C/W

Note: *Thermal resistance refers to 4 layer JEDEC PCB (2S2P) test board with thermal vias.*

Table 4. ESD data

Symbol	Parameter	DFN10 3 x 3	Unit
HBM	Human body model	± 2000	V
CDM	Charged device model	± 750	V

5 Electrical characteristics

T_J = - 40 °C to + 125 °C, typical values refer to T_J = + 25 °C, V_{IN} = V_{OUT} + 0.3 V, V_{EN} = 1.1 V, V_{BIAS} = 5 V, I_{OUT} = 50 mA, C_{IN} = C_{OUT} = 10 µF, C_{BIAS} = 0.1 µF, C_{SS} = 1 nF unless otherwise specified.

Table 5. Electrical characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{IN}	Operating input voltage		V_{OUT}+ V_{drop}		5.5	V
V_{BIAS}	Bias pin voltage		2.7		5.5	V
V_{REF}	Reference voltage	T = + 25 °C	0.796	0.8	0.804	V
V_{OUT}	Range	V_{IN} = 5.5 V, I_{OUT} = 1.5 A	V_{REF}		3.6	V
	Accuracy	50 mA < I_{OUT} < 1.5 A 2.97 V < V_{BIAS} < 5.5 V	-2	± 0.5	+2	%
	Line regulation	$V_{OUT(nom)}$ + 0.3 V < V_{IN} < 5.5 V		0.01		%/V
	Load regulation	50 mA < I_{OUT} < 1.5 A		0.02		%/A
V_{drop} [1]	V_{IN} dropout voltage	I_{OUT} = 1.5 A, V_{BIAS} - V_{OUT} > 3.25 V		65	125	mV
	V_{BIAS} dropout voltage	I_{OUT} = 1.5 A V_{IN} = V_{BIAS}		0.92	1.1	V
I_{cl} [2]	Current limit	V_{OUT} = 80% x $V_{OUT(nom)}$	2.0	3	5.5	A
I_{BIAS}	Bias pin current			0.88	1.5	mA
I_{SHDN}	Shutdown supply current	V_{EN} < 0.4 V (measured through GND)		1	50	µA
I_{FB}	Feedback pin current		-1	0.001	+1	µA
PSRR	Power supply rejection (V_{IN} to V_{OUT})	f = 1 kHz, I_{OUT} = 1.5 A V_{IN} = 1.8 V, V_{OUT} = 1.5 V		70		dB
		f = 300 kHz, I_{OUT} = 1.5 A V_{IN} = 1.8 V, V_{OUT} = 1.5 V		30		
	Power supply rejection (V_{BIAS} to V_{OUT})	f = 1 kHz, I_{OUT} = 1.5 A V_{IN} = 1.8 V, V_{OUT} = 1.5 V		75		dB
		f = 300 kHz, I_{OUT} = 1.5 A V_{IN} = 1.8 V, V_{OUT} = 1.5 V		40		
Noise	Output noise voltage	f = 100 Hz to 100 kHz, I_{OUT} = 1.5 A, C_{SS} = 1 nF		25xV_{OUT}		µV$_{RMS}$
I_{SS}	Soft start charging current	V_{SS} = 0.4 V		0.44		µA
T_{str}	Min. startup time	I_{OUT} = 1 A, C_{SS} = floating		100		µsec
V_{EN-H}	Enable input high		1.1		5.5	V
V_{EN-L}	Enable input low		0		0.4	V
$V_{EN-Hyst}$	Enable hysteresis			50		mV
T_{DG}	Enable deglitch time			20		µsec
I_{EN}	Enable pin current	V_{EN} = 5 V		0.1	1	µA
V_{IT}	Power Good threshold	V_{OUT} decreasing	85	90	94	%V_{OUT}
V_{HYS}	Power Good hysteresis			3		%V_{OUT}

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{PG-L}	Power good low voltage				0.3	V
I_{LK}	Power good leakage	V_{PG} = 5.25 V, V_{OUT} > V_{IT}		0.1	1	µA
T_{SD}	Thermal shutdown temperature	High temp threshold		165		°C
		Thermal hysteresis		20		

1. *Dropout is defined as the voltage drop when V_{OUT} is 3% below nominal voltage.*

2. *Maximum value is guaranteed by design and not tested in production.*

6 Application information

6.1 Output voltage setting

The output voltage can be set from 0.8 V (V_{REF}) up to the input voltage minus the voltage drop across the pass transistor (dropout voltage), by connecting a resistor divider between the feedback (FB) pin and the output, thus allowing remote voltage sensing.

With reference to the typical circuit shown in Figure 3, the resistor divider can be designed by using the following equation:

$$V_{OUT} = V_{REF} (1 + R_1/R_2), \text{ with } V_{REF} = 0.8 \text{ V typ.} \tag{1}$$

It is recommended to use resistors with values in the range from 5 kΩ to 100 kΩ. Lower values can also be suitable, but current consumption increases.

The following table shows examples of R_1, R_2 choices, among standard 1% resistors, to obtain the most common output voltages.

Table 6. Resistor divider settings for common output voltages

V_{OUT}	R_1	R_2
0.8 (V_{FB})	Short	Open
0.9	0.619	4.99
1	1.13	4.53
1.05	1.37	4.42
1.1	1.87	4.99
1.2	2.49	4.99
1.5	4.12	4.75
1.8	3.57	2.87
2.5	3.57	1.69
3.3	3.57	1.15

6.2 Soft-start time programming

The LD59150 provides a monotonic soft-start feature, which is useful in those applications requiring controlled power-up sequences and low inrush current during turn-on phase.

The soft-start time, defined as the duration of output voltage ramp, from enable pin assertion to Power Good flag releasing, can be adjusted by the user by means of an external capacitor (C_{SS}).

C_{SS} capacitor is charged with constant current (I_{SS}) and its voltage compared to the internal voltage reference, therefore the soft-start time can be calculated as follows:

$$t_{SS} = (V_{REF} \times C_{SS}) / I_{SS} \tag{2}$$

with V_{REF} = 0.8 V typ., I_{SS} = 0.44 µA typ.

Good quality, low leakage ceramic capacitors are recommended for C_{SS}.

6.3 Power Good

Power Good function provides a flag showing that the output voltage is in the correct range. Power Good signal is available on the PG open-drain pin.

A partition of the output voltage (via the output resistor divider), is sensed at the feedback pin.

When the output voltage surpasses V_{IT} + V_{HYS} Power Good pin is set to high impedance. When V_{OUT} falls below V_{IT}, the Power Good pin is pulled low.

If the device is disabled (EN pin low) the PG signal is set to low state.

Power Good function requires an external pull-up resistor, which may be connected to any potential lower than 5.5 V. PG pin typical current capability is up to 1 mA, so it is advisable to choose a pull-up resistor in the range from 10 kΩ to 1 MΩ. If Power Good function is not used, PG pin has to remain floating.

6.4 Protection features

Current limit

The LD59150 embeds a constant-current limit circuit, which acts in case of overload or short-circuit on the output, clamping the load current to a safe value (typ. 3 A).

Normal operation is restored if the overload disappears, but prolonged operation in current limit may lead to high power dissipation inside the LDO and subsequently to thermal shutdown.

Thermal potection

An internal thermal feedback loop disables the output voltage if the die temperature reaches approximately 165 °C. This feature protects the device from excessive temperature that could lead to permanent damage of the LDO.

Once the thermal protection is triggered and the device is shut down, normal operation is automatically recovered if the die temperature falls below 145 °C (thermal protection hysteresis of 20 °C typically).

Current and thermal limit protections are designed to protect the LDO from excessive power dissipation and not intended to replace a proper thermal and electrical design of the application. Continuous operation above the maximum ratings may lead to permanent damage to the device.

6.5 Power dissipation

An accurate PCB design is recommended, to ensure that the device internal junction temperature is kept below 150 °C, in all the operating condition. The thermal energy generated by the device flows from the die surface to the PCB copper area through the package leads.

The PCB copper area acts as a heat sink. The footprint copper pads should be as wide as possible to spread and dissipate the heat to the surrounding environment. Thermal micro-vias to the inner or backside copper layers improve the overall thermal performance of the device.

The power dissipation of the LDO depends on the input voltage, output voltage and output current and is given by:

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} \tag{3}$$

The junction temperature of the device is:

$$T_{J\_MAX} = T_A + R_{thJA} \times P_D \tag{4}$$

where: T_{J_MAX} is the maximum allowable junction temperature of the die, 150 °C; T_A is the ambient temperature; R_{thJA} is the thermal resistance junction-to-ambient.

With the above equation it is possible to calculate the maximum allowable power dissipation, therefore the maximum load current for a certain voltage drop. Appropriate de-rating of the operating condition should be applied accordingly.

7 Typical performance characteristics

T_J = 25 °C, V_{IN} = V_{OUT} + 0.3 V, V_{BIAS} = 5 V, V_{OUT} = V_{REF}, V_{EN} = 1.1 V, I_{OUT} = 50 mA, C_{IN} = C_{OUT} = 10 µF, C_{BIAS} = 0.1 µF, C_{SS} = 1 nF unless otherwise specified.

**Figure 5. Output voltage vs. temperature and V_{BIAS} (I_{OUT} = 50 mA)**
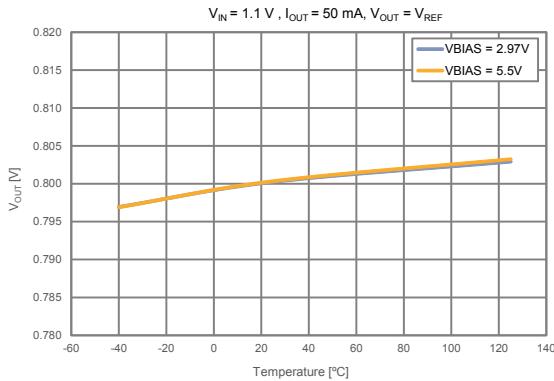
**Figure 6. Output voltage vs. temperature and V_{BIAS} (I_{OUT} = 1.5 A)**
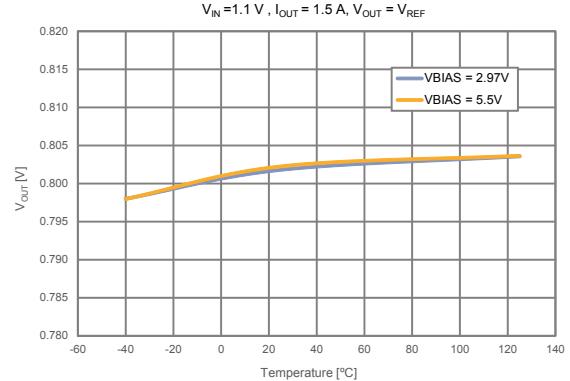
Figure 7. Line regulation vs. temperature
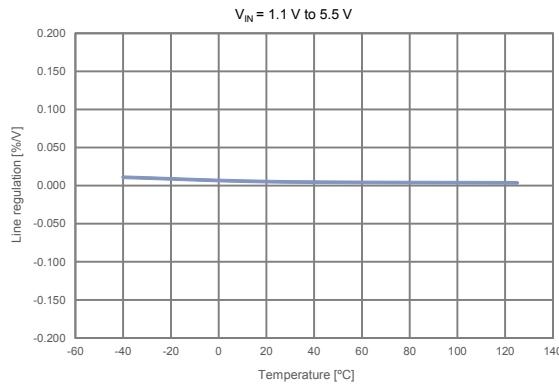
Figure 8. Load regulation vs. temperature
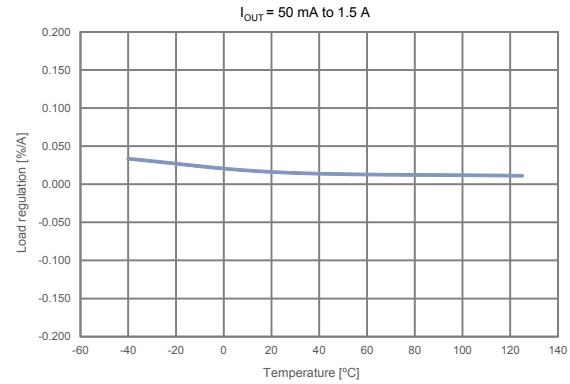
Figure 9. Bias pin current vs. temperature
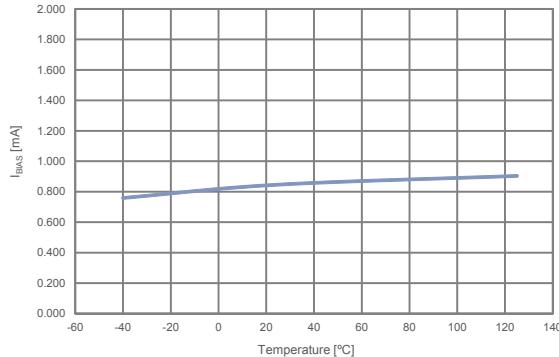
Figure 10. Soft-start charging current vs. temperature
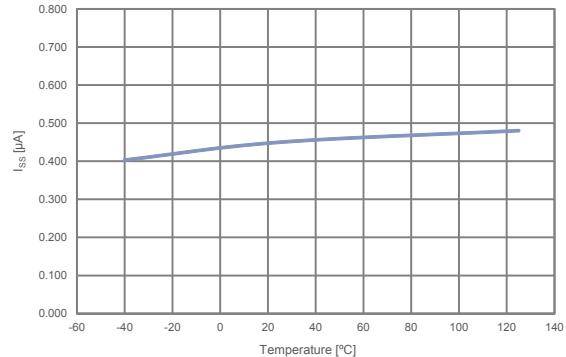
Figure 11. Current limit vs. temperature
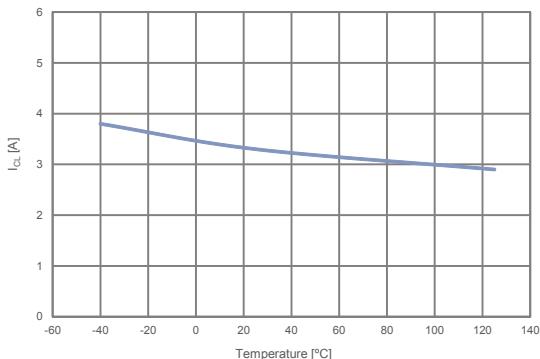
Figure 12. V_{IN} dropout voltage vs. temperature (I_{OUT} = 1.5 A)
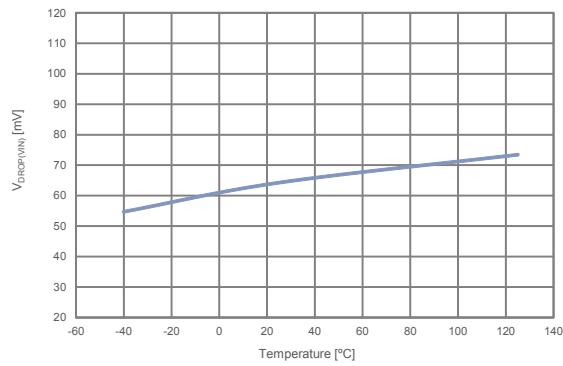
Figure 13. V_{BIAS} dropout voltage vs. temperature (I_{OUT} = 1.5 A)
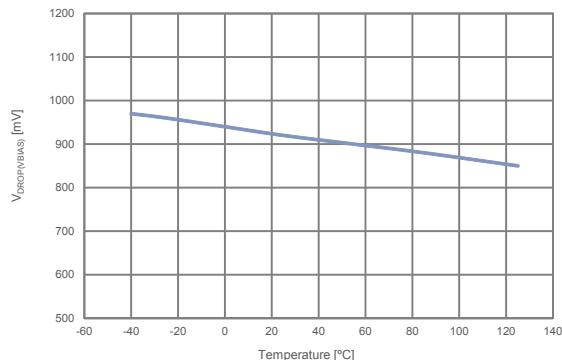
Figure 14. V_{BIAS} PSRR vs. frequency (V_{IN} = 1.8 V, V_{OUT} = 1.2 V)
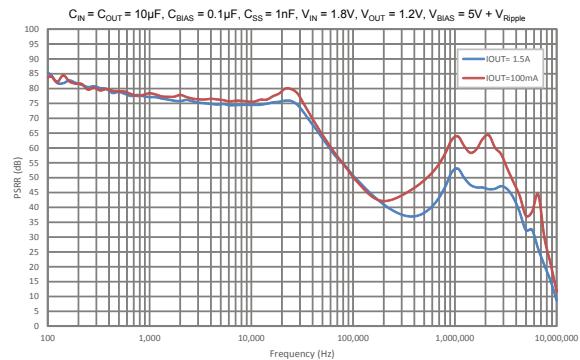
Figure 15. V_{IN} PSRR vs. frequency (V_{IN} = 1.8 V, V_{OUT} = 1.2 V)

C_{IN} = C_{OUT} = 10µF, C_{BIAS} = 0.1µF, C_{SS} = 1nF, V_{IN} = 1.8V + V_{Ripple} , V_{OUT} = 1.2V, V_{BIAS} = 5V
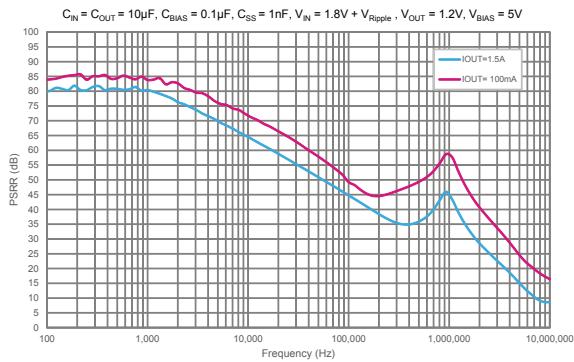
Figure 16. Noise spectral density

C_{IN} = C_{OUT} = 10µF, C_{SS} = 1nF, C_{BIAS} = 0.1µF, V_{IN} = 1.25V, V_{OUT} = 1V, V_{BIAS} = 5V
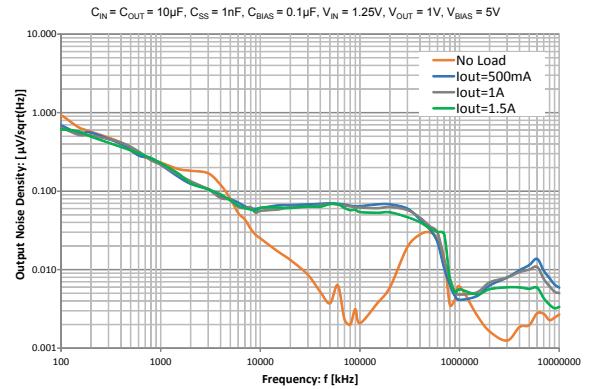
Figure 17. Line transient

V_{IN}=V_{EN}=from 1.1V to 5V and vice versa, V_{BIAS}=5V, tr=tf=5µs
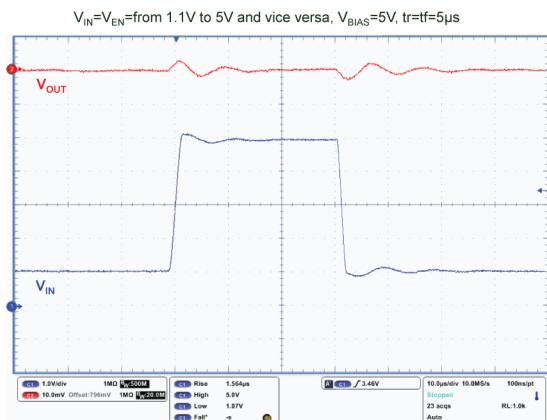
Figure 18. Load transient

V_{IN}=V_{EN}=1.1V, I_{OUT}=from 50mA to 1.5A and vice versa, V_{BIAS}=5V, tr=tf=5µs
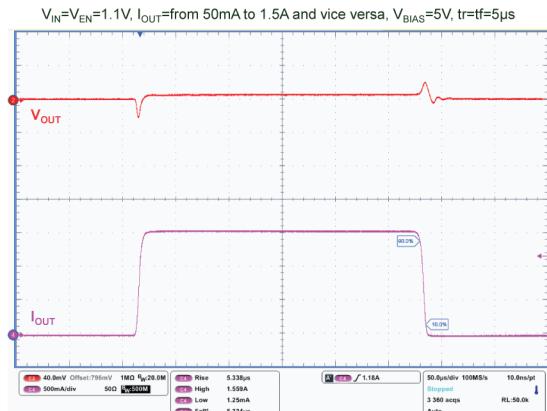
Figure 19. Turn-on time (C_{SS} = 0 nF)

V_{IN}= 5.5V, V_{EN}= from 0 to 5.5V, V_{BIAS}= 5V, I_{OUT}=1mA, No C_{SS}
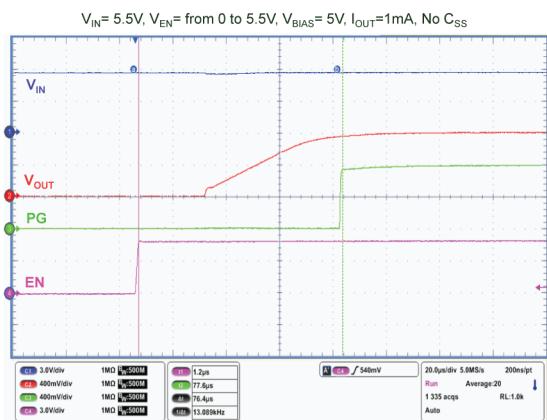
Figure 20. Turn-on time (C_{SS} = 1 nF)

V_{IN}= 5.5V, V_{EN}= from 0 to 5.5V, V_{BIAS}= 5V, I_{OUT}=1mA, C_{SS}=1nF
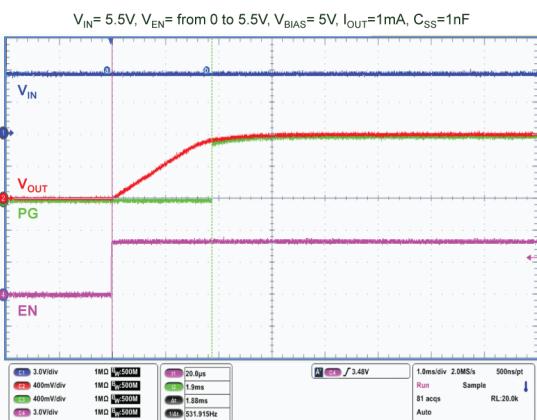
Figure 21. Turn-on time (C_SS = 2.2 nF)

V_{IN}= 5.5V, V_{EN}= from 0 to 5.5V, V_{BIAS}= 5V, I_{OUT}=1mA, C_{SS}=2.2nF
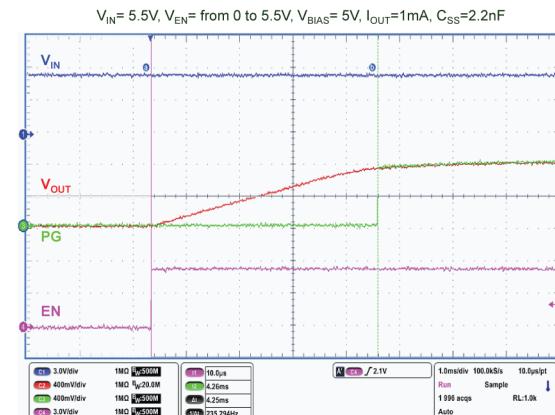
Figure 22. Turn-on time (C_SS = 10 nF)

V_{IN}= 5.5V, V_{EN}= from 0 to 5.5V, V_{BIAS}= 5V, I_{OUT}=1mA, C_{SS}=1nF
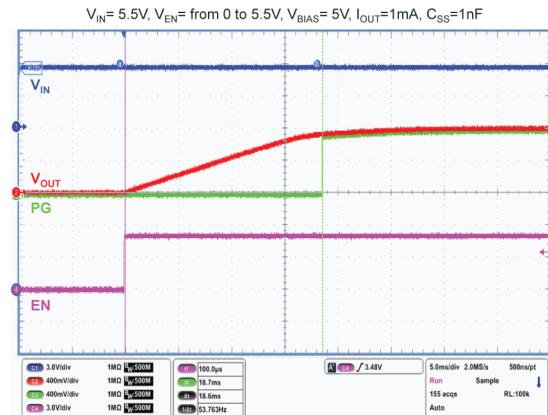
8 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

8.1 [Package name] package information

Figure 23. DFN10 3 x 3 package outline

BOTTOM VIEW
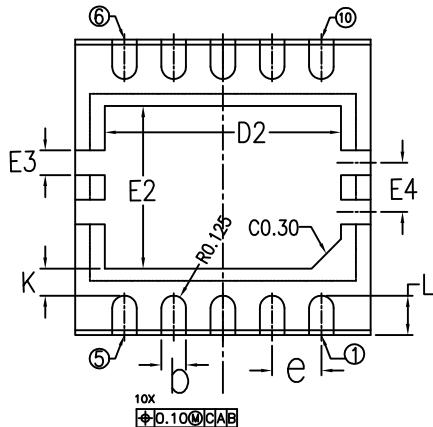
DETAIL A
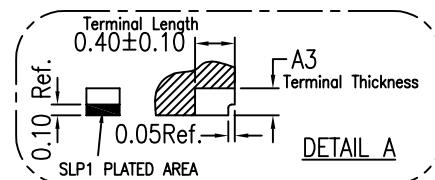
SIDE VIEW
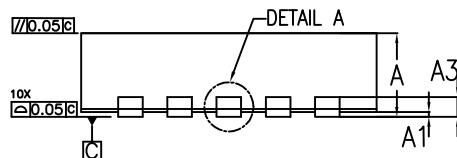
SIDE VIEW
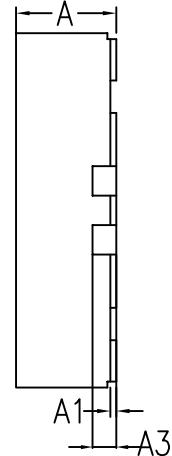
TOP VIEW
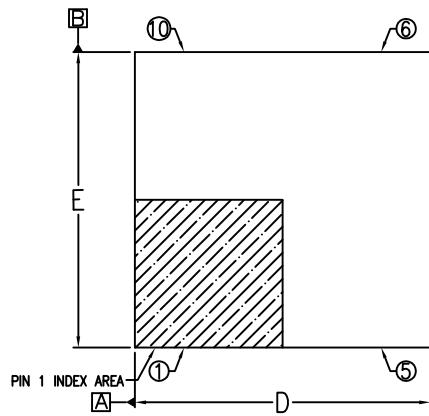
Table 7. **DFN10 3 x 3 mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A	0.80	0.85	0.90
A1	0.00		0.05
A3	0.203 Ref.		
b	0.20	0.25	0.30
D	2.95	3.00	3.05
D2	2.30	2.40	2.50
e	0.50 BSC		
E	2.95	3.00	3.05
E2	1.55	1.65	1.75
E3	0.25 Ref.		
E4	0.50 Ref.		
L	0.30	0.40	0.50
K	0.275 Ref.		
N	10		
aaa	0.15		
bbb	0.10		
ccc	0.10		
ddd	0.05		
eee	0.08		

Figure 24. **DFN10 3 x 3 recommended footprint**
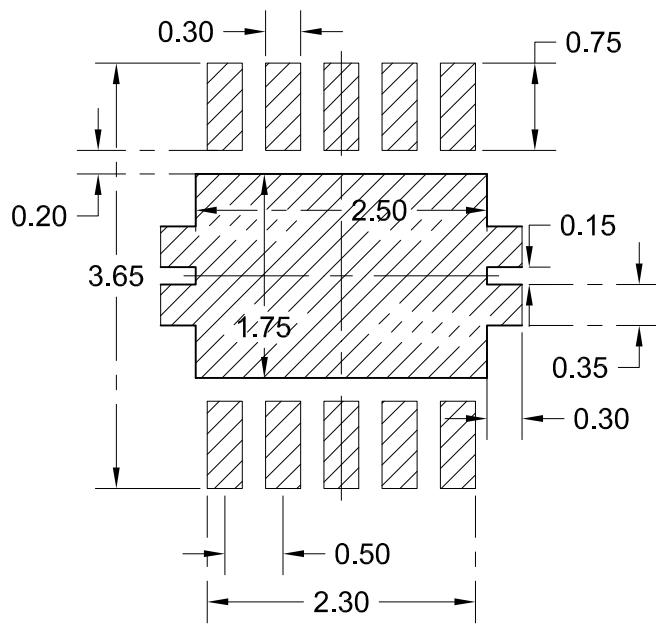
Figure 25. DFN10 3 x 3 tape and reel
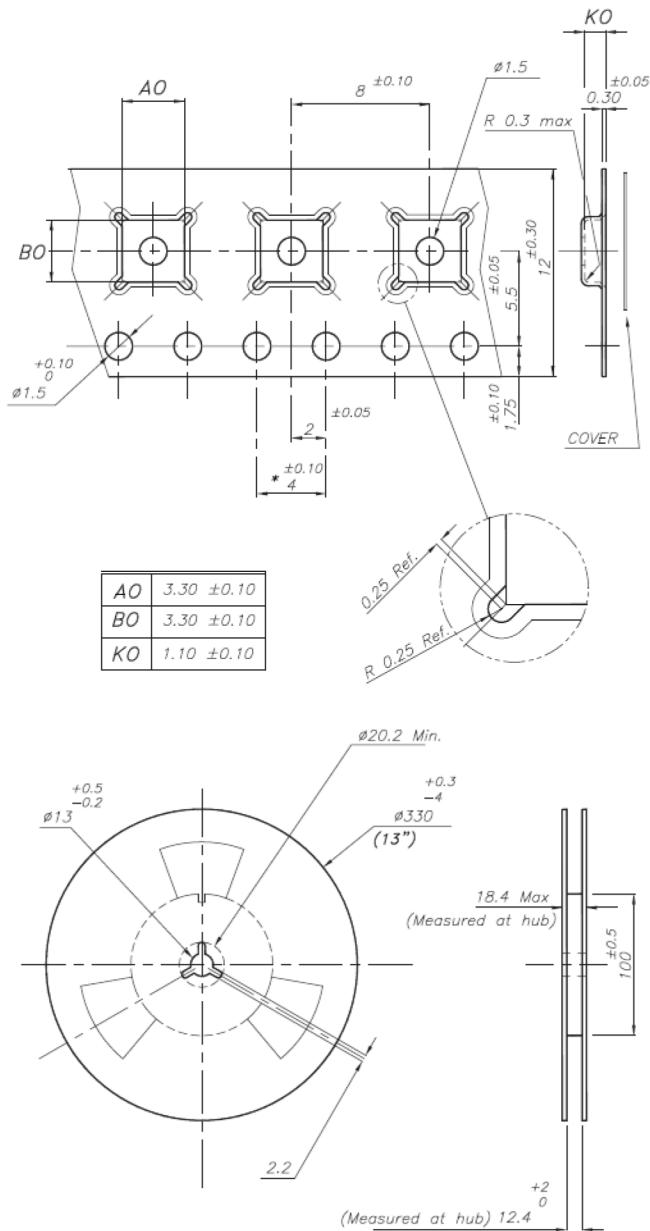
Revision history

Table 8. Document revision history

Date	Revision	Changes
06-Mar-2018	1	Initial release.
15-May-2018	2	Updated marking in the device summary on the cover page.
22-Jun-2018	3	Added footnote I_{CL} in Table 5. Electrical characteristics. Minor text change in Section 6.3 Power Good.

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На всех этапах разработки и производства наши партнеры могут получить квалифицированную поддержку опытных инженеров.

Система менеджмента качества компании отвечает требованиям в соответствии с ГОСТ Р ИСО 9001, ГОСТ РВ 0015-002 и ЭС РД 009

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