



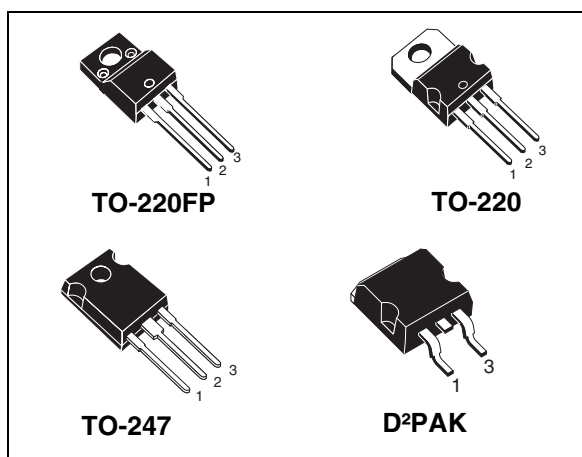
# STB23NM50N, STF23NM50N STP23NM50N, STW23NM50N

N-channel 500 V, 0.162  $\Omega$ , 17 A TO-220, TO-220FP, TO-247, D<sup>2</sup>PAK  
MDmesh™ II Power MOSFET

## Features

Order codes	V <sub>DSS</sub> (@T <sub>jmax</sub> )	R <sub>DS(on)</sub> max.	I <sub>D</sub>
STB23NM50N	550 V	< 0.19 $\Omega$	17 A
STF23NM50N			
STP23NM50N			
STW23NM50N			

- 100% avalanche tested
- Low input capacitance and gate charge
- Low gate input resistance



## Application

Switching applications

## Description

These devices are made using the second generation of MDmesh™ technology. This revolutionary Power MOSFET associates a new vertical structure to the company's strip layout to yield one of the world's lowest on-resistance and gate charge. It is therefore suitable for the most demanding high efficiency converters.

Figure 1. Internal schematic diagram

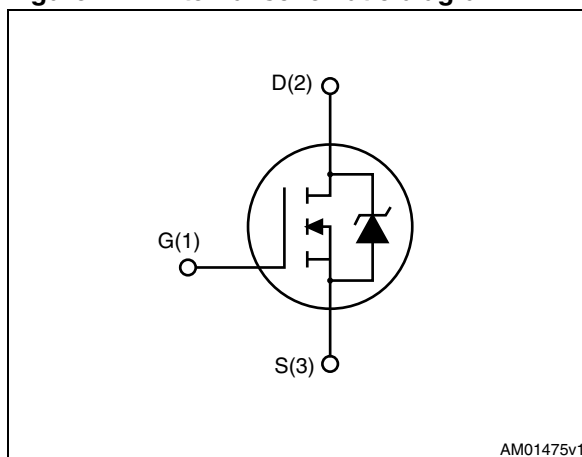


Table 1. Device summary

Order codes	Marking	Package	Packaging
STB23NM50N	23NM50N	D <sup>2</sup> PAK	Tape and reel
STF23NM50N		TO-220FP	Tube
STP23NM50N		TO-220	
STW23NM50N		TO-247	

# Contents

<b>1</b>	<b>Electrical ratings</b> .....	<b>3</b>
<b>2</b>	<b>Electrical characteristics</b> .....	<b>4</b>
2.1	Electrical characteristics (curves) .....	6
<b>3</b>	<b>Test circuits</b> .....	<b>9</b>
<b>4</b>	<b>Package mechanical data</b> .....	<b>10</b>
<b>5</b>	<b>Package mechanical data</b> .....	<b>15</b>
<b>6</b>	<b>Revision history</b> .....	<b>16</b>

# 1 Electrical ratings

**Table 2. Absolute maximum ratings**

Symbol	Parameter	Value			Unit
		TO-220, D <sup>2</sup> PAK	TO-247	TO-220FP	
V <sub>DS</sub>	Drain-source voltage (V <sub>GS</sub> = 0)	500			V
V <sub>GS</sub>	Gate- source voltage	± 25			V
I <sub>D</sub>	Drain current (continuous) at T <sub>C</sub> = 25 °C	17		17 <sup>(1)</sup>	A
I <sub>D</sub>	Drain current (continuous) at T <sub>C</sub> = 100 °C	11		11 <sup>(1)</sup>	A
I <sub>DM</sub> <sup>(2)</sup>	Drain current (pulsed)	68		68 <sup>(1)</sup>	A
P <sub>TOT</sub>	Total dissipation at T <sub>C</sub> = 25 °C	125		30	W
V <sub>ISO</sub>	Insulation withstand voltage (RMS) from all three leads to external heat sink (t=1 s; T <sub>C</sub> =25 °C)			2500	V
dv/dt <sup>(3)</sup>	Peak diode recovery voltage slope	15			V/ns
T <sub>stg</sub>	Storage temperature	-55 to 150			°C
T <sub>j</sub>	Max. operating junction temperature	150			°C

- Limited only by maximum temperature allowed
- Pulse width limited by safe operating area
- I<sub>SD</sub> ≤ 17 A, di/dt ≤ 400 A/μs, V<sub>DS peak</sub> ≤ V<sub>(BR)DSS</sub>, V<sub>DD</sub> = 80% V<sub>(BR)DSS</sub>

**Table 3. Thermal data**

Symbol	Parameter	Value				Unit
		D <sup>2</sup> PAK	TO-247	TO-220	TO-220FP	
R <sub>thj-case</sub>	Thermal resistance junction-case max	1			4.17	°C/W
R <sub>thj-pcb</sub> <sup>(1)</sup>	Thermal resistance junction-pcb minimum footprint	30				°C/W
R <sub>thj-amb</sub>	Thermal resistance junction-ambient max		62.5	50	62.5	°C/W
T <sub>l</sub>	Maximum lead temperature for soldering purpose		300			°C

- When mounted on 1inch<sup>2</sup> FR-4 board, 2 oz Cu

**Table 4. Avalanche characteristics**

Symbol	Parameter	Value	Unit
I <sub>AR</sub>	Avalanche current, repetitive or not-repetitive (pulse width limited by T <sub>j</sub> Max)	6	A
E <sub>AS</sub>	Single pulse avalanche energy (starting T <sub>j</sub> = 25 °C, I <sub>D</sub> = I <sub>AR</sub> , V <sub>DD</sub> = 50 V)	254	mJ

## 2 Electrical characteristics

( $T_{CASE}=25\text{ }^{\circ}\text{C}$  unless otherwise specified)

**Table 5. On/off states**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 1\text{ mA}$ , $V_{GS} = 0$	500			V
$I_{DSS}$	Zero gate voltage drain current ( $V_{GS} = 0$ )	$V_{DS} = \text{max rating}$ $V_{DS} = \text{max rating}$ , @125 °C			1 100	$\mu\text{A}$ $\mu\text{A}$
$I_{GSS}$	Gate-body leakage current ( $V_{DS} = 0$ )	$V_{GS} = \pm 25\text{ V}$			100	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$ , $I_D = 250\text{ }\mu\text{A}$	2	3	4	V
$R_{DS(on)}$	Static drain-source on resistance	$V_{GS} = 10\text{ V}$ , $I_D = 8.5\text{ A}$		0.162	0.19	$\Omega$

**Table 6. Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$C_{iss}$	Input capacitance	$V_{DS} = 50\text{ V}$ , $f = 1\text{ MHz}$ , $V_{GS} = 0$	-	1330	-	pF
$C_{oss}$	Output capacitance			84		pF
$C_{rss}$	Reverse transfer capacitance			4.8		pF
$C_{oss\text{ eq.}}^{(1)}$	Equivalent output capacitance	$V_{GS} = 0$ , $V_{DS} = 0\text{ to }400\text{ V}$	-	210	-	pF
$Q_g$	Total gate charge	$V_{DD} = 400\text{ V}$ , $I_D = 17\text{ A}$ , $V_{GS} = 10\text{ V}$ , <i>(see Figure 18)</i>	-	45	-	nC
$Q_{gs}$	Gate-source charge			7		nC
$Q_{gd}$	Gate-drain charge			24		nC
$R_g$	Gate input resistance	f=1 MHz Gate DC Bias=0 Test signal level=20 mV open drain	-	4.6	-	$\Omega$

1.  $C_{oss\text{ eq.}}$  is defined as a constant equivalent capacitance giving the same charging time as  $C_{oss}$  when  $V_{DS}$  increases from 0 to 80%  $V_{DS}$

**Table 7. Switching times**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 250\text{ V}$ , $I_D = 17\text{ A}$ $R_G = 4.7\ \Omega$ , $V_{GS} = 10\text{ V}$ (see Figure 17)	-	6.6	-	ns
$t_r$	Rise time			19		ns
$t_{d(off)}$	Turn-off-delay time			71		ns
$t_f$	Fall time			29		ns

**Table 8. Source drain diode**

Symbol	Parameter	Test conditions	Min	Typ.	Max	Unit
$I_{SD}$	Source-drain current		-		17	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)				68	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 17\text{ A}$ , $V_{GS} = 0$	-		1.5	V
$t_{rr}$	Reverse recovery time	$I_{SD} = 17\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = 60\text{ V}$ (see Figure 22)	-	286		ns
$Q_{rr}$	Reverse recovery charge			3700		nC
$I_{RRM}$	Reverse recovery current			26		A
$t_{rr}$	Reverse recovery time	$I_{SD} = 17\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = 60\text{ V}$ , $T_j = 150\text{ }^\circ\text{C}$ (see Figure 22)	-	350		ns
$Q_{rr}$	Reverse recovery charge			4800		nC
$I_{RRM}$	Reverse recovery current			27		A

1. Pulse width limited by safe operating area
2. Pulsed: pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5%

## 2.1 Electrical characteristics (curves)

Figure 2. Safe operating area for TO-220, D<sup>2</sup>PAK

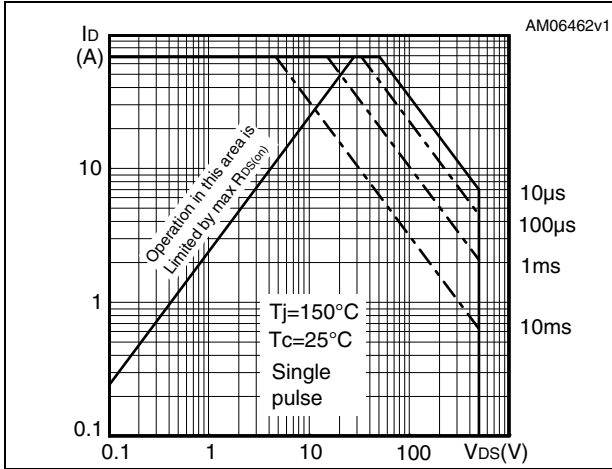


Figure 3. Thermal impedance for TO-220, D<sup>2</sup>PAK

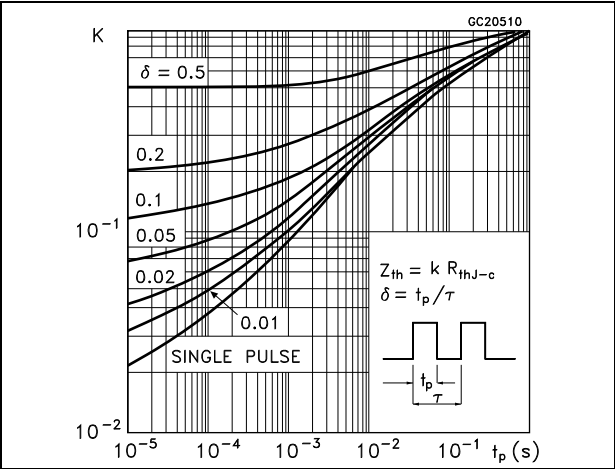


Figure 4. Safe operating area for TO-220FP

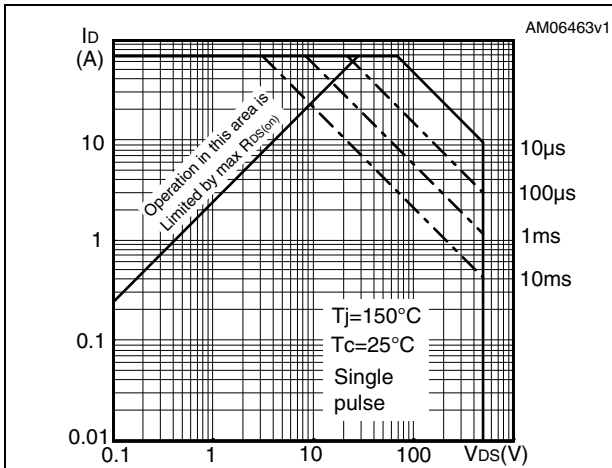


Figure 5. Thermal impedance for TO-220FP

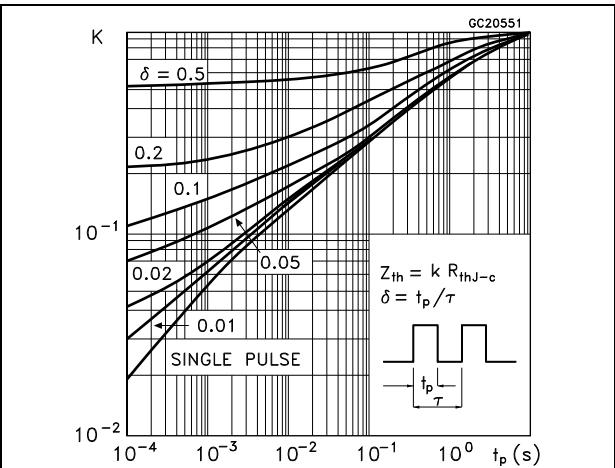


Figure 6. Safe operating area for TO-247

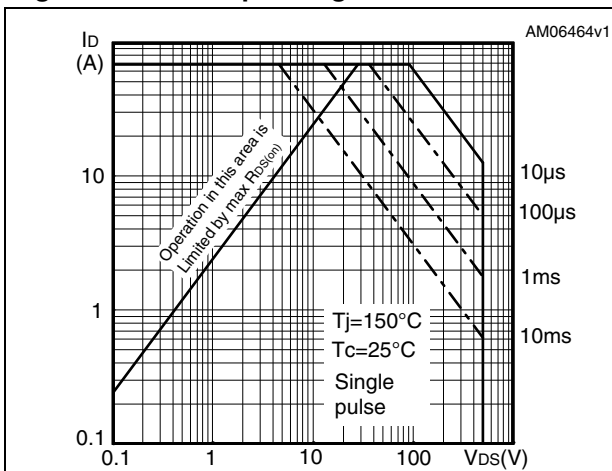


Figure 7. Thermal impedance for TO-247

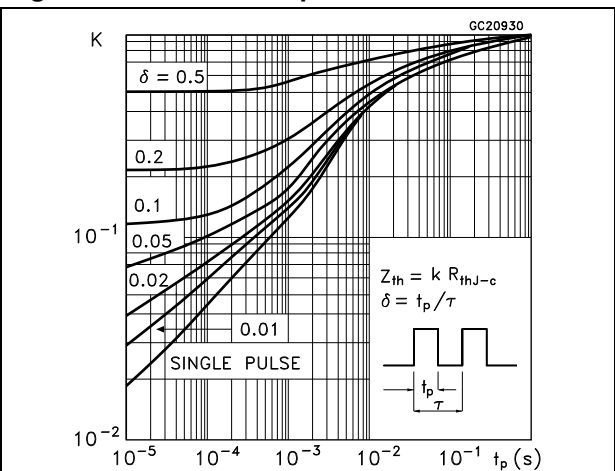


Figure 8. Output characteristics

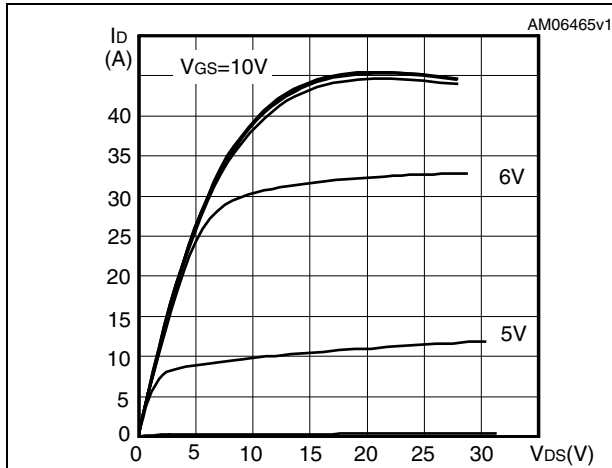


Figure 9. Transfer characteristics

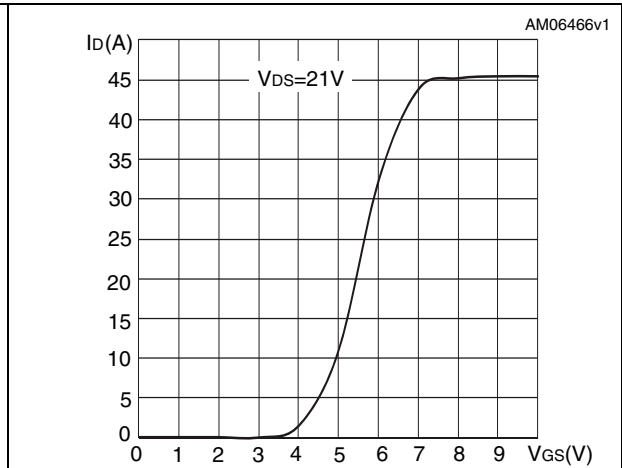


Figure 10. Normalized  $B_{V_{DSS}}$  vs temperature

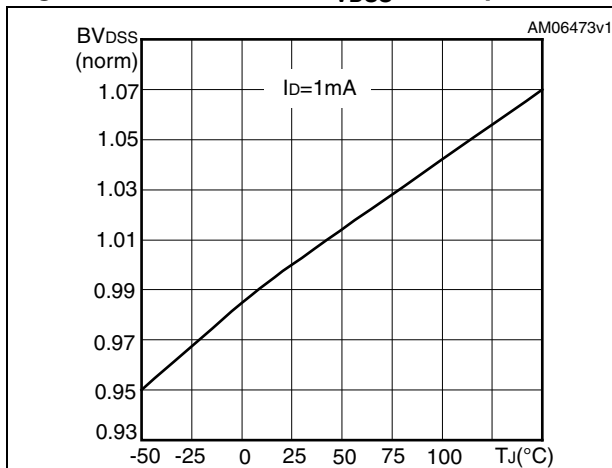


Figure 11. Static drain-source on resistance

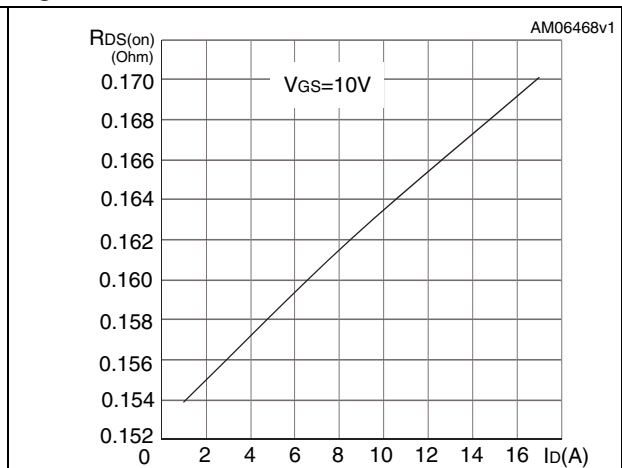


Figure 12. Gate charge vs gate-source voltage

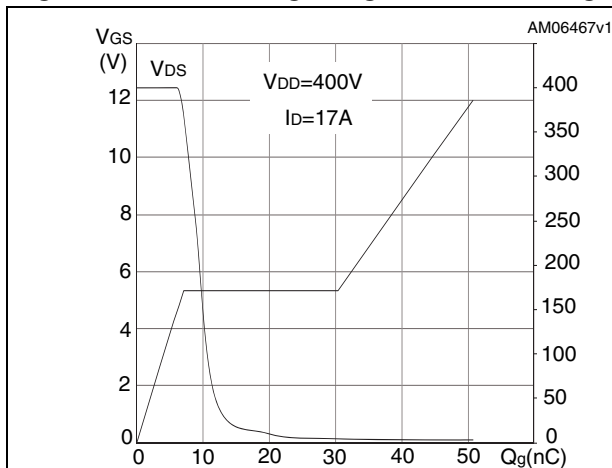


Figure 13. Capacitance variations

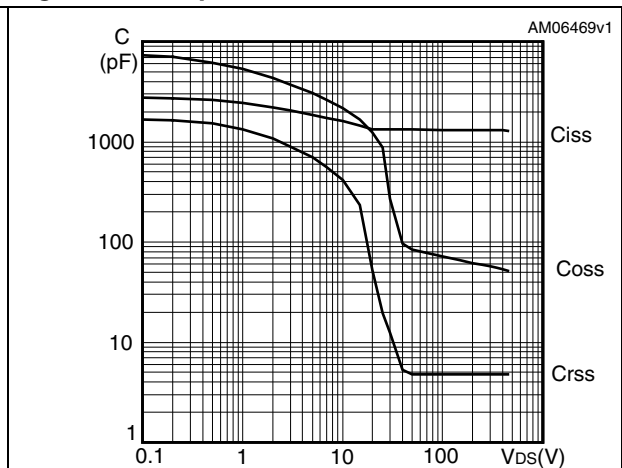


Figure 14. Normalized gate threshold voltage vs temperature

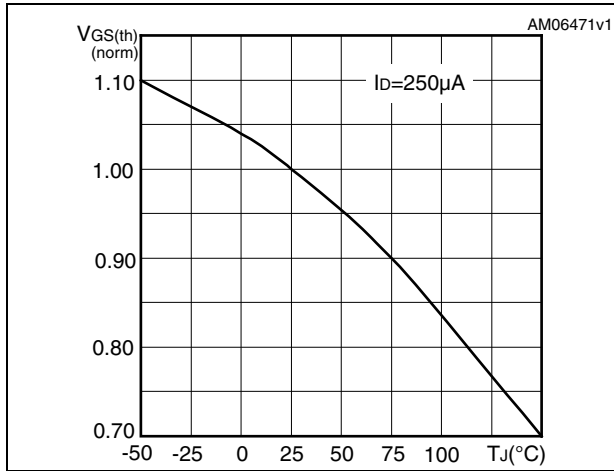


Figure 15. Normalized on resistance vs temperature

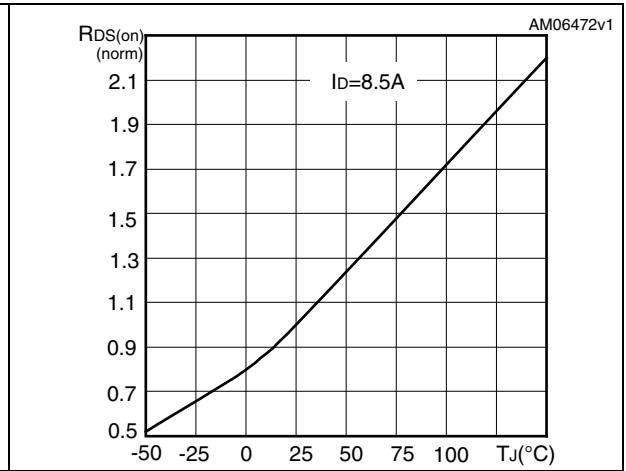
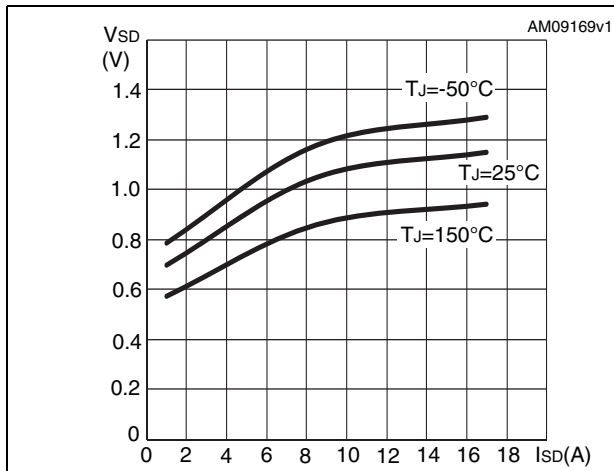


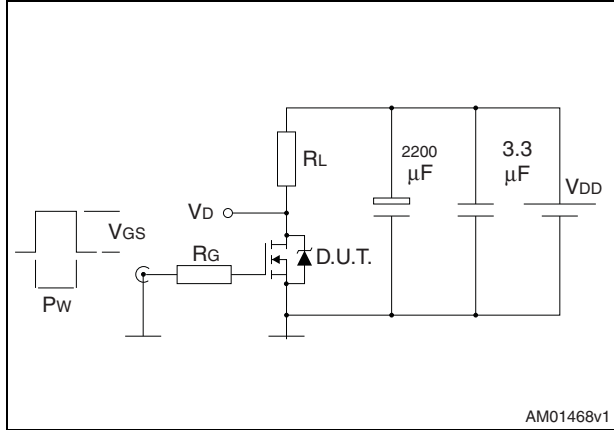
Figure 16. Source-drain diode forward characteristics





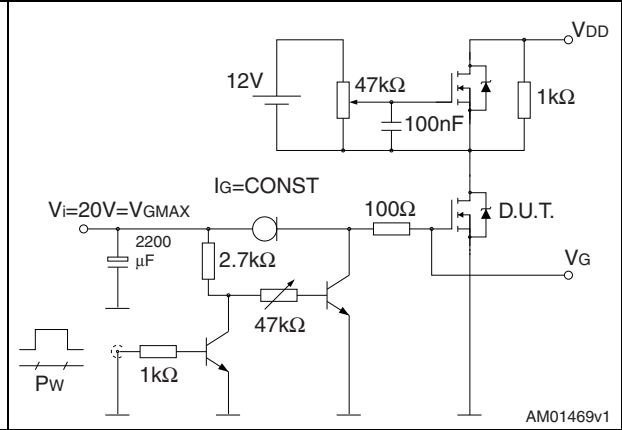
### 3 Test circuits

**Figure 17. Switching times test circuit for resistive load**



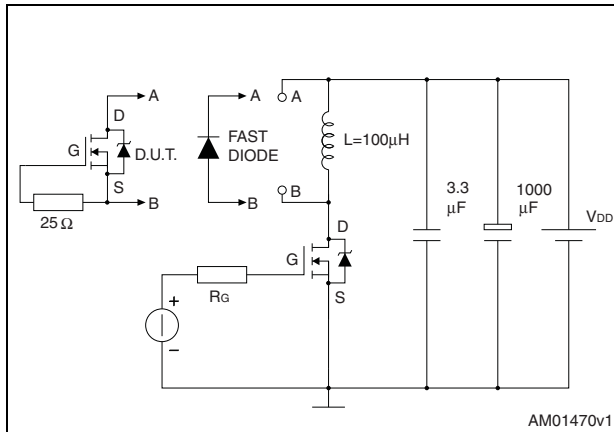
AM01468v1

**Figure 18. Gate charge test circuit**



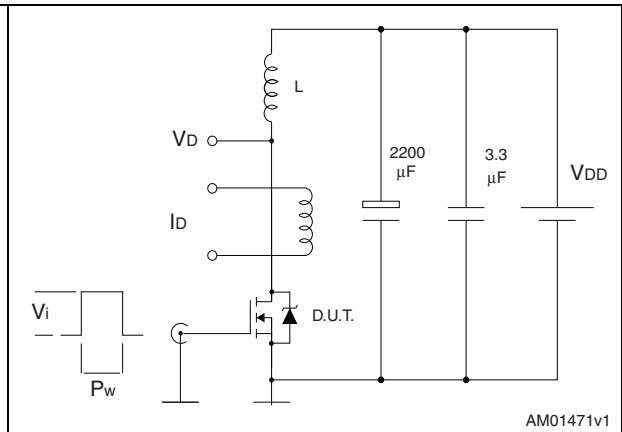
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**Figure 19. Test circuit for inductive load switching and diode recovery times**



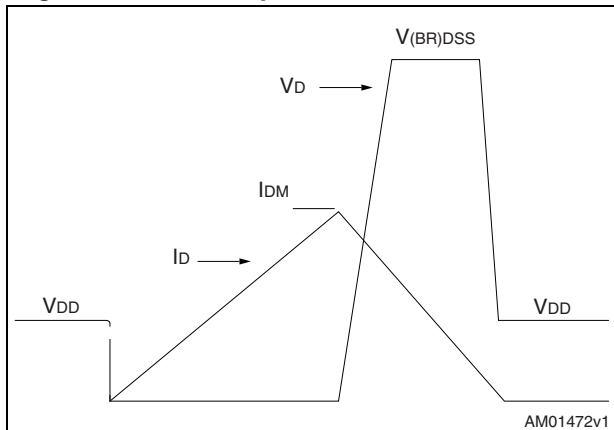
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**Figure 20. Unclamped inductive load test circuit**



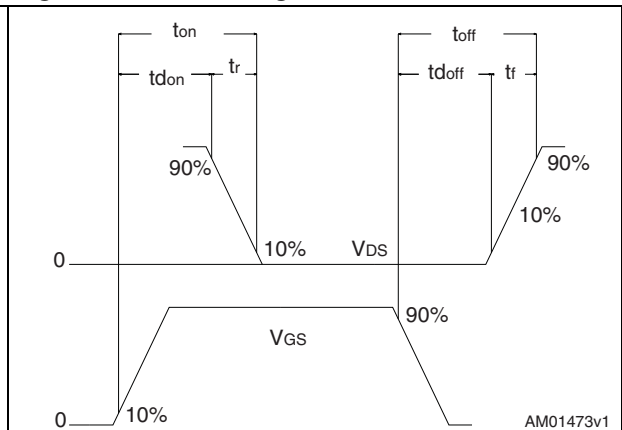
AM01471v1

**Figure 21. Unclamped inductive waveform**



AM01472v1

**Figure 22. Switching time waveform**



AM01473v1

## 4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK<sup>®</sup> packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK is an ST trademark.

Table 9. TO-220FP mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.4		4.6
B	2.5		2.7
D	2.5		2.75
E	0.45		0.7
F	0.75		1
F1	1.15		1.70
F2	1.15		1.70
G	4.95		5.2
G1	2.4		2.7
H	10		10.4
L2		16	
L3	28.6		30.6
L4	9.8		10.6
L5	2.9		3.6
L6	15.9		16.4
L7	9		9.3
Dia	3		3.2

Figure 23. TO-220FP drawing

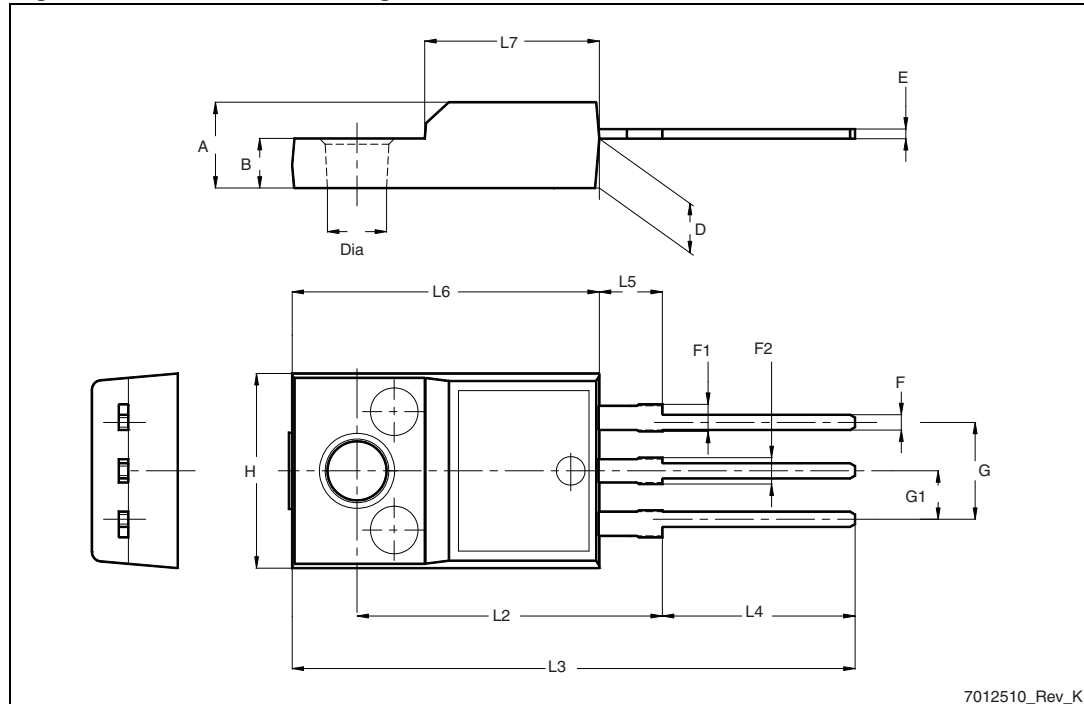
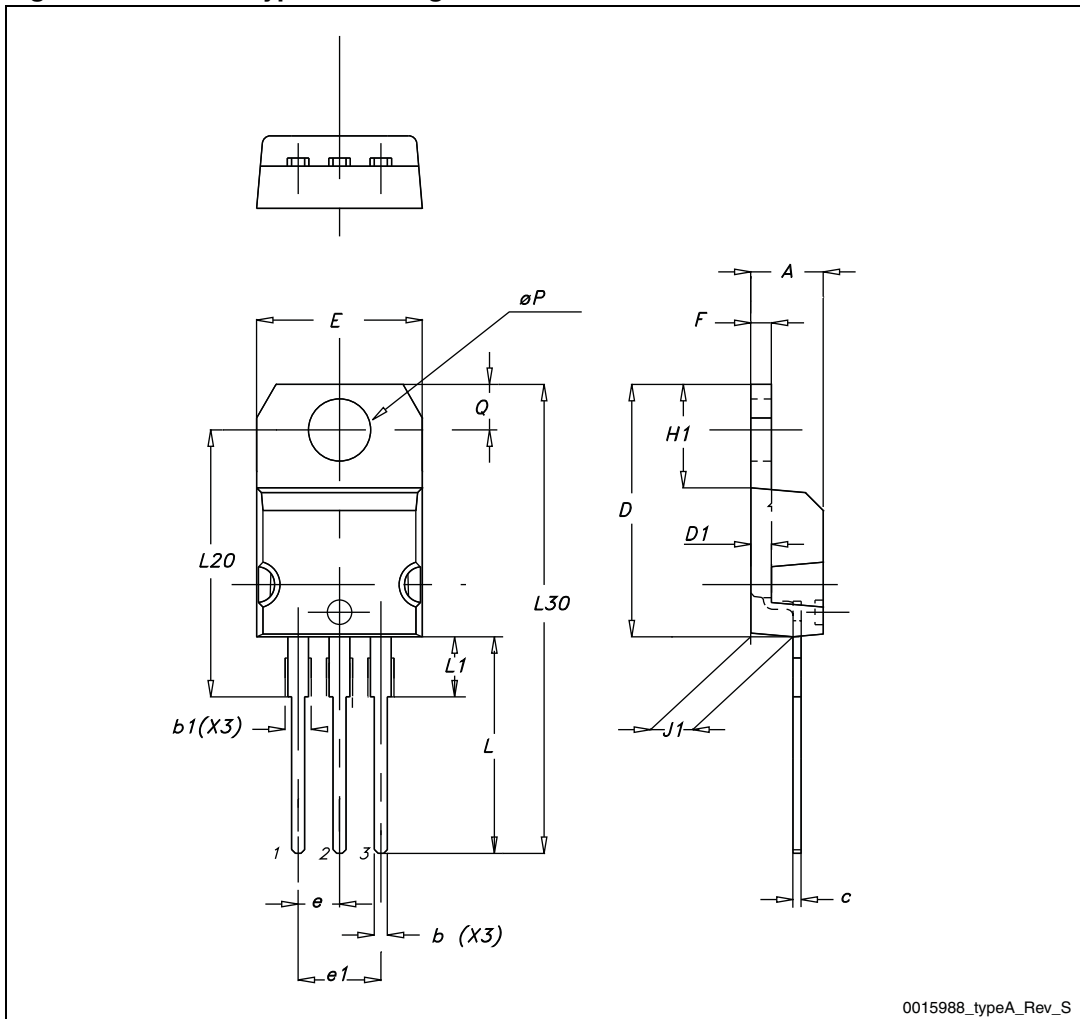


Table 10. TO-220 type A mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
b	0.61		0.88
b1	1.14		1.70
c	0.48		0.70
D	15.25		15.75
D1		1.27	
E	10		10.40
e	2.40		2.70
e1	4.95		5.15
F	1.23		1.32
H1	6.20		6.60
J1	2.40		2.72
L	13		14
L1	3.50		3.93
L20		16.40	
L30		28.90	
ØP	3.75		3.85
Q	2.65		2.95

Figure 24. TO-220 type A drawing



0015988\_typeA\_Rev\_S

Table 11. TO-247 mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.85		5.15
A1	2.20		2.60
b	1.0		1.40
b1	2.0		2.40
b2	3.0		3.40
c	0.40		0.80
D	19.85		20.15
E	15.45		15.75
e		5.45	
L	14.20		14.80
L1	3.70		4.30
L2		18.50	
ØP	3.55		3.65
ØR	4.50		5.50
S		5.50	

Figure 25. TO-247 drawing

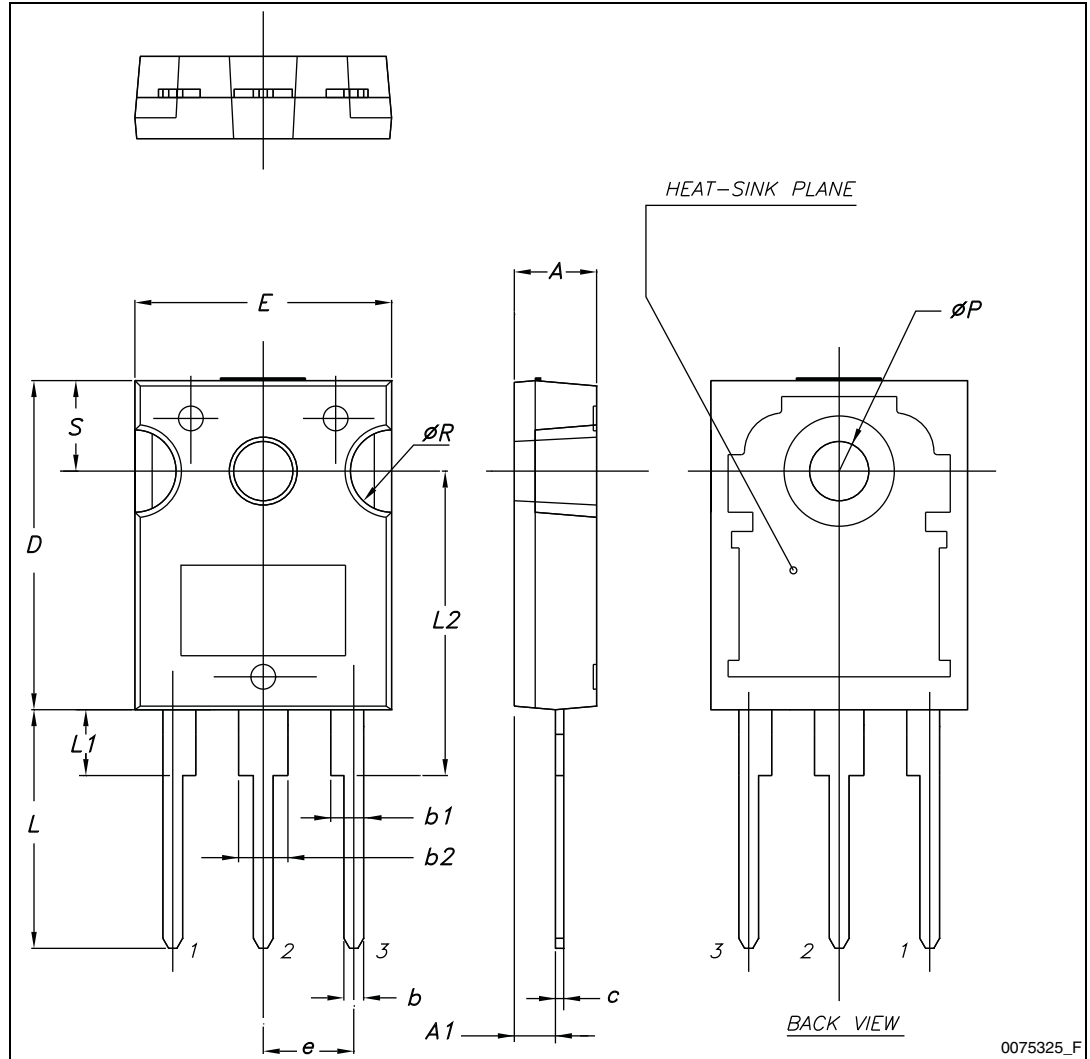


Table 12. D<sup>2</sup>PAK (TO-263) mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
A1	0.03		0.23
b	0.70		0.93
b2	1.14		1.70
c	0.45		0.60
c2	1.23		1.36
D	8.95		9.35
D1	7.50		
E	10		10.40
E1	8.50		
e		2.54	
e1	4.88		5.28
H	15		15.85
J1	2.49		2.69
L	2.29		2.79
L1	1.27		1.40
L2	1.30		1.75
R		0.4	
V2	0°		8°



Figure 26. D<sup>2</sup>PAK footprint<sup>(a)</sup>

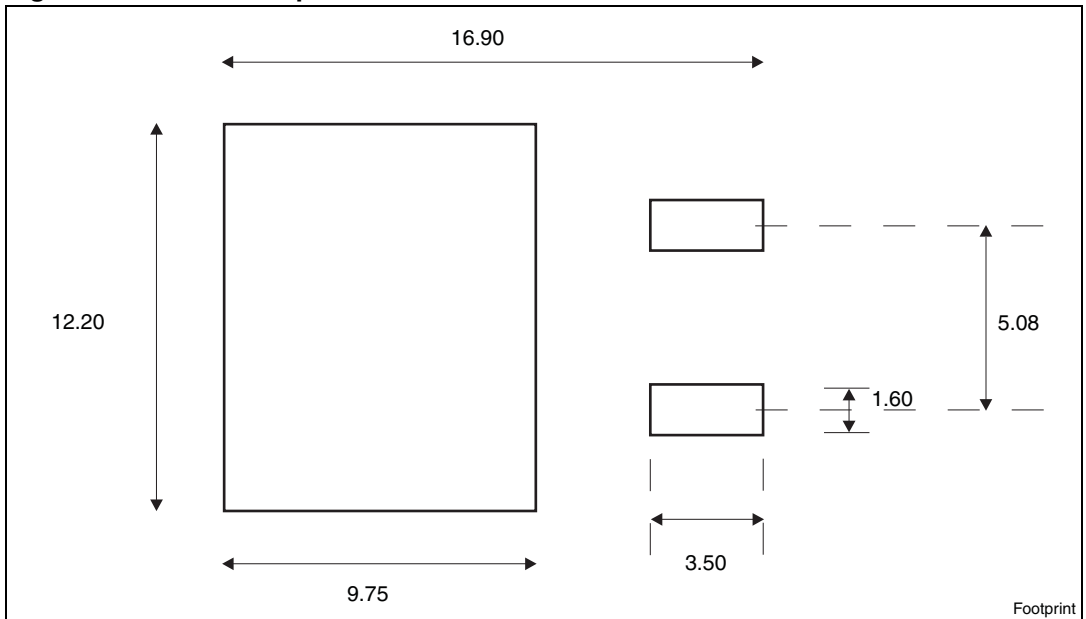
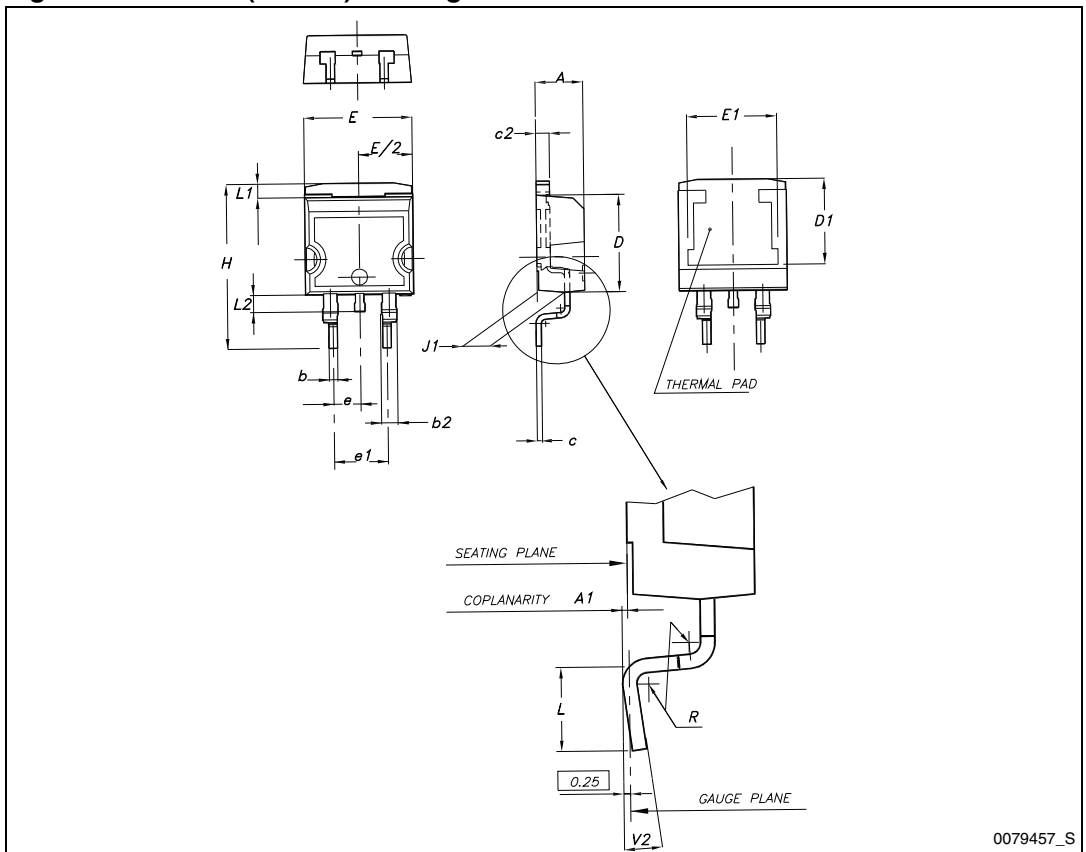


Figure 27. D<sup>2</sup>PAK (TO-263) drawing



a. All dimension are in millimeters

## 5 Package mechanical data

Table 13. D<sup>2</sup>PAK (TO-263) tape and reel mechanical data

Tape			Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.		Min.	Max.
A0	10.5	10.7	A		330
B0	15.7	15.9	B	1.5	
D	1.5	1.6	C	12.8	13.2
D1	1.59	1.61	D	20.2	
E	1.65	1.85	G	24.4	26.4
F	11.4	11.6	N	100	
K0	4.8	5.0	T		30.4
P0	3.9	4.1			
P1	11.9	12.1		Base qty	1000
P2	1.9	2.1		Bulk qty	1000
R	50				
T	0.25	0.35			
W	23.7	24.3			

Figure 28. Tape

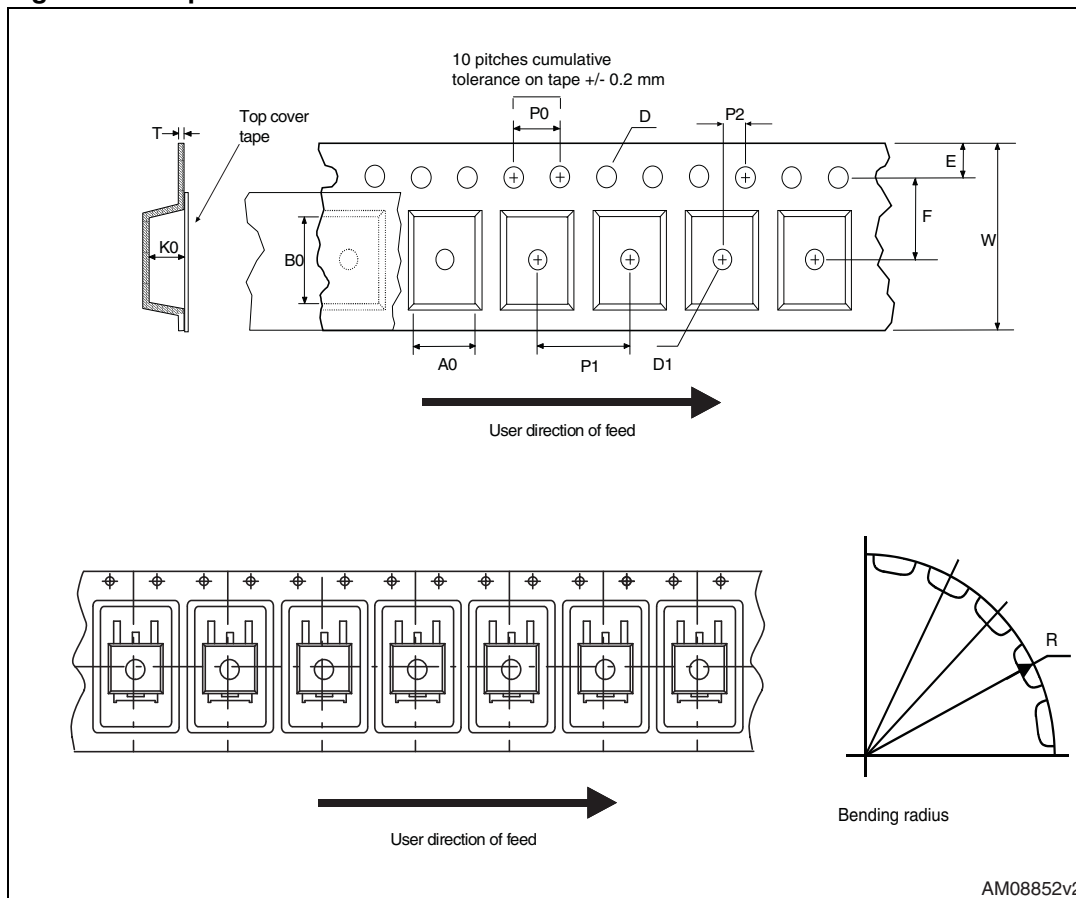
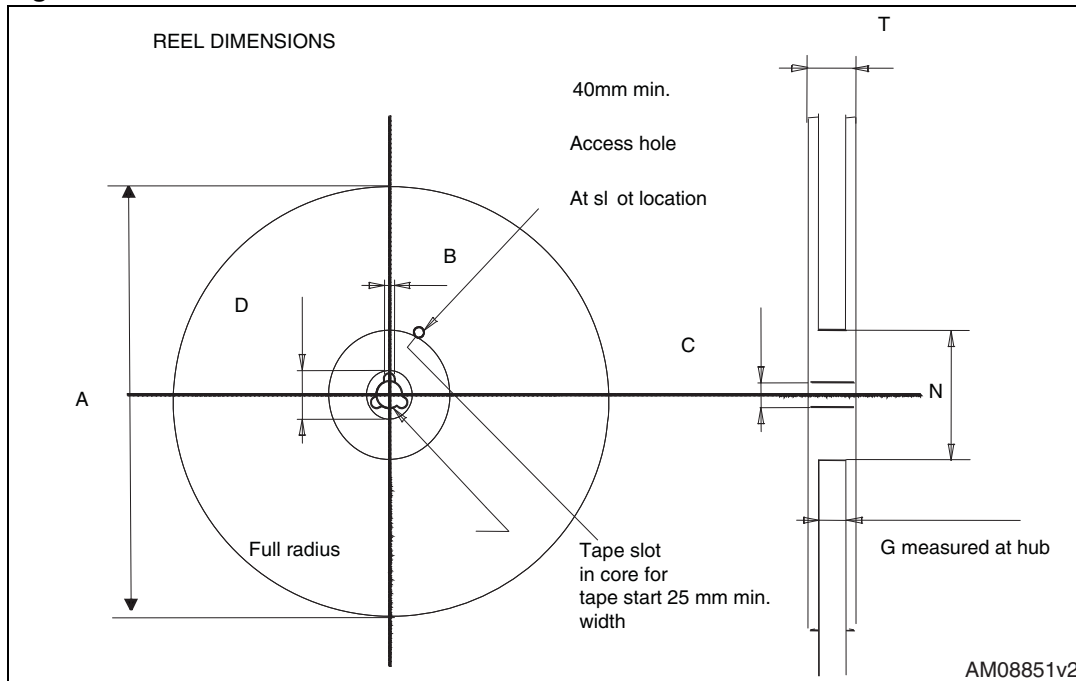


Figure 29. Reel



## 6 Revision history

Table 14. Document revision history

Date	Revision	Changes
11-Dec-2009	1	First release.
26-May-2010	2	Document status promoted from preliminary data to datasheet.
16-Sep-2010	3	Added new value in <i>Figure 14</i> , <i>Figure 15</i> and <i>Figure 10</i> .
23-May-2011	4	<i>Section 2.1: Electrical characteristics (curves)</i> has been updated.

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Нашей специализацией является поставка электронной компонентной базы двойного назначения, продукции таких производителей как XILINX, Intel (ex.ALTERA), Vicor, Microchip, Texas Instruments, Analog Devices, Mini-Circuits, Amphenol, Glenair.

Сотрудничество с глобальными дистрибьюторами электронных компонентов, предоставляет возможность заказывать и получать с международных складов практически любой перечень компонентов в оптимальные для Вас сроки.

На всех этапах разработки и производства наши партнеры могут получить квалифицированную поддержку опытных инженеров.

Система менеджмента качества компании отвечает требованиям в соответствии с ГОСТ Р ИСО 9001, ГОСТ РВ 0015-002 и ЭС РД 009

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