$\frac{\text{MOSFET}}{\text{SUPERFET}^{\text{®}}} - \text{Power, N-Channel,} \\ \text{SUPERFET}^{\text{®}} \text{ III, Easy Drive,} \\ \text{650 V, 17 A, 190 m} \\ \Omega$

Description

SUPERFET III MOSFET is ON Semiconductor's brand-new high voltage super-junction (SJ) MOSFET family that is utilizing charge balance technology for outstanding low on-resistance and lower gate charge performance. This advanced technology is tailored to minimize conduction loss, provide superior switching performance, and withstand extreme dv/dt rate. Consequently, SUPERFET III MOSFET Easy drive series helps manage EMI issues and allows for easier design implementation.

Features

- 700 V @ $T_J = 150$ °C
- Typ. $R_{DS(on)} = 159 \text{ m}\Omega$
- Ultra Low Gate Charge (Typ. Q_g = 33 nC)
- Low Effective Output Capacitance (Typ. C_{oss(eff.)} = 300 pF)
- 100% Avalanche Tested
- These Devices are Pb–Free, Halogen Free/BFR Free and are RoHS Compliant

Applications

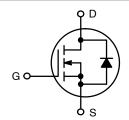
- Computing / Display Power Supplies
- Telecom / Server Power Supplies
- Industrial Power Supplies
- Lighting / Charger / Adapter



ON Semiconductor®

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V _{DSS}	R _{DS(ON)} MAX	I _D MAX
650 V	190 mΩ @ 10 V	17 A



POWER MOSFET



MARKING DIAGRAM

FCHD190 N65S3R0 AYWWG

FCHD190N65S3R0 = Specific Device Code

A = Assembly Location

Y = Year WW = Work Week G = Pb-Free Package

ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

ABSOLUTE MAXIMUM RATINGS (T_C = 25°C, Unless otherwise specified)

Symbol	Parameter		Value	Unit
V_{DSS}	Drain to Source Voltage		650	V
V_{GSS}	Gate to Source Voltage	DC	±30	V
		AC (f > 1 Hz)	±30	V
I _D	Drain Current	Continuous (T _C = 25°C)	17	Α
		Continuous (T _C = 100°C)	11	
I _{DM}	Drain Current	Pulsed (Note 1)	42.5	Α
E _{AS}	Single Pulsed Avalanche Energy (Note 2)		76	mJ
I _{AS}	Avalanche Current (Note 1)		2.5	Α
E _{AR}	Repetitive Avalanche Energy (Note 1)		1.44	mJ
dv/dt	MOSFET dv/dt		100	V/ns
	Peak Diode Recovery dv/dt (Note 3)		20	
P_{D}	Power Dissipation	(T _C = 25°C)	144	W
		Derate Above 25°C	1.15	W/°C
T _J , T _{STG}	Operating and Storage Temperature Range		-55 to +150	°C
TL	Maximum Lead Temperature for Soldering, 1/8" from Case for 5 s		300	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected. 1. Repetitive rating: pulse-width limited by maximum junction temperature. 2. $I_{AS} = 2.5 \text{ A}$, $R_{G} = 25 \Omega$, starting $T_{J} = 25^{\circ}\text{C}$. 3. $I_{SD} \le 8.5 \text{ A}$, di/dt $\le 200 \text{ A}/\mu\text{s}$, $V_{DD} \le 400 \text{ V}$, starting $T_{J} = 25^{\circ}\text{C}$.

THERMAL CHARACTERISTICS

Symbol	Parameter	Value	Unit
$R_{ hetaJC}$	Thermal Resistance, Junction to Case, Max.	0.87	°C/W
$R_{ heta JA}$	Thermal Resistance, Junction to Ambient, Max.	40	

PACKAGE MARKING AND ORDERING INFORMATION

Part Number	Top Marking	Package	Packing Method	Reel Size	Tape Width	Quantity
FCHD190N65S3R0-F155	FCHD190N65S3R0	TO-247AD	Tube	N/A	N/A	30 Units

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Тур	Max	Unit
OFF CHARACT	ERISTICS	•	•	•	•	•
BV _{DSS}	Drain to Source Breakdown Voltage	V _{GS} = 0 V, I _D = 1 mA, T _J = 25°C	650			V
		V _{GS} = 0 V, I _D = 1 mA, T _J = 150°C	700			V
$\Delta BV_{DSS}/\Delta T_{J}$	Breakdown Voltage Temperature Coefficient	I _D = 1 mA, Referenced to 25°C		0.6		V/°C
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} = 650 V, V _{GS} = 0 V			1	μΑ
		V _{DS} = 520 V, T _C = 125°C		0.89		
I _{GSS}	Gate to Body Leakage Current	V _{GS} = ±30 V, V _{DS} = 0 V			±100	nA
ON CHARACTE	RISTICS					
V _{GS(th)}	Gate Threshold Voltage	$V_{GS} = V_{DS}, I_D = 0.39 \text{ mA}$	2.5		4.5	V
R _{DS(on)}	Static Drain to Source On Resistance	V _{GS} = 10 V, I _D = 8.5 A		159	190	mΩ
9FS	Forward Transconductance	V _{DS} = 20 V, I _D = 8.5 A		10		S
YNAMIC CHA	RACTERISTICS	•				
C _{iss}	Input Capacitance	V _{DS} = 400 V, V _{GS} = 0 V, f = 1 MHz		1350		pF
C _{oss}	Output Capacitance			30		pF
C _{oss(eff.)}	Effective Output Capacitance	V _{DS} = 0 V to 400 V, V _{GS} = 0 V		300		pF
C _{oss(er.)}	Energy Related Output Capacitance	V _{DS} = 0 V to 400 V, V _{GS} = 0 V		43		pF
Q _{g(tot)}	Total Gate Charge at 10 V	$V_{DS} = 400 \text{ V}, I_D = 8.5 \text{ A},$		33		nC
Q _{gs}	Gate to Source Gate Charge	V _{GS} = 10 V (Note 4)		7.9		nC
Q _{gd}	Gate to Drain "Miller" Charge			14		nC
ESR	Equivalent Series Resistance	f = 1 MHz		0.5		Ω
WITCHING CH	IARACTERISTICS					
t _{d(on)}	Turn-On Delay Time	$V_{DD} = 400 \text{ V}, I_D = 8.5 \text{ A},$		17		ns
t _r	Turn-On Rise Time	$V_{GS} = 10 \text{ V}, R_g = 4.7 \Omega$ (Note 4)		16		ns
t _{d(off)}	Turn-Off Delay Time			42		ns
t _f	Turn-Off Fall Time			6		ns
OURCE-DRAI	N DIODE CHARACTERISTICS			-	•	-
I _S	Maximum Continuous Source to Drain Diod	e Forward Current			17	Α
I _{SM}	Maximum Pulsed Source to Drain Diode Fo	rward Current			42.5	Α
V _{SD}	Source to Drain Diode Forward Voltage	V _{GS} = 0 V, I _{SD} = 8.5 A			1.2	V
t _{rr}	Reverse Recovery Time	V _{DD} = 400 V, I _{SD} = 8.5 A,		313		ns
Q _{rr}	Reverse Recovery Charge	dl _F /dt = 100 A/μs		4.9		μС

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Essentially independent of operating temperature typical characteristics.

TYPICAL PERFORMANCE CHARACTERISTICS

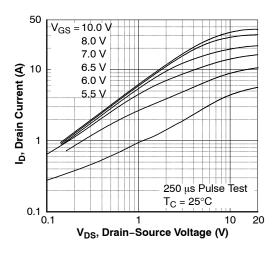


Figure 1. On-Region Characteristics

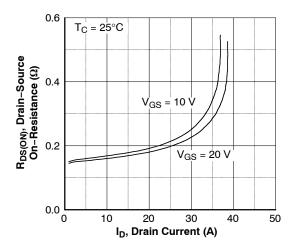


Figure 3. On-Resistance Variation vs.
Drain Current and Gate Voltage

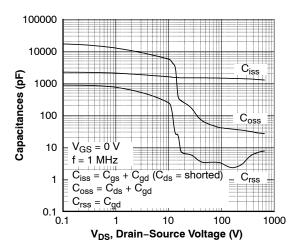


Figure 5. Capacitance Characteristics

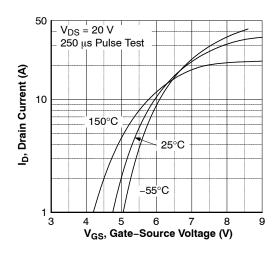


Figure 2. Transfer Characteristics

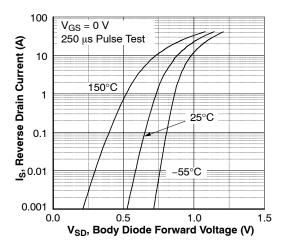


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

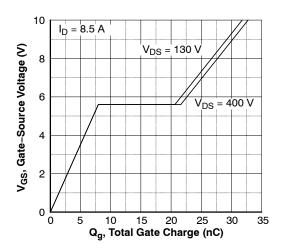


Figure 6. Gate Charge Characteristics

TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

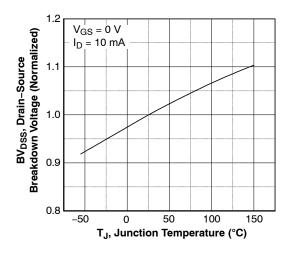


Figure 7. Breakdown Voltage Variation vs. Temperature

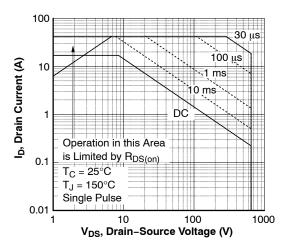


Figure 9. Maximum Safe Operating Area

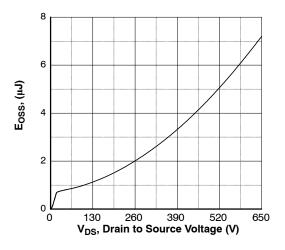


Figure 11. $E_{\mbox{OSS}}$ vs. Drain to Source Voltage

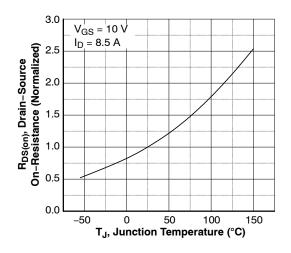


Figure 8. On–Resistance Variation vs. Temperature

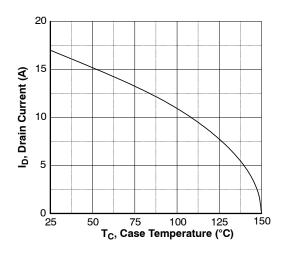


Figure 10. Maximum Drain Current vs. Case Temperature

TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

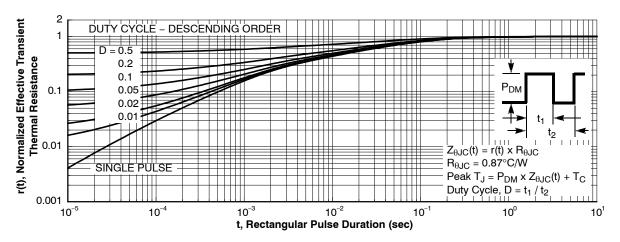


Figure 12. Transient Thermal Response Curve

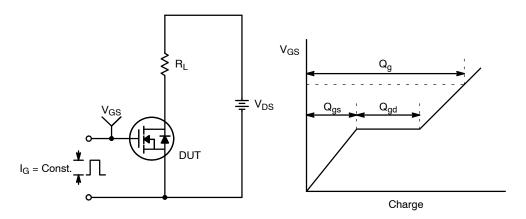


Figure 13. Gate Charge Test Circuit & Waveform

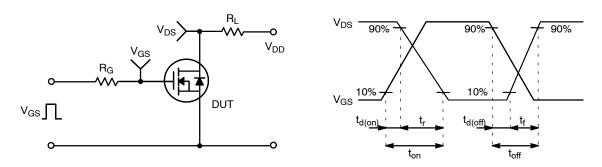


Figure 14. Resistive Switching Test Circuit & Waveforms

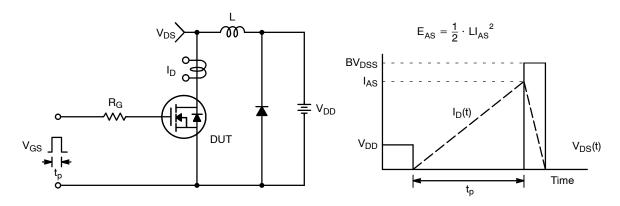


Figure 15. Unclamped Inductive Switching Test Circuit & Waveforms

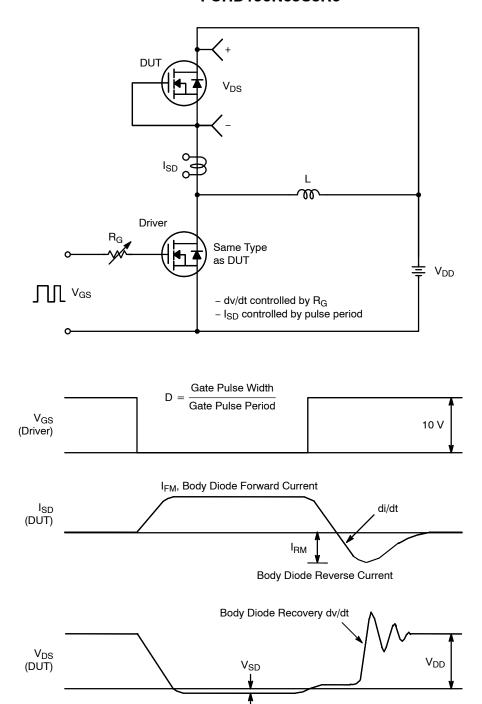
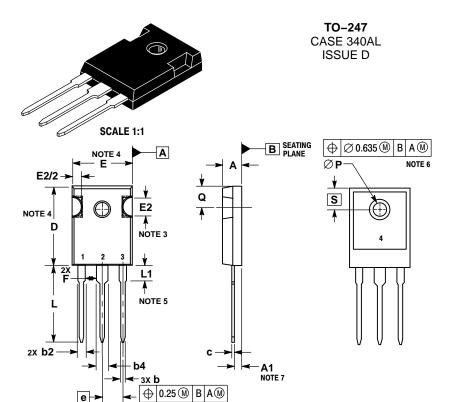


Figure 16. Peak Diode Recovery dv/dt Test Circuit & Waveforms

Body Diode Forward Voltage Drop



DATE 17 MAR 2017

- NOTES:

 1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.

 2. CONTROLLING DIMENSION: MILLIMETERS.

 3. SLOT REQUIRED, NOTCH MAY BE ROUNDED.

 - SLOT HEQUITED, NOTCH MAY BE HOUNDED.

 DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH.

 MOLD FLASH SHALL NOT EXCEED 0.13 PER SIDE. THESE

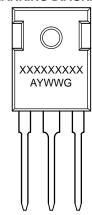
 DIMENSIONS ARE MEASURED AT THE OUTERMOST

 EXTREME OF THE PLASTIC BODY.
- 5. LEAD FINISH IS UNCONTROLLED IN THE REGION DEFINED BY L1.
- ©P SHALL HAVE A MAXIMUM DRAFT ANGLE OF 1.5° TO THE TOP OF THE PART WITH A MAXIMUM DIAMETER OF 3.91.

 DIMENSION A1 TO BE MEASURED IN THE REGION DEFINED

	MILLIMETERS		
DIM	MIN	MAX	
Α	4.70	5.30	
A1	2.20	2.60	
b	1.07	1.33	
b2	1.65	2.35	
b4	2.60	3.40	
С	0.45	0.68	
D	20.80	21.34	
Е	15.50	16.25	
E2	4.32	5.49	
е	5.45	BSC	
F	2.655		
L	19.80	20.80	
L1	3.81	4.32	
P	3.55	3.65	
Q	5.40	6.20	
S	6.15 BSC		

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code = Assembly Location

Υ = Year WW = Work Week G = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot " ■", may or may not be present.

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PAGE 2 OF 2

ISSUE	REVISION	DATE
0	RELEASED TO PRODUCTION. REQ. BY D. TRUHITTE.	26 JUN 2013
Α	REMOVED DIMENSION A2. REQ. BY S. BRUTCHER.	01 AUG 2013
В	MODIFED DIMENSIONS D AND L1. REQ. BY C. ENRIQUEZ.	08 MAR 2016
С	ADDED DIMENSION F. REQ. BY C. ENRIQUEZ.	30 NOV 2016
D	MODIFED DIMENSIONS b AND c. REQ. BY C. ENRIQUEZ.	17 MAR 2017

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