ISL24202

Programmable VCOM Calibrator with EEPROM

FN7587
Rev 0.00
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The ISL24202 is an 8-bit programmable current sink that can be used in conjunction with an external voltage divider to generate a voltage source (V_{COM}) positioned between the analog supply voltage and ground. The current sink's full-scale range is controlled by an external resistor, R_{SET}. With the appropriate choice of external resistors R_1 and R_2, the V_{COM} voltage range can be controlled between any arbitrary voltage range. The ISL24202 has an 8-bit data register and 8-bit EEPROM for storing both a volatile and a permanent value for its output, accessible through a single up/down counter interface pin (CTL). After the part is programmed with the desired V_{COM} value, the Counter Enable pin (CE) can be grounded to prevent further changes. On every power-up the EEPROM contents are automatically transferred to the data register, and the pre-programmed output voltage appears at the V_{OUT} pin.

The ISL24202 can be used with a high output drive buffer amplifier, which allows it to directly drive the V_{COM} input of an LCD panel.

The ISL24202 is available in an 8 Ld 3mm x 3mm TDFN package. This package has a maximum height of 0.8mm for very low profile designs. The ambient operating temperature range is
-40°C to +85°C.

Features

- Adjustable 8-Bit, 256-Step, Current Sink Output
- On-Chip 8-Bit EEPROM
- Up/Down Counter Interface
- Guaranteed Monotonic Over-Temperature
- 4.5V to 19.0V Analog Supply Range for Normal Operation (10.8V Minimum Analog Supply Voltage for Programming)
- 2.25V to 3.6V Logic Supply Voltage Operating Range
- Pb-free (RoHS-Compliant)
- Ultra-Thin 8 Ld TDFN (3 x 3 x 0.8mm Max)

Applications

- LCD Panel V_{COM} Generator
- Electrophoretic Display V_{COM} Generator

Related Literature

- See AN1633 for ISL24202 Evaluation Board Application Note "ISL24202IRTZ-EVALZ Evaluation Board User Guide" (Coming Soon)

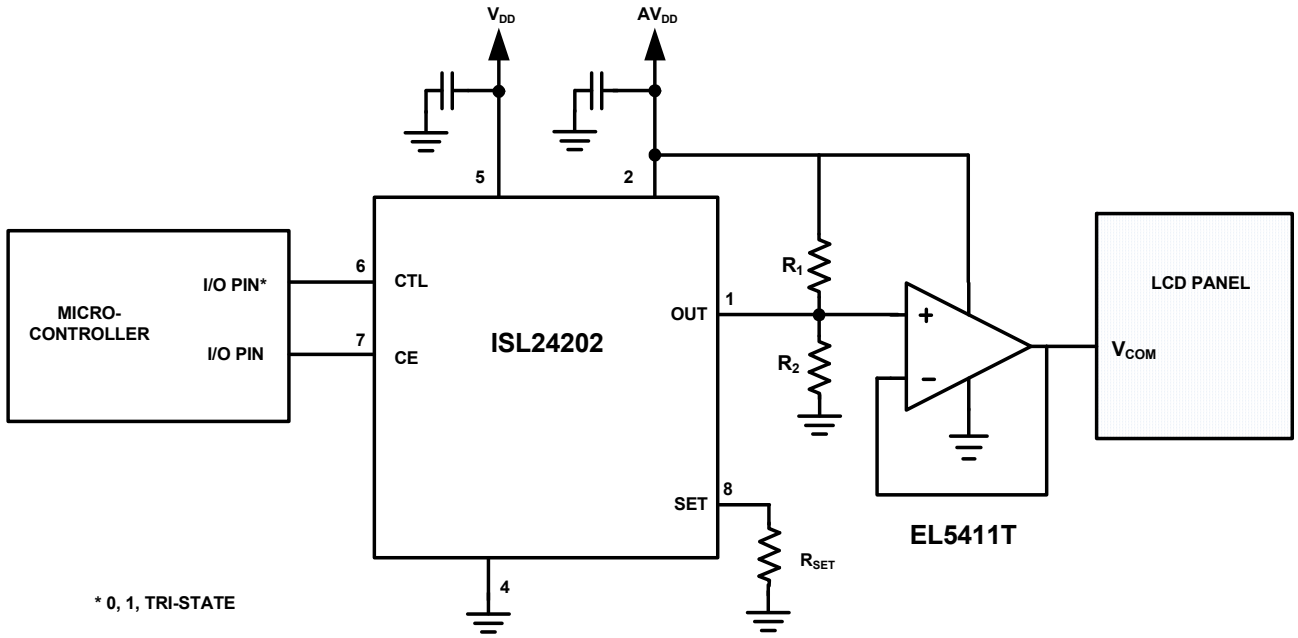


FIGURE 1. TYPICAL ISL24202 APPLICATION

Block Diagram

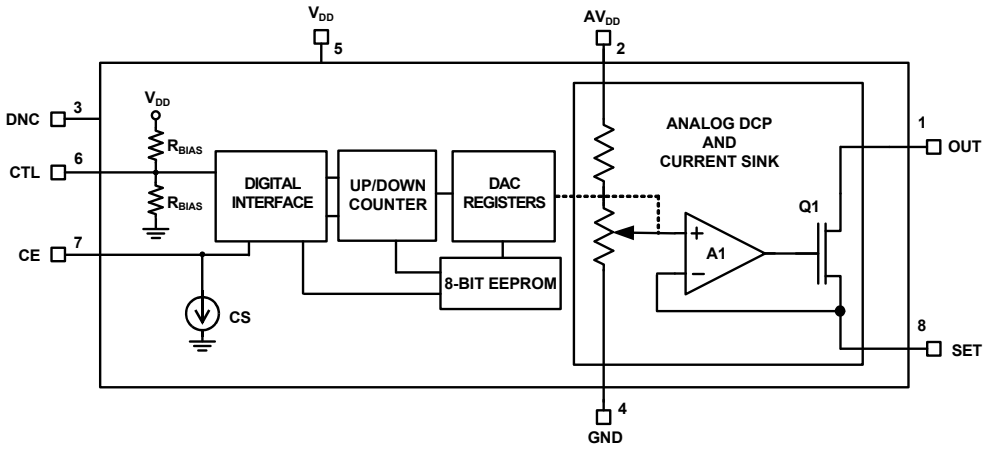


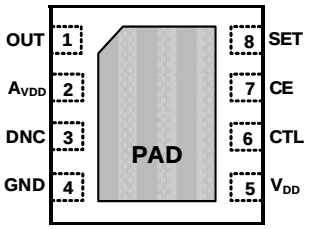
FIGURE 2. BLOCK DIAGRAM OF THE ISL24202

Pin Descriptions

PIN NAME	PIN #	FUNCTION
OUT	1	Adjustable Sink Current Output Pin. The sink current into the OUT pin is equal to the DAC setting times the maximum adjustable sink current divided by 256. See the "SET" pin function description below (pin 8) for setting the maximum adjustable sink current.
A_{VDD}	2	High-Voltage Analog Supply. Bypass to GND with 0.1µF capacitor.
DNC	3	Do Not Connect to external circuitry. It is acceptable to ground this pin.
GND	4	Ground connection.
V_{DD}	5	Digital power supply input. Bypass to GND with 0.1µF de-coupling capacitor.
CTL	6	Up/Down Control for internal counter and Internal EEPROM Programming Control Input. When CE is high: A low-to-mid transition increments the 8-bit counter, adding 1 to the DAC setting, increasing the OUT sink current, and lowering the divider voltage at the OUT pin. A high-to-mid transition decrements the 8-bit counter, subtracting 1 from the DAC setting, decreasing the OUT sink current, and increasing the divider voltage at the OUT pin. To program the EEPROM, take this pin to >4.9V (see "CTL EEPROM Programming Signal Time" in the "Electrical Specifications" table on page 5 for details). Float when not in use.
CE	7	Counter Enable Pin. Connect CE to V_{DD} to enable adjustment of the output sink current. Float or connect CE to GND to prevent further adjustment or programming (Note: the CE pin has an internal 500nA pull-down sink current). The EEPROM value will be copied to the register on a V_{OH} to V_{OL} transition.
SET	8	Maximum Sink Current Adjustment Pin. Connect a resistor from SET to GND to set the maximum adjustable sink current of the OUT pin. The maximum adjustable sink current is equal to (AV_{DD}/20) divided by R_{SET}.
PAD	-	Thermal pad should be connected to system ground plane to optimize thermal performance.

Pin Configuration

ISL24202
(8 LD TDFN)
TOP VIEW



(*CONNECT THERMAL PAD TO GND)

Ordering Information

PART NUMBER (Notes 1, 2, 3)	PART MARKING	INTERFACE	TEMP RANGE (°C)	PACKAGE (Pb-Free)	PKG. DWG. #
ISL24202IRTZ	202Z	COUNTER	-40 to +85	8 Ld 3x3 TDFN	L8.3x3A
ISL24202IRTZ-EVALZ	Evaluation Board				

NOTES:

1. Add “-T*” suffix for tape and reel. Please refer to TB347 for details on reel specifications.
2. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), please see device information page ISL24202. For more information on MSL please see techbrief TB363.

Absolute Maximum Ratings

Supply Voltage
- AV_{DD} to GND 20V
- V_{DD} to GND 4V

Input Voltage with respect to Ground
- SET, CTL ..... AV_{DD}+0.3V
- CE and WP ..... V_{DD}+0.3V

Output Voltage with respect to Ground
- OUT ..... AV_{DD}

Continuous Output Current
- OUT 5mA

ESD Ratings
- Human Body Model (Tested per JESD22-A114) 7kV
- Machine Model (Tested per JESD22-A115) 300V
- Charged Device Model (Tested per JESD22-C101) 2kV

Latch Up (Tested per JESD 78, Class II, Level A) 100mA

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
8 Ld TDFN Package (Notes 4, 5)	53	11

Moisture Sensitivity (see Technical Brief TB363)
- All Packages ..... Level 1

Maximum Die Temperature ..... +150°C

Storage Temperature ..... -65°C to +150°C

Pb-free Reflow Profile ..... see link below
- http://www.intersil.com/pbfree/Pb-FreeReflow.asp

Recommended Operating Conditions

Operating Range
- AV_{DD} ..... 4.5V to 19V
- V_{DD} ..... 2.25V to 3.6V

Ambient Operating Temperature ..... -40°C to +85°C

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

4. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with "direct attach" features. See Tech Brief TB379.
5. For θ_{JC}, the "case temp" location is the center of the exposed metal pad on the package underside.

Electrical Specifications

Test Conditions: V_{DD} = 3.3V, AV_{DD} = 18V, R_{SET} = 5kΩ, R_1 = 10kΩ, R_2 = 10kΩ, (See Figure 5). Typicals are at T_A = +25°C. **Boldface limits apply over the operating temperature range, -40°C to +85°C.**

SYMBOL	PARAMETER	TEST CONDITIONS	MIN (Note 6)	TYP	MAX (Note 6)	UNITS
DC CHARACTERISTICS						
V_{DD}	V_{DD} Supply Range - Operating		**2.25**		**3.6**	V
AV_{DD}	AV_{DD} Supply Range Supporting EEPROM Programming		**10.8**		**19**	V
AV_{DD}	AV_{DD} Supply Range for Wide-Supply Operation without EEPROM Programming		**4.5**		**19**	V
I_{DD}	V_{DD} Supply Current	CTL = 0.5*V_{DD}		40	**65**	µA
I_{AVDD}	AV_{DD} Supply Current	CTL = 0.5*V_{DD}		24	**38**	µA
OUT PIN CHARACTERISTICS						
SET_{ZSE}	SET Zero-Scale Error				±3	LSB
SET_{FSE}	SET Full-Scale Error				±8	LSB
V_{OUT}	OUT Voltage Range		**V_{SET} + 1.75**		**AV_{DD}**	V
SET_{VD}	SET Voltage Drift			7		µV/°C
I_{OUT}	Maximum OUT Sink Current			4		mA
INL	Integral Non-Linearity				±2	LSB
DNL	Differential Non-Linearity				±1	LSB
EEPROM CHARACTERISTICS						
t_{PROG}	EEPROM Programming Time (internal)				100	ms
UP/DOWN COUNTER CONTROL INPUTS (SEE FIGURE 11)						
V_{IH}	CE and CTL Input Logic High Threshold		**0.7*V_{DD}**			V
V_{IL}	CE and CTL Input Logic Low Threshold				**0.3*V_{DD}**	V
I_{CS_PD}	CE Input Pull Down Current Sink			0.5	**1.5**	µA
I_{CTL}	CTL Input Bias Current	CTL = GND (sourcing)		7	**15**	µA
		CTL = V_{DD} (sinking)		7	**15**	µA
t_{ST}	CE to CTL Start Delay		**50**			µs
t_{READ}	EEPROM Recall Time (after CE de-asserted)				**10**	ms

Electrical Specifications Test Conditions: V_{DD} = 3.3V, AV_{DD} = 18V, R_{SET} = 5kΩ, R_1 = 10kΩ, R_2 = 10kΩ, (See Figure 5). Typicals are at T_A = +25°C. **Boldface limits apply over the operating temperature range, -40°C to +85°C. (Continued)**

SYMBOL	PARAMETER	TEST CONDITIONS	MIN (Note 6)	TYP	MAX (Note 6)	UNITS
t_{H_REJ}	CTL High Pulse Rejection Width				**20**	µs
t_{L_REJ}	CTL Low Pulse Rejection Width				**20**	µs
t_{H_MIN}	CTL High Minimum Valid Pulse Width		**200**			µs
t_{L_MIN}	CTL Low Minimum Valid Pulse Width		**200**			µs
t_{MTC}	CTL Minimum Time Between Counts		**10**			µs
V_{PROG}	CTL EEPROM Program Voltage (see Figure 9)		**4.9**		**19**	V
t_{PROG}	CTL EEPROM Programming Signal Time			200		µs
t_{H_PROP}	CTL High-to-Mid to OUT Propagation Time			65		µs
t_{L_PROP}	CTL Low-to-Mid to OUT Propagation Time			65		µs

NOTE:

6. Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.

Application Information

LCD panels have a V_{COM} (common voltage) that must be precisely set to minimize flicker. Figure 3 shows a typical V_{COM} adjustment circuit using a mechanical potentiometer, and the equivalent circuit replacement using the ISL24202. Having a digital counter interface enables automatic, digital flicker minimization during production test and alignment. After programming, the counter interface is not needed again - the ISL24202 automatically powers up with the correct V_{COM} voltage programmed previously.

The ISL24202 uses a digitally controllable potentiometer (DCP), with 256 steps of resolution (Figure 4) to change the current drawn at the OUT pin, which then changes the voltage created by the R_1 - R_2 resistor divider (Figure 5). The OUT voltage can then be buffered by an external amplifier (A2) to generate a buffered output voltage (V_{COM}) capable of driving the V_{COM} input of an LCD panel. The amount of current sunk is controlled by the setting of the DCP, which is recalled at power-up from the ISL24202's internal EEPROM. The EEPROM is typically programmed during panel manufacture. As noted in the "Electrical Specifications" section on page 4, the ISL24202 requires a minimum AV_{DD} voltage of 10.8V for EEPROM programming, but will work in normal operation down to 4.5V after the EEPROM has been programmed, with no additional EEPROM writing.

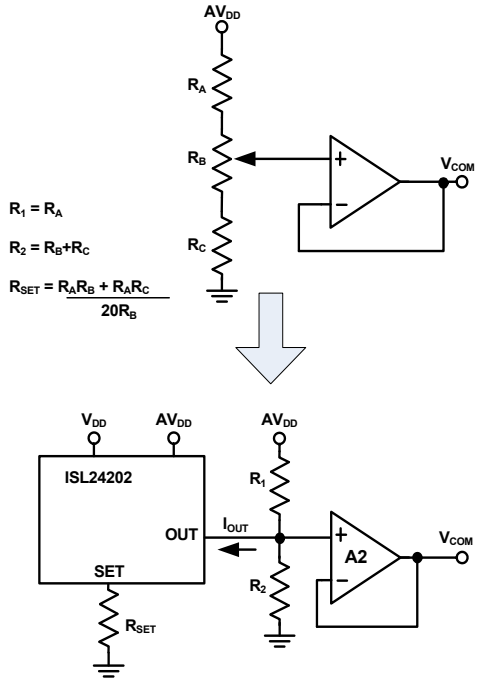


FIGURE 3. MECHANICAL ADJUSTMENT REPLACEMENT

DCP (Digitally Controllable Potentiometer)

The DCP controls the voltage that ultimately controls the SET current. Figure 4 shows the relationship between the register value and the DCP's tap position. Note that a register value of 0 selects the first step of the resistor string. The output voltage of the DCP is given in Equation 1:

$$V_{DCP} = \left(\frac{RegisterValue + 1}{256}\right)\left(\frac{AV_{DD}}{20}\right) \quad \text{(EQ. 1)}$$

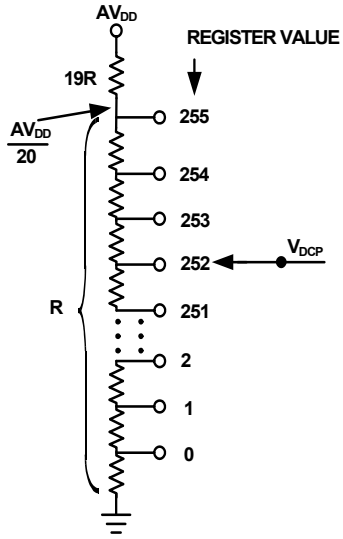


FIGURE 4. SIMPLIFIED SCHEMATIC OF DCP

Output Current Sink

Figure 5 shows the schematic of the OUT current sink. The combination of amplifier A1, transistor Q1, and resistor R_{SET} forms a voltage-controlled current source, with the voltage determined by the DCP setting.

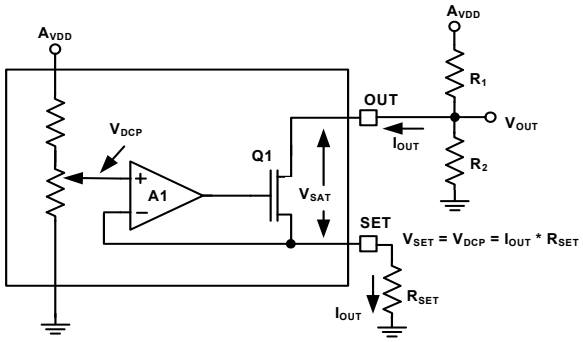


FIGURE 5. CURRENT SINK CIRCUIT

The external R_{SET} resistor sets the full-scale (maximum) sink current that can be pulled from the OUT node. The relationship between I_{OUT} and Register Value is shown in Equation 2.

$$I_{OUT} = \frac{V_{DCP}}{R_{SET}} = \left(\frac{RegisterValue + 1}{256}\right)\left(\frac{AV_{DD}}{20}\right)\left(\frac{1}{R_{SET}}\right) \quad \text{(EQ. 2)}$$

The maximum value of I_{OUT} can be calculated by substituting the maximum register value of 255 into Equation 2, resulting in Equation 3:

$$I_{OUT}(MAX) = \frac{A_{VDD}}{20R_{SET}} \quad \text{(EQ. 3)}$$

Equation 2 can also be used to calculate the unit sink current step size per Register Code, resulting in Equation 4:

$$I_{STEP} = \frac{AV_{DD}}{(256)(20)(R_{SET})} \quad \text{(EQ. 4)}$$

Determination of R_{SET}

The ultimate goal for the ISL24202 is to generate an adjustable voltage between two endpoints, V_{COM_MIN} and V_{COM_MAX}, with a fixed power supply voltage, AV_{DD}. This is accomplished by choosing the correct values for R_{SET}, R_1 and R_2. The exact value of R_{SET} is not critical. Values from 1k to more than 100k will work under most conditions. The following expression calculates the minimum R_{SET} value:

$$R_{SET}(MIN) = \left(\frac{\frac{AV_{DD}}{16}}{\left(V_{OUT(MIN)} - \frac{AV_{DD}}{20}\right)}\right)(k\Omega) \quad \text{(EQ. 5)}$$

Note that this is the absolute minimum value for R_{SET}. Larger R_{SET} values reduce quiescent power, since R_1 and R_2 are proportional to R_{SET}. The ISL24202 is tested with a 5kΩ R_{SET}.

Determination of R_1 and R_2

With AV_{DD}, $V_{COM(MIN)}$ and $V_{COM(MAX)}$ known and R_{SET} chosen per the above requirements, R_1 and R_2 can be determined using Equations 6 and 7:

$$R_1 = 5120 \cdot R_{SET}\left(\frac{V_{COM(MAX)} - V_{COM(MIN)}}{256 \cdot V_{COM(MAX)} - V_{COM(MIN)}}\right) \quad \text{(EQ. 6)}$$

$$R_2 = 5120 \cdot R_{SET}\left(\frac{V_{COM(MAX)} - V_{COM(MIN)}}{255 \cdot AV_{DD} + V_{COM(MIN)} - 256 \cdot V_{COM(MAX)}}\right) \quad \text{(EQ. 7)}$$

Final Transfer Function

The voltage at the OUT pin can be calculated from Equation 8:

$$V_{OUT} = AV_{DD}\left(\frac{R_2}{R_1+R_2}\right)\left(1 - \frac{RegisterValue + 1}{256}\left(\frac{R_1}{20R_{SET}}\right)\right) \quad \text{(EQ. 8)}$$

With external amplifier A2 in the unity-gain configuration, $V_{OUT} = V_{COM}$.

Example

As an example, suppose the A_{VDD} supply is 15V, the desired V_{COM_MIN} = 6.5V and the desired V_{COM_MAX} = 8.5V. R_{SET} is arbitrarily chosen to be 7.5kΩ.

First, verify that our chosen R_{SET} meets the minimum requirement described in Equation 5:

$$(7.5k\Omega) > \left(R_{SET}(MIN) = \left(\frac{\frac{15}{16}}{\left(6.5V - \frac{15}{20}\right)}\right) = 0.163k\Omega\right) \quad \text{(EQ. 9)}$$

Using Equations 6 and 7, calculate the values of R_1 and R_2:

$$R_1 = 5120 \cdot 7500 \cdot \left(\frac{8.5-6.5}{256 \cdot 8.5 - 6.5}\right) = 35.4k\Omega \quad \text{(EQ. 10)}$$

$$R_2 = 5120 \cdot 7500 \cdot \left(\frac{8.5 - 6.5}{255 \cdot 15 + 6.5 - 256 \cdot 8.5}\right) = 46.4k\Omega \quad \text{(EQ. 11)}$$

Table 1 shows the resulting V_{COM} voltage as a function of register value for these conditions.

TABLE 1. EXAMPLE V_{OUT} vs REGISTER VALUE

REGISTER VALUE	V_{OUT} (V)
0	8.49
20	8.34
40	8.18
60	8.02
80	7.87
100	7.71
120	7.55
127	7.50
140	7.40
160	7.24
180	7.09
200	6.93
220	6.77
240	6.62
255	6.50

Output Voltage Span Calculation

It is also possible to calculate $V_{COM(MIN)}$ and $V_{COM(MAX)}$ from the existing resistor values.

V_{COM_MIN} occurs when the greatest current, $I_{OUT(MAX)}$, is drawn from the middle node of the R_1/R_2 divider. Substituting RegisterValue = 255 into Equation 8 gives the following:

$$V_{COM(MIN)} = AV_{DD}\left(\frac{R_2}{R_1+R_2}\right)\left(1 - \left(\frac{R_1}{20R_{SET}}\right)\right) \quad \text{(EQ. 12)}$$

Similarly, RegisterValue = 0 for $V_{COM(MAX)}$:

$$V_{COM(MAX)} = AV_{DD}\left(\frac{R_2}{R_1+R_2}\right)\left(1 - \frac{1}{256}\left(\frac{R_1}{20R_{SET}}\right)\right) \quad \text{(EQ. 13)}$$

By finding the difference of Equation 13 and Equation 12, the total span of V_{COM} can be found:

$$V_{COM}SPAN = AV_{DD}\left(\frac{R_2}{R_1+R_2}\right)\left(1 - \frac{1}{256}\right)\left(\frac{R_1}{20R_{SET}}\right) \quad \text{(EQ. 14)}$$

Assuming that the $I_{OUT}(MIN) = 0$ instead of I_{STEP}, the expression in Equation 14 simplifies to:

$$V_{COM}SPAN = \left(\frac{R_1 \cdot R_2}{R_1 + R_2}\right)\left(\frac{AV_{DD}}{20R_{SET}}\right) = \left(\frac{R_1 \cdot R_2}{R_1 + R_2}\right)I_{DVROUT}(MAX) \quad \text{(EQ. 15)}$$

OUT Pin Leakage Current

When the voltage on the OUT pin is greater than 10V, an additional leakage current flows into the pin in addition to the I_{SET} current. Figure 6 shows the I_{SET} current and the OUT pin current for OUT pin voltage up to 19V. In applications where the voltage on the OUT pin will be greater than 10V, the actual output voltage will be lower than the voltage calculated by Equation 8 due to this extra current. The graph in Figure 6 was measured with $R_{SET} = 4.99k\Omega$.

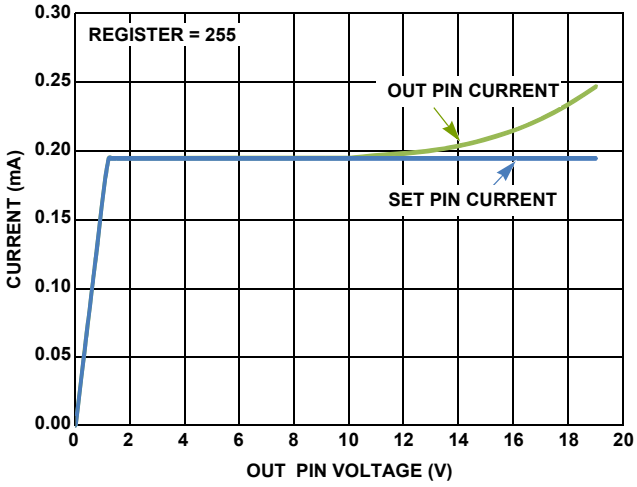


FIGURE 6. OUT PIN LEAKAGE CURRENT

Power Supply Sequence

The recommended power supply sequencing is shown in Figure 7. When applying power, V_{DD} should be applied before or at the same time as AV_{DD}. The minimum time for t_{VS} is 0µs. When removing power, the sequence of V_{DD} and AV_{DD} is not important.

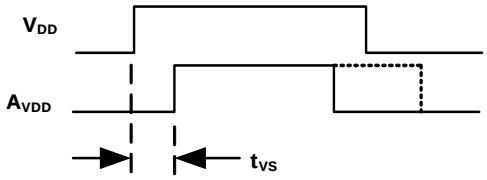


FIGURE 7. POWER SUPPLY SEQUENCE

Do not remove V_{DD} or AV_{DD} within 100ms of the start of the EEPROM programming cycle. Removing power before the EEPROM programming cycle is completed may result in corrupted data in the EEPROM.

Operating and Programming Supply Voltage and Current

To program the EEPROM, AV_{DD} must be ≥10.8V. If further programming is not required, the ISL24202 will operate over an AV_{DD} range of 4.5V to 19V.

During EEPROM programming, I_{DD} and I_{AVDD} will temporarily be 4-5x higher for up to 100ms (t_{PROG}).

Up/Down Counter Interface

The ISL24202 allows the adjustment of the output V_{COM} voltage and the programming of the non-volatile memory through a single pin (CTL) when the CE (counter enable) pin is high. The CTL pin is biased so that its voltage is set to VDD/2 if the driving circuit is set to Tri-state or High Impedance (Hi-Z), allowing up/down operation using common digital I/O logic.

CTL Pin

When a mid-high-mid transition is detected on the CTL pin (see Figure 11), the internal register value counts down by one at the trailing (high-mid) edge, and the output V_{COM} voltage is increased according to Equation 8. Similarly, when a mid-low-mid transition is detected on the CTL pin, the internal register value counts up by one at the trailing (low-mid) edge, and the output V_{COM} voltage is decreased. Once the maximum or minimum value is reached, the counter saturates and will not overflow or underflow beyond those values.

CTL should have a noise filter to reduce bouncing or noise on the input that could cause unwanted counts when the CE pin is high. Figure 8 shows a simple debouncing circuit consisting of a series 1kΩ resistor and a shunt 0.01µF capacitor connected on the CTL pin. To avoid unintentional adjustment, the ISL24202 guarantees to reject CTL pulses shorter than 20µs.

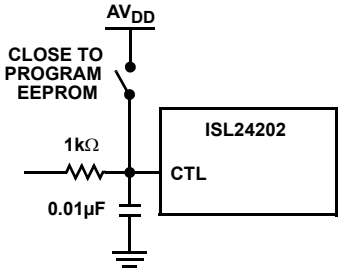


FIGURE 8. EXTERNAL DEBOUNCER ON CTL PIN

This pin is pulled above 4.9V to program the EEPROM. See “Programming the EEPROM” on page 9 for details.

After CE (Counter Enable) is asserted and after programming EEPROM, the very first CTL pulse is ignored (see Figure 11) to avoid the possibility of a false count (since CTL state may be unknown after programming).

CE Pin

To change the counter controlling the output voltage, the CE (Counter Enable) pin must be pulled high (V_{DD}). When the CE pin is pulled low, the counter value is loaded from EEPROM, which takes 10ms (during which the inputs should remain constant). The CE pin has an internal pull-down to keep it at a logic low

when not being driven. CE should be pulled low before powering the device down to ensure that any glitches or transients during power-down will not cause unwanted EEPROM overwriting.

The CE pin has a Schmitt trigger on the input to prevent false triggering during slow transitions of the CE pin. The CE pin transition time should be 10µs or less.

Programming the EEPROM

To program the non-volatile EEPROM, pull the CTL pin above 4.9V for more than 200µs. The level and timing is shown in Figure 9. It then takes a maximum of 100ms after CTL crosses 4.9V for the programming to be completed inside the device.

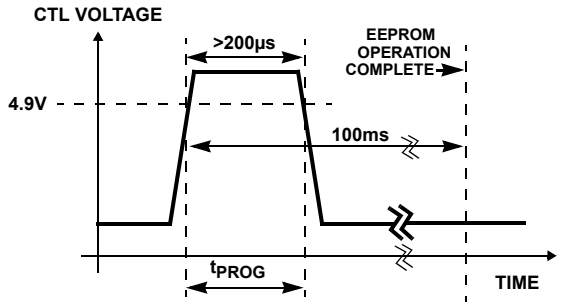


FIGURE 9. EEPROM PROGRAMMING

When the part is programmed, the data in the counter register is written into the EEPROM. This value will be loaded from the EEPROM during subsequent power-ups as well as when the CE pin is pulled low. The ISL24202 is factory-programmed to mid-scale. As with asserting CE, the first pulse after a program operation is ignored. The EEPROM contents can be written and verified using the following steps:

1. Power-up the ISL24202. The EEPROM value will be loaded.
2. Set the CE pin to V_{DD}.
3. Change the V_{OUT} voltage using the CTL pin to the desired value, noting that first pulse will be ignored.
4. Pull the CTL pin to 4.9V or higher for at least 200µs. The counter value will be written to EEPROM after 100ms.
5. Change the V_{OUT} value (using the CTL pin) to a different value, noting that first pulse after programming will be ignored.
6. Set the CE pin to 0V. The stored output value will be loaded from EEPROM after 10ms.
7. Verify that the output value is the same value programmed in Step 4.

The CTL pin should be left floating after programming. The voltage at the CTL pin will be internally biased to $V_{DD}/2$ to ensure that no additional pulses will be seen by the Up/Down counter. To prevent further changes, ground the CE pin.

Typical Application Circuit

Shown below in Figure 10 is a typical circuit that can be used to program the ISL24202 via the up/down counter interface. Three momentary push-button switches are required. SW1 connected between CTL and AV_{DD} allows the user to bring CTL above V_{DD} for programming the EEPROM, SW2 connected to V_{DD} to pull CTL up, and SW3 connected to GND to pull CTL to down. All the switches should have 1kΩ current-limiting resistors in series.

For adjustment and programming to occur, the CE pin has to be set to V_{DD}. This can be achieved by a single-pull double-throw switch (SW4) connected between V_{DD} and GND.

Note that pressing the UP button increments the counter, but results in V_{COM_OUT} decreasing. Similarly, pressing the DOWN button decrements the counter, and results in V_{COM_OUT} increasing.

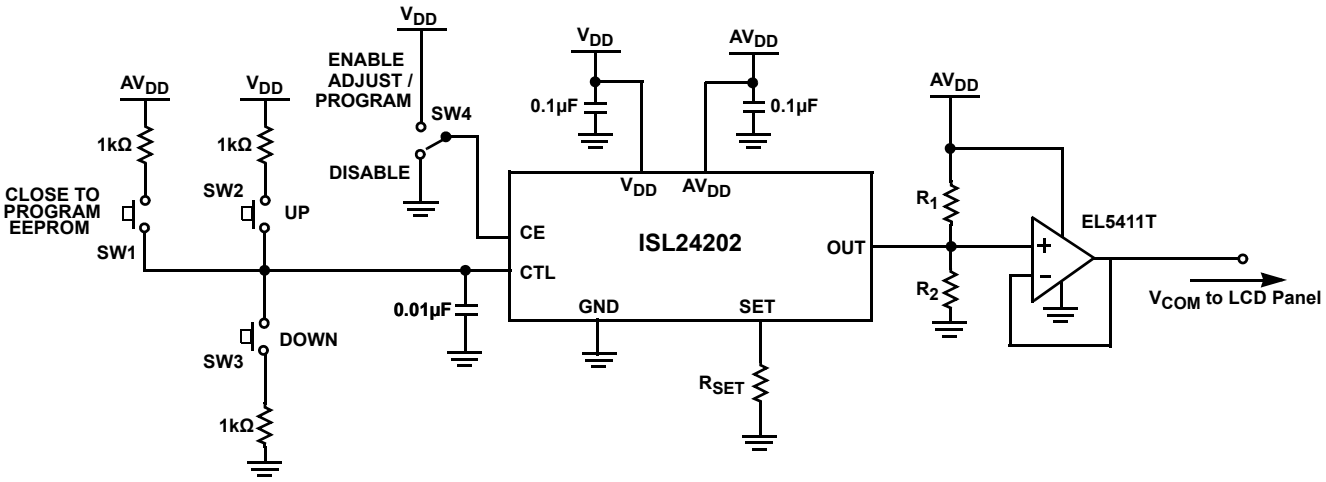


FIGURE 10. TYPICAL APPLICATION CIRCUIT

Up/Down Counter Waveforms

The operation modes of the ISL24202 is shown in Table 2.

TABLE 2. ISL24202 OPERATION MODES

INPUT		OUTPUT		
CTL	CE	Counter	V_{COM_OUT}	EEPROM
X	Lo	No Change		
X	Lo to Hi	Ignore first CTL pulse		No Change
Hi to Mid	Hi	Decrement	Increase	No Change
Lo to Mid	Hi	Increment	Decrease	No Change
Mid to >4.9V	Hi	No Change	No Change	Write Counter Value to EEPROM
>4.9V to Mid	Hi	Ignore next CTL Pulse		No Change
X	Hi to Lo	EEPROM Read Value	Programmed Value	No Change

Figure 11 shows the associated waveforms.

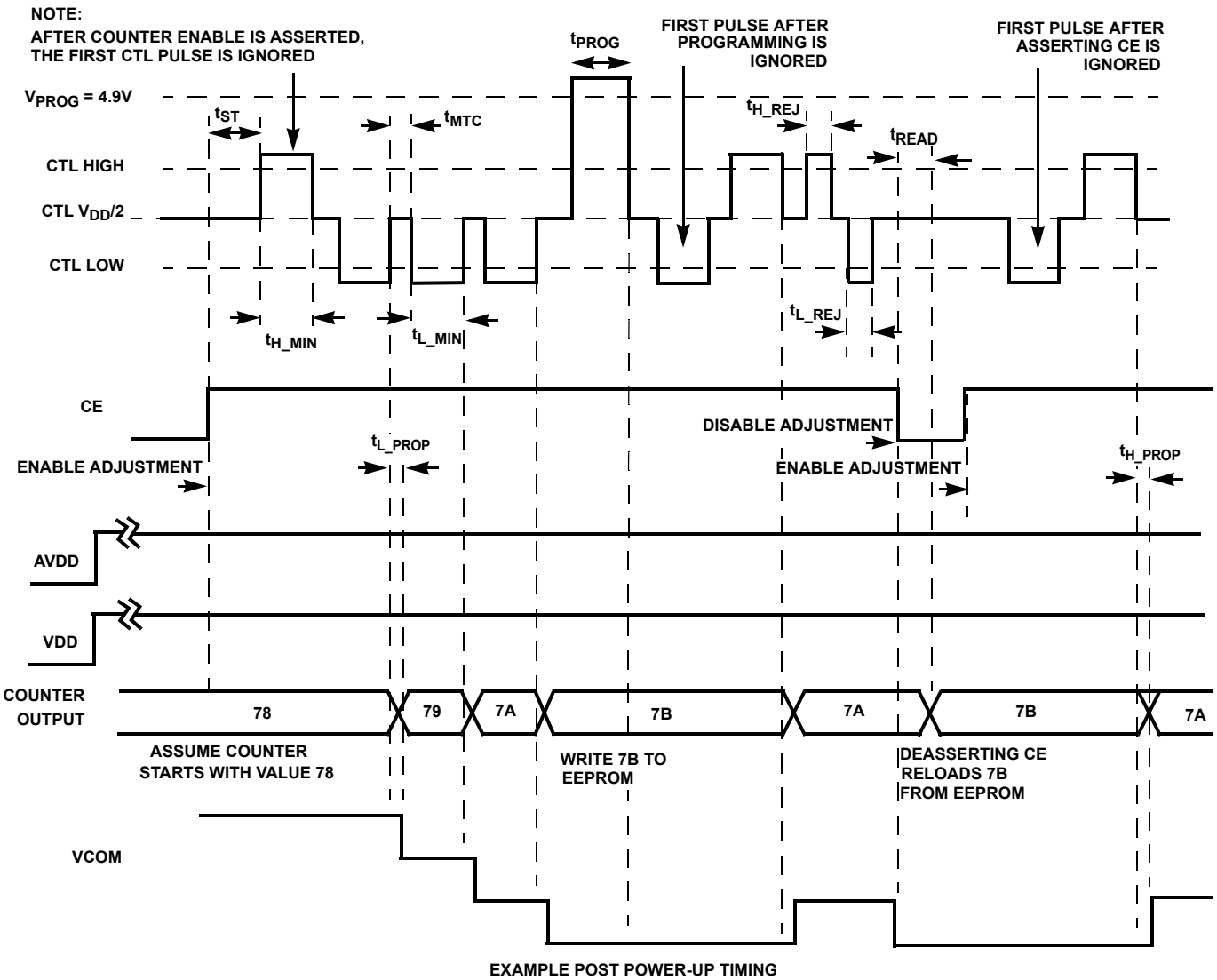


FIGURE 11. COUNTER INTERFACE TIMING DIAGRAM

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to web to make sure you have the latest revision.

DATE	REVISION	CHANGE
3/15/11	FN7587.0	Initial release.

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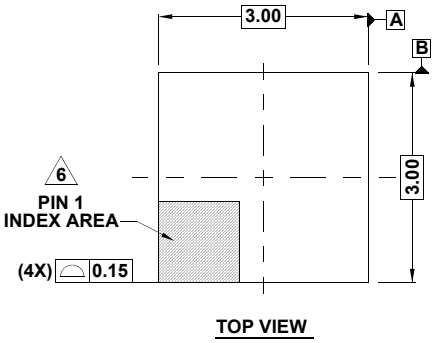
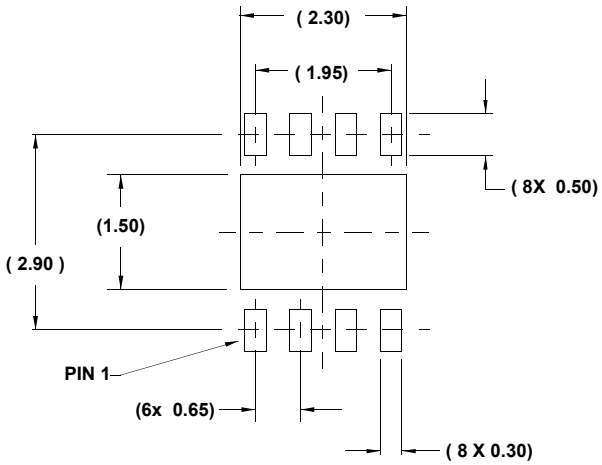
Package Outline Drawing

L8.3x3A

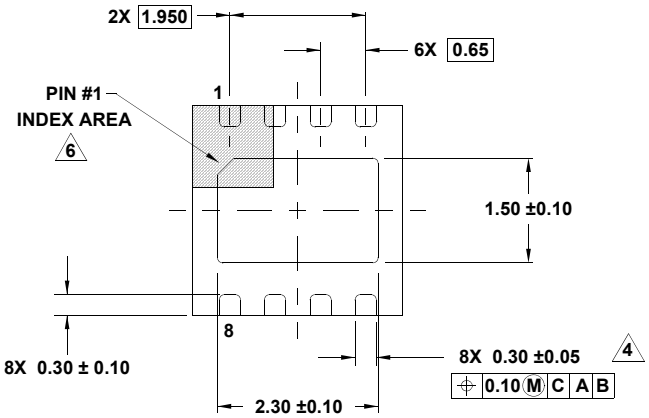
8 LEAD THIN DUAL FLAT NO-LEAD PLASTIC PACKAGE
Rev 4, 2/10



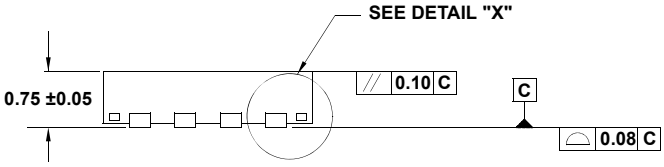
TOP VIEW



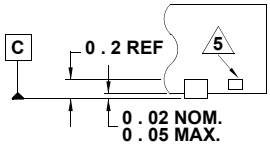
TYPICAL RECOMMENDED LAND PATTERN



BOTTOM VIEW



SIDE VIEW



DETAIL "X"

NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to ASME Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Dimension applies to the metallized terminal and is measured between 0.15mm and 0.20mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.
7. Compliant to JEDEC MO-229 WEEC-2 except for the foot length.

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