

## MAX34451

## PMBus 16-Channel V/I Monitor and 12-Channel Sequencer/Marginer

### General Description

The MAX34451 is a power-supply system manager that is capable of monitoring up to 16 different voltage rails or currents and is also capable of sequencing and margining up to 12 power supplies. The system manager monitors the power-supply output voltages and currents and constantly checks them for user programmable over and under threshold limits. If a fault is detected, the device automatically shuts down the system in an orderly fashion. The device can sequence the supplies in any order at both power-up and power-down. The device has the ability to close-loop margin the power-supply output voltages up or down to a user-programmable level. The device contains an internal temperature sensor and can support up to four external remote temperature sensors. Once configured, the device can operate autonomously without any host intervention.

### Applications

- Network Switches/Routers
- Base Stations
- Servers
- Smart Grid Network Systems

### Ordering Information

| PART          | TEMP RANGE     | PIN-PACKAGE |
|---------------|----------------|-------------|
| MAX34451ETN+  | -40°C to +85°C | 56 TQFN-EP* |
| MAX34451ETN+T | -40°C to +85°C | 56 TQFN-EP* |

+Denotes a lead(Pb)-free/RoHS-compliant package.

T = Tape and reel.

\*EP = Exposed pad.

Typical Operating Circuit appears at end of data sheet.

### Benefits and Features

- Integration Enables Management of Multiple Power Supplies to Maximize System Performance
  - 16 Channels of Voltage or Current Monitoring
  - 12 Channels of Sequencing and Margining (8 PWM, 4 External Current DACs (1 x DS4424), and Sequencing)
  - Expandable Channel Operation with Parallel Devices
  - Remote Ground Sensing Improves Measurement Accuracy
  - Programmable Up and Down Time-Based or Event-Based Sequencing
  - Dual Sequencing Loops
  - Configurable Combinatorial Logic Supporting Up to 16 GPIs and 20 GPOs
  - Automatic Closed-Loop Margining
  - No External Clocking Required
  - PMBus™-Compliant Command Interface
- Fast, Reliable Control and Fault Detection Improves System Reliability
  - Fast Minimum/Maximum Threshold Excursion Detection
  - Supports Up to 5 Temperature Sensors (1 Internal and 4 Remote)
  - Fault Detection on All Temperature Sensors
  - Reports Peak, Minimum, and Average Levels for a Number of Parameters
  - Programmable Alarm Outputs
  - On-Board Nonvolatile Black Box Fault Logging and Default Configuration Setting
- I<sup>2</sup>C-/SMBus-Compatible Serial Bus with Bus Time-Out Function Simplifies Additional Temperature Sensors and DACs to the MAX34451
- +3.0V to +3.6V Supply Voltage

PMBus is a trademark of SMIF, Inc.



## Absolute Maximum Ratings

$V_{DD}$  and  $V_{DDA}$  to  $V_{SS}$  ..... -0.3V to +4.0V  
 RSG0 and RSG1 to  $V_{SS}$  ..... -0.3V to +0.3V  
 All Other Pins Except REG18  
     Relative to  $V_{SS}$  ..... -0.3V to ( $V_{DD} + 0.3V$ )\*  
 REG18 to  $V_{SS}$  ..... -0.3V to +2.0V

\*Subject to not exceeding +4.0V.

Continuous Power Dissipation ( $T_A = +70^\circ\text{C}$ )  
     TQFN (derate 27.8mW/ $^\circ\text{C}$  above  $+70^\circ\text{C}$ ) ..... 2222.2mW  
 Operating Temperature Range .....  $-40^\circ\text{C}$  to  $+85^\circ\text{C}$   
 Storage Temperature Range .....  $-55^\circ\text{C}$  to  $+125^\circ\text{C}$   
 Lead Temperature (soldering, 10s) .....  $+260^\circ\text{C}$   
 Soldering Temperature (reflow) .....  $+260^\circ\text{C}$

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## RECOMMENDED OPERATING CONDITIONS

( $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ , unless otherwise noted.)

| PARAMETER                                                | SYMBOL    | CONDITIONS              | MIN            | TYP                  | MAX            | UNITS      |
|----------------------------------------------------------|-----------|-------------------------|----------------|----------------------|----------------|------------|
| $V_{DD}$ Operating Voltage Range                         | $V_{DD}$  | (Note 1)                | 3.0            |                      | 3.6            | V          |
| Input Logic 1<br>(Except I <sup>2</sup> C and GPIn Pins) | $V_{IH1}$ |                         | 0.7 x $V_{DD}$ |                      | $V_{DD} + 0.3$ | V          |
| Input Logic 0<br>(Except I <sup>2</sup> C and GPIn Pins) | $V_{IL1}$ |                         | -0.3           | $+0.3 \times V_{DD}$ |                | V          |
| Input Logic 1: SCL, SDA,<br>MSCL, MSDA                   | $V_{IH2}$ |                         | 2.1            | $V_{DD} + 0.3$       |                | V          |
| Input Logic 0: SCL, SDA,<br>MSCL, MSDA                   | $V_{IL2}$ |                         | -0.3           | $+0.8$               |                | V          |
| Input Logic 1 (GPIn Pins)                                | $V_{IH3}$ | Minimum pulse width 5ms | 1.5            | $V_{DD} + 0.3$       |                | V          |
| Input Logic 0 (GPIn Pins)                                | $V_{IL3}$ | Minimum pulse width 5ms | -0.3           | $+1.0$               |                | V          |
| Source Impedance to RSn                                  |           | ADC_TIME[1:0] = 00      |                |                      | 1              | k $\Omega$ |
|                                                          |           | ADC_TIME[1:0] = 01      |                |                      | 5              |            |
|                                                          |           | ADC_TIME[1:0] = 10      |                |                      | 10             |            |
|                                                          |           | ADC_TIME[1:0] = 11      |                |                      | 20             |            |
| $V_{DD}$ Rise Time                                       |           | From 0V to 3.0V         |                |                      | 4              | ms         |
| $V_{DD}$ Source Impedance                                |           |                         |                |                      | 10             | $\Omega$   |

## ELECTRICAL CHARACTERISTICS

( $V_{DD}$  and  $V_{DDA} = 3.0V$  to  $3.6V$ ,  $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ , unless otherwise noted. Typical values are at  $V_{DD}/V_{DDA} = 3.3V$ ,  $T_A = +25^\circ\text{C}$ .)  
 (Note 2)

| PARAMETER                                          | SYMBOL         | CONDITIONS                                    | MIN | TYP | MAX | UNITS |
|----------------------------------------------------|----------------|-----------------------------------------------|-----|-----|-----|-------|
| <b>GENERAL</b>                                     |                |                                               |     |     |     |       |
| Supply Current                                     | $I_{CPU}$      | (Note 3)                                      |     | 12  |     | mA    |
|                                                    | $I_{PROGRAM}$  |                                               |     | 18  |     |       |
| System Clock Error                                 | $f_{ERR:MOSC}$ | $+25^\circ\text{C} < T_A < +85^\circ\text{C}$ | -3  |     | +3  | %     |
|                                                    |                | $-40^\circ\text{C} < T_A < +25^\circ\text{C}$ | -4  |     | +4  |       |
| Output Logic-Low<br>(Except I <sup>2</sup> C Pins) | $V_{OL1}$      | $I_{OL} = 4mA$ (Note 1)                       |     |     | 0.4 | V     |

**ELECTRICAL CHARACTERISTICS (continued)**

( $V_{DD}$  and  $V_{DDA}$  = 3.0V to 3.6V,  $T_A$  = -40°C to +85°C, unless otherwise noted. Typical values are at  $V_{DD}/V_{DDA}$  = 3.3V,  $T_A$  = +25°C.)  
(Note 2)

| PARAMETER                                      | SYMBOL             | CONDITIONS                          | MIN                   | TYP   | MAX   | UNITS           |
|------------------------------------------------|--------------------|-------------------------------------|-----------------------|-------|-------|-----------------|
| Output Logic-High<br>(Except I2C Pins)         | V <sub>OH1</sub>   | I <sub>OH</sub> = -2mA (Note 1)     | V <sub>DD</sub> - 0.5 |       |       | V               |
| Output Logic-Low: SCL, SDA,<br>MSCL, MSDA      | V <sub>OL2</sub>   | I <sub>OL</sub> = 4mA (Note 1)      | 0.4                   |       |       | V               |
| SCL, SDA, MSCL, MSDA<br>Leakage                | I <sub>LI2C</sub>  | V <sub>DD</sub> = 0V or unconnected | ±5                    |       |       | μA              |
| CONTROL0 Threshold                             |                    |                                     | 2.048                 |       |       | V               |
| CONTROL0 Hysteresis                            |                    |                                     | 50                    |       |       | mV              |
| ADC                                            |                    |                                     |                       |       |       |                 |
| ADC Bit Resolution                             |                    |                                     | 12                    |       |       | Bits            |
| ADC Conversion Time                            |                    | ADC_TIME[1:0] = 00                  | 1000                  |       |       | ns              |
| ADC Full Scale                                 | V <sub>FS</sub>    | T <sub>A</sub> = 0°C to +85°C       | 2.032                 | 2.048 | 2.064 | V               |
| ADC Measurement Resolution                     | V <sub>LSB</sub>   |                                     | 500                   |       |       | μV              |
| RSn Input Capacitance                          | C <sub>RS</sub>    |                                     | 15                    |       |       | pF              |
| RSn Input Leakage                              | I <sub>LRS</sub>   | 0V < V <sub>RSn</sub> < 2.1V        | ±0.25                 |       |       | μA              |
| ADC Integral Nonlinearity                      | INL                |                                     | ±1                    |       |       | LSB             |
| ADC Differential Nonlinearity                  | DNL                |                                     | ±1                    |       |       | LSB             |
| TEMPERATURE SENSOR                             |                    |                                     |                       |       |       |                 |
| Internal Temperature-<br>Measurement Error     |                    | T <sub>A</sub> = -40°C to +85°C     | ±2                    |       |       | °C              |
| FLASH                                          |                    |                                     |                       |       |       |                 |
| Flash Endurance                                | N <sub>FLASH</sub> | Note 3                              | 20,000                |       |       | Write<br>Cycles |
| Data Retention                                 |                    | T <sub>A</sub> = +50°C (Note 4)     | 100                   |       |       | Years           |
| STORE_DEFAULT_ALL,<br>MFR_STORE_ALL Write Time |                    |                                     | 80                    |       |       | ms              |
| RESTORE_DEFAULT_ALL                            |                    | With MFR_STORE_SINGLE data          | 105                   |       |       | ms              |
| RESTORE_DEFAULT_ALL or<br>MFR_RESTORE_ALL      |                    | Without MFR_STORE_SINGLE data       | 500                   |       |       | μs              |
| MFR_STORE_SINGLE<br>Write Time                 |                    |                                     | 310                   |       |       | μs              |
| MFR_NV_FAULT_LOG<br>Write Time                 |                    | Writing 1 fault log                 | 11                    |       |       | ms              |
| MFR_NV_FAULT_LOG<br>Delete Time                |                    | Deleting all fault logs             | 200                   |       |       | ms              |
| MFR_NV_FAULT_LOG<br>Overwrite Time             |                    |                                     | 40                    |       |       | ms              |

**ELECTRICAL CHARACTERISTICS (continued)**

( $V_{DD}$  and  $V_{DDA}$  = 3.0V to 3.6V,  $T_A$  = -40°C to +85°C, unless otherwise noted. Typical values are at  $V_{DD}/V_{DDA}$  = 3.3V,  $T_A$  = +25°C.)  
(Note 2)

| PARAMETER                                   | SYMBOL | CONDITIONS                    | MIN | TYP   | MAX | UNITS |
|---------------------------------------------|--------|-------------------------------|-----|-------|-----|-------|
| <b>TIMING OPERATING CHARACTERISTICS</b>     |        |                               |     |       |     |       |
| Round-Robin Voltage and Current Sample Rate |        | Threshold excursion (Note 5)  |     | 64    |     | μs    |
|                                             |        | Data collection               |     | 5     |     | ms    |
| Temperature Sample Rate                     |        |                               |     | 1000  |     | ms    |
| Device Startup Time                         |        | With MFR_STORE_SINGLE data    |     | 170   |     | ms    |
|                                             |        | Without MFR_STORE_SINGLE data |     | 90    |     |       |
| PWM Frequency                               |        | PWM power-supply margining    |     | 312.5 |     | kHz   |
| PWM Resolution                              |        | PWM power-supply margining    |     | 8     |     | Bits  |

**Note 1:** All voltages are referenced to ground. Current entering the device are specified as positive and currents exiting the device are negative.

**Note 2:** Limits are 100% production tested at  $T_A$  = +25°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization.

**Note 3:** This does not include pin input/output currents.

**Note 4:** Guaranteed by design.

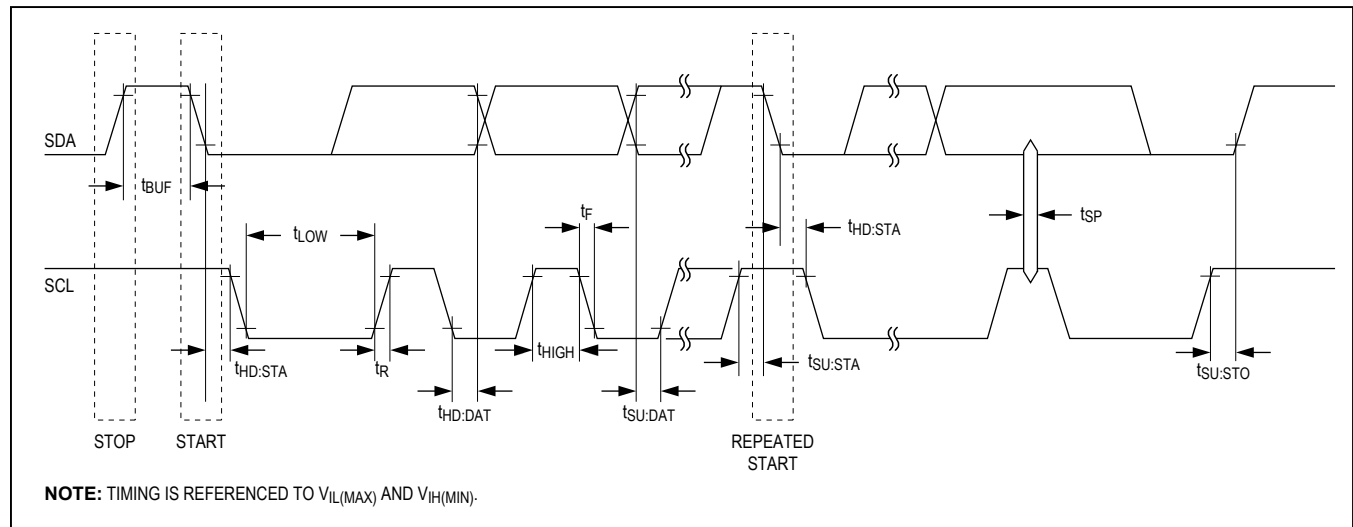
**Note 5:** The round-robin threshold excursion rate can be changed with the ADC\_AVERAGE and ADC\_TIME bits in MFR\_MODE from 16μs (no averaging and 1μs conversion) to 1024μs (8x averaging and 8μs conversion).

**I<sup>2</sup>C/SMBus INTERFACE ELECTRICAL SPECIFICATIONS**

( $V_{DD}$  and  $V_{DDA}$  = 3.0V to 3.6V,  $T_A$  = -40°C to +85°C, unless otherwise noted. Typical values are at  $V_{DD}/V_{DDA}$  = 3.3V,  $T_A$  = +25°C.)

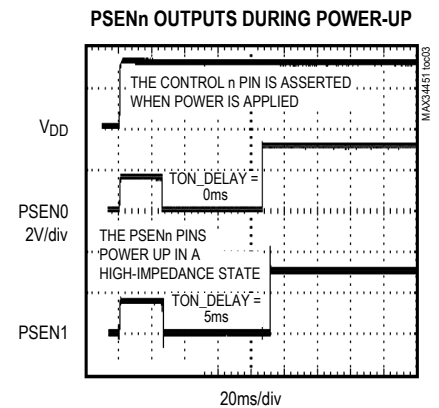
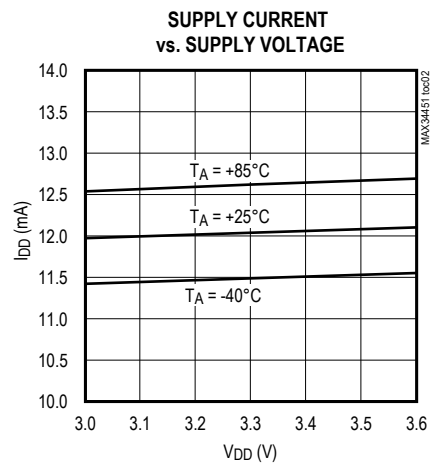
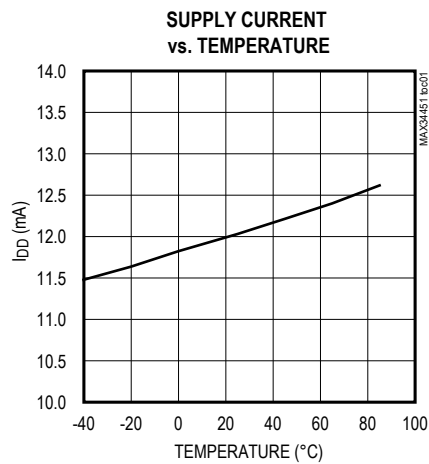
| PARAMETER                                       | SYMBOL       | CONDITIONS | MIN | TYP | MAX | UNITS |
|-------------------------------------------------|--------------|------------|-----|-----|-----|-------|
| SCL Clock Frequency                             | $f_{SCL}$    |            | 10  |     | 400 | kHz   |
| MSCL Clock Frequency                            | $f_{MSCL}$   |            |     | 100 |     | kHz   |
| Bus Free Time Between STOP and START Conditions | $t_{BUF}$    |            | 1.3 |     |     | μs    |
| Hold Time (Repeated) START Condition            | $t_{HD:STA}$ |            | 0.6 |     |     | μs    |
| Low Period of SCL                               | $t_{LOW}$    |            | 1.3 |     |     | μs    |
| High Period of SCL                              | $t_{HIGH}$   |            | 0.6 |     |     | μs    |
| Data Hold Time                                  | $t_{HD:DAT}$ | Receive    | 0   |     |     | ns    |
|                                                 |              | Transmit   | 300 |     |     |       |
| Data Setup Time                                 | $t_{SU:DAT}$ |            | 100 |     |     | ns    |
| Start Setup Time                                | $t_{SU:STA}$ |            | 0.6 |     |     | μs    |
| SDA and SCL Rise Time                           | $t_R$        |            |     |     | 300 | ns    |
| SDA and SCL Fall Time                           | $t_F$        |            |     |     | 300 | ns    |
| Stop Setup Time                                 | $t_{SU:STO}$ |            | 0.6 |     |     | μs    |
| Clock Low Timeout                               | $t_{TO}$     |            | 25  | 27  | 35  | ms    |

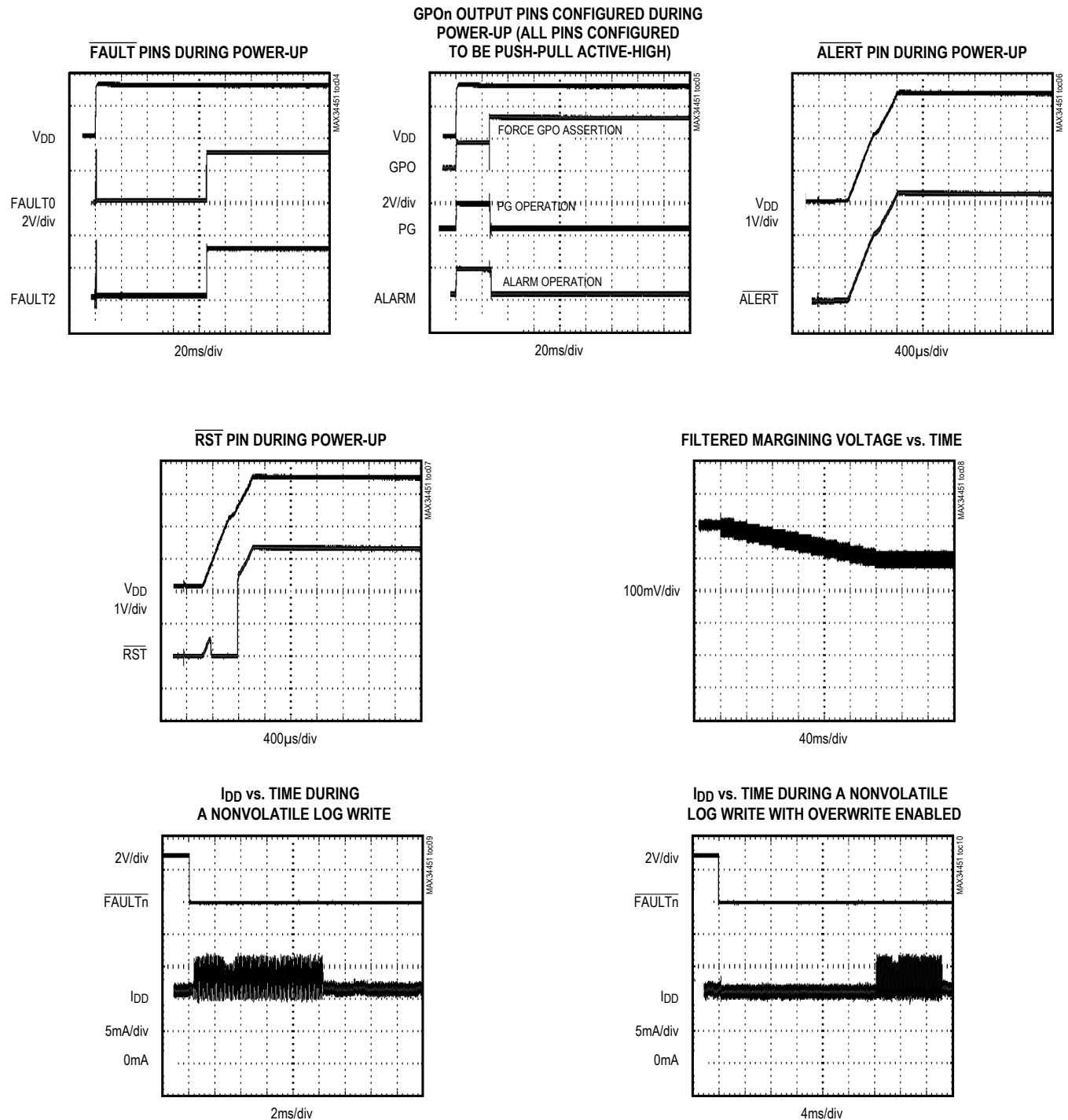
## I<sup>2</sup>C/SMBus Timing



## Typical Operating Characteristics

( $V_{DD} = 3.3V$  and  $T_A = +25^\circ C$ , without MFR\_STORE\_SINGLE data, unless otherwise noted.)

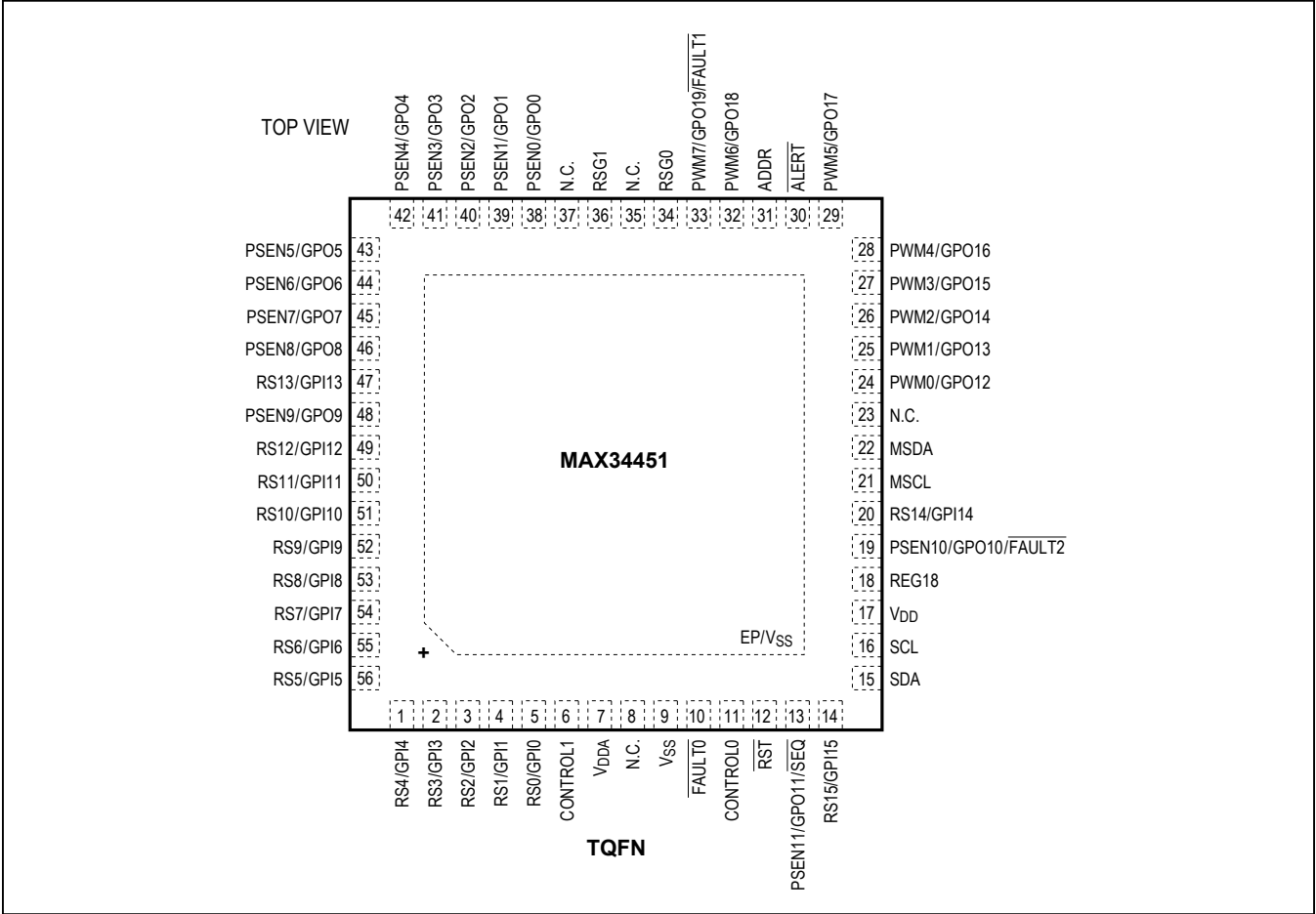


**Typical Operating Characteristics (continued)**(V<sub>DD</sub> = 3.3V and T<sub>A</sub> = +25°C, without MFR\_STORE\_SINGLE data, unless otherwise noted.)

MAX34451

PMBus 16-Channel V/I Monitor and  
12-Channel Sequencer/Marginer

Pin Configuration



Pin Description

| PIN* | NAME     | TYPE** | FUNCTION                                                                                                                                    |
|------|----------|--------|---------------------------------------------------------------------------------------------------------------------------------------------|
| 1    | RS4      | AI     | ADC Voltage-Sense Input 4. Connect to V <sub>SS</sub> if unused.                                                                            |
|      | GPI4     | AI     | General-Purpose Input 4. Connect to V <sub>SS</sub> if unused.                                                                              |
| 2    | RS3      | AI     | ADC Voltage-Sense Input 3. Connect to V <sub>SS</sub> if unused.                                                                            |
|      | GPI3     | AI     | General-Purpose Input 3. Connect to V <sub>SS</sub> if unused.                                                                              |
| 3    | RS2      | AI     | ADC Voltage-Sense Input 2. Connect to V <sub>SS</sub> if unused.                                                                            |
|      | GPI2     | AI     | General-Purpose Input 2. Connect to V <sub>SS</sub> if unused.                                                                              |
| 4    | RS1      | AI     | ADC Voltage-Sense Input 1. Connect to V <sub>SS</sub> if unused.                                                                            |
|      | GPI1     | AI     | General-Purpose Input 1. Connect to V <sub>SS</sub> if unused.                                                                              |
| 5    | RS0      | AI     | ADC Voltage-Sense Input 0. Connect to V <sub>SS</sub> if unused.                                                                            |
|      | GPI0     | AI     | General-Purpose Input 0. Connect to V <sub>SS</sub> if unused.                                                                              |
| 6    | CONTROL1 | DI     | Power-Supply Master On/Off Control Input 1. Active low or active high based on ON_OFF_CONFIG command. Connect to V <sub>SS</sub> if unused. |

## Pin Description (continued)

| PIN* | NAME             | TYPE** | FUNCTION                                                                                                                                                |
|------|------------------|--------|---------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7    | V <sub>DDA</sub> | Power  | Analog Supply Voltage. Bypass V <sub>DDA</sub> to V <sub>SS</sub> with 0.1µF. Connect to V <sub>DD</sub> .                                              |
| 8    | N.C.             | —      | No Connection. Do not connect any signal to this pin.                                                                                                   |
| 9    | V <sub>SS</sub>  | Power  | Ground Reference. Must be connected to EP (exposed pad).                                                                                                |
| 10   | FAULT0           | DIO    | Fault Input/Output 0. Open-drain, active-low I/O. See the <i>Expanded Pin Description</i> section for more details.                                     |
| 11   | CONTROL0         | AI     | Power-Supply Master On/Off Control Input 0. Active low or active high based on ON_OFF_CONFIG command. Connect to V <sub>SS</sub> if unused.             |
| 12   | RST              | DIO    | Active-Low Reset Input/Output. Contains an internal pullup.                                                                                             |
| 13   | PSEN11           | DO     | Power-Supply Enable 11. See the <i>Expanded Pin Description</i> section for more details.                                                               |
|      | GPO11            | DO     | General-Purpose Output 11                                                                                                                               |
|      | SEQ              | DIO    | Sequencing Input/Output. Open-drain, active-low I/O. This pin is used as a handshake signal to coordinate sequencing in systems using multiple devices. |
| 14   | RS15             | AI     | ADC Voltage-Sense Input 15. Connect to V <sub>SS</sub> if unused.                                                                                       |
|      | GPI15            | AI     | General-Purpose Input 15. Connect to V <sub>SS</sub> if unused.                                                                                         |
| 15   | SDA              | DIO    | I <sup>2</sup> C/SMBus-Compatible Input/Output. Open-drain output.                                                                                      |
| 16   | SCL              | DIO    | I <sup>2</sup> C/SMBus-Compatible Clock Input/Output. Open-drain output.                                                                                |
| 17   | V <sub>DD</sub>  | Power  | Digital Supply Voltage. Bypass V <sub>DD</sub> to V <sub>SS</sub> with 0.1µF. Connect to V <sub>DDA</sub> .                                             |
| 18   | REG18            | Power  | Regulator for Digital Circuitry. Bypass to V <sub>SS</sub> with 1µF and 10nF (500mΩ maximum ESR). Do not connect other circuitry to this pin.           |
| 19   | PSEN10           | DO     | Power-Supply Enable 10. See the <i>Expanded Pin Description</i> section for more details.                                                               |
|      | GPO10            | DO     | General-Purpose Output 10                                                                                                                               |
|      | FAULT2           | DIO    | Fault Input/Output 2. Open-drain, active-low I/O. See the <i>Expanded Pin Description</i> section for more details.                                     |
| 20   | RS14             | AI     | ADC Voltage-Sense Input 14. Connect to V <sub>SS</sub> if unused.                                                                                       |
|      | GPI14            | AI     | General-Purpose Input 14. Connect to V <sub>SS</sub> if unused.                                                                                         |
| 21   | MSCL             | DIO    | Master I <sup>2</sup> C Clock Input/Output. Open-drain output.                                                                                          |
| 22   | MSDA             | DIO    | Master I <sup>2</sup> C Data Input/Output. Open-drain output.                                                                                           |
| 23   | N.C.             | —      | No Internal Connection                                                                                                                                  |
| 24   | PWM0             | DO     | PWM Margin Output 0. See the <i>Expanded Pin Description</i> section for more details.                                                                  |
|      | GPO12            | DO     | General-Purpose Output 12                                                                                                                               |
| 25   | PWM1             | DO     | PWM Margin Output 1. See the <i>Expanded Pin Description</i> section for more details.                                                                  |
|      | GPO13            | DO     | General-Purpose Output 13                                                                                                                               |
| 26   | PWM2             | DO     | PWM Margin Output 2. See the <i>Expanded Pin Description</i> section for more details.                                                                  |
|      | GPO14            | DO     | General-Purpose Output 14                                                                                                                               |
| 27   | PWM3             | DO     | PWM Margin Output 3. See the <i>Expanded Pin Description</i> section for more details.                                                                  |
|      | GPO15            | DO     | General-Purpose Output 15                                                                                                                               |
| 28   | PWM4             | DO     | PWM Margin Output 4. See the <i>Expanded Pin Description</i> section for more details.                                                                  |
|      | GPO16            | DO     | General-Purpose Output 16                                                                                                                               |



## Pin Description (continued)

| PIN* | NAME   | TYPE** | FUNCTION                                                                                                                                                                                                                      |
|------|--------|--------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 29   | PWM5   | DO     | PWM Margin Output 5. See the <i>Expanded Pin Description</i> section for more details.                                                                                                                                        |
|      | GPO17  | DO     | General-Purpose Output 17                                                                                                                                                                                                     |
| 30   | ALERT  | DO     | Alert Output. Open-drain, active-low output.                                                                                                                                                                                  |
| 31   | ADDR   | DI     | SMBus Slave Address Select. This pin is sampled on device power-up to determine the SMBus address. See the <i>PMBus/SMBus Address Select</i> section for details on how to strap this pin to select the proper slave address. |
| 32   | PWM6   | DO     | PWM Margin Output 6. See the <i>Expanded Pin Description</i> section for more details.                                                                                                                                        |
|      | GPO18  | DO     | General-Purpose Output 18                                                                                                                                                                                                     |
| 33   | PWM7   | DO     | PWM Margin Output 7. See the <i>Expanded Pin Description</i> section for more details.                                                                                                                                        |
|      | GPO19  | DO     | General-Purpose Output 19                                                                                                                                                                                                     |
|      | FAULT1 | DIO    | Fault Input/Output 1. Open-drain, active-low I/O. See the <i>Expanded Pin Description</i> section for more details.                                                                                                           |
| 34   | RSG0   | AI     | Remote-Sense Ground for RS0/GPI0 to RS3/GPI3 and RS12/GPI12 to RS15/GPI15.                                                                                                                                                    |
| 35   | N.C.   | —      | No Internal Connection                                                                                                                                                                                                        |
| 36   | RSG1   | AI     | Remote-Sense Ground for RS4/GPI4 to RS11/GPI11.                                                                                                                                                                               |
| 37   | N.C.   | —      | No Internal Connection                                                                                                                                                                                                        |
| 38   | PSEN0  | DO     | Power-Supply Enable 0. See the <i>Expanded Pin Description</i> section for more details.                                                                                                                                      |
|      | GPO0   | DO     | General-Purpose Output 0                                                                                                                                                                                                      |
| 39   | PSEN1  | DO     | Power-Supply Enable 1. See the <i>Expanded Pin Description</i> section for more details.                                                                                                                                      |
|      | GPO1   | DO     | General-Purpose Output 1                                                                                                                                                                                                      |
| 40   | PSEN2  | DO     | Power-Supply Enable 2. See the <i>Expanded Pin Description</i> section for more details.                                                                                                                                      |
|      | GPO2   | DO     | General-Purpose Output 2                                                                                                                                                                                                      |
| 41   | PSEN3  | DO     | Power-Supply Enable 3. See the <i>Expanded Pin Description</i> section for more details.                                                                                                                                      |
|      | GPO3   | DO     | General-Purpose Output 3                                                                                                                                                                                                      |
| 42   | PSEN4  | DO     | Power-Supply Enable 4. See the <i>Expanded Pin Description</i> section for more details.                                                                                                                                      |
|      | GPO4   | DO     | General-Purpose Output 4                                                                                                                                                                                                      |
| 43   | PSEN5  | DO     | Power-Supply Enable 5. See the <i>Expanded Pin Description</i> section for more details.                                                                                                                                      |
|      | GPO5   | DO     | General-Purpose Output 5                                                                                                                                                                                                      |
| 44   | PSEN6  | DO     | Power-Supply Enable 6. See the <i>Expanded Pin Description</i> section for more details.                                                                                                                                      |
|      | GPO6   | DO     | General-Purpose Output 6                                                                                                                                                                                                      |
| 45   | PSEN7  | DO     | Power-Supply Enable 7. See the <i>Expanded Pin Description</i> section for more details.                                                                                                                                      |
|      | GPO7   | DO     | General-Purpose Output 7                                                                                                                                                                                                      |
| 46   | PSEN8  | DO     | Power-Supply Enable 8. See the <i>Expanded Pin Description</i> section for more details.                                                                                                                                      |
|      | GPO8   | DO     | General-Purpose Output 8                                                                                                                                                                                                      |
| 47   | RS13   | AI     | ADC Voltage-Sense Input 13. Connect to V <sub>SS</sub> if unused.                                                                                                                                                             |
|      | GPI13  | AI     | General-Purpose Input 13. Connect to V <sub>SS</sub> if unused.                                                                                                                                                               |
| 48   | PSEN9  | DO     | Power-Supply Enable 9. See the <i>Expanded Pin Description</i> section for more details.                                                                                                                                      |
|      | GPO9   | DO     | General-Purpose Output 9                                                                                                                                                                                                      |

## Pin Description (continued)

| PIN* | NAME               | TYPE** | FUNCTION                                                                                                                                            |
|------|--------------------|--------|-----------------------------------------------------------------------------------------------------------------------------------------------------|
| 49   | RS12               | AI     | ADC Voltage-Sense Input 12. Connect to V <sub>SS</sub> if unused.                                                                                   |
|      | GPI12              | AI     | General-Purpose Input 12. Connect to V <sub>SS</sub> if unused.                                                                                     |
| 50   | RS11               | AI     | ADC Voltage-Sense Input 11. Connect to V <sub>SS</sub> if unused.                                                                                   |
|      | GPI11              | AI     | General-Purpose Input 11. Connect to V <sub>SS</sub> if unused.                                                                                     |
| 51   | RS10               | AI     | ADC Voltage-Sense Input 10. Connect to V <sub>SS</sub> if unused.                                                                                   |
|      | GPI10              | AI     | General-Purpose Input 10. Connect to V <sub>SS</sub> if unused.                                                                                     |
| 52   | RS9                | AI     | ADC Voltage-Sense Input 9. Connect to V <sub>SS</sub> if unused.                                                                                    |
|      | GPI9               | AI     | General-Purpose Input 9. Connect to V <sub>SS</sub> if unused.                                                                                      |
| 53   | RS8                | AI     | ADC Voltage-Sense Input 8. Connect to V <sub>SS</sub> if unused.                                                                                    |
|      | GPI8               | AI     | General-Purpose Input 8. Connect to V <sub>SS</sub> if unused.                                                                                      |
| 54   | RS7                | AI     | ADC Voltage-Sense Input 7. Connect to V <sub>SS</sub> if unused.                                                                                    |
|      | GPI7               | AI     | General-Purpose Input 7. Connect to V <sub>SS</sub> if unused.                                                                                      |
| 55   | RS6                | AI     | ADC Voltage-Sense Input 6. Connect to V <sub>SS</sub> if unused.                                                                                    |
|      | GPI6               | AI     | General-Purpose Input 6. Connect to V <sub>SS</sub> if unused.                                                                                      |
| 56   | RS5                | AI     | ADC Voltage-Sense Input 5. Connect to V <sub>SS</sub> if unused.                                                                                    |
|      | GPI5               | AI     | General-Purpose Input 5. Connect to V <sub>SS</sub> if unused.                                                                                      |
| —    | EP/V <sub>SS</sub> | Power  | Exposed Pad (Bottom Side of Package). Must be connected to local ground. The exposed pad is the ground reference (V <sub>SS</sub> ) for the device. |

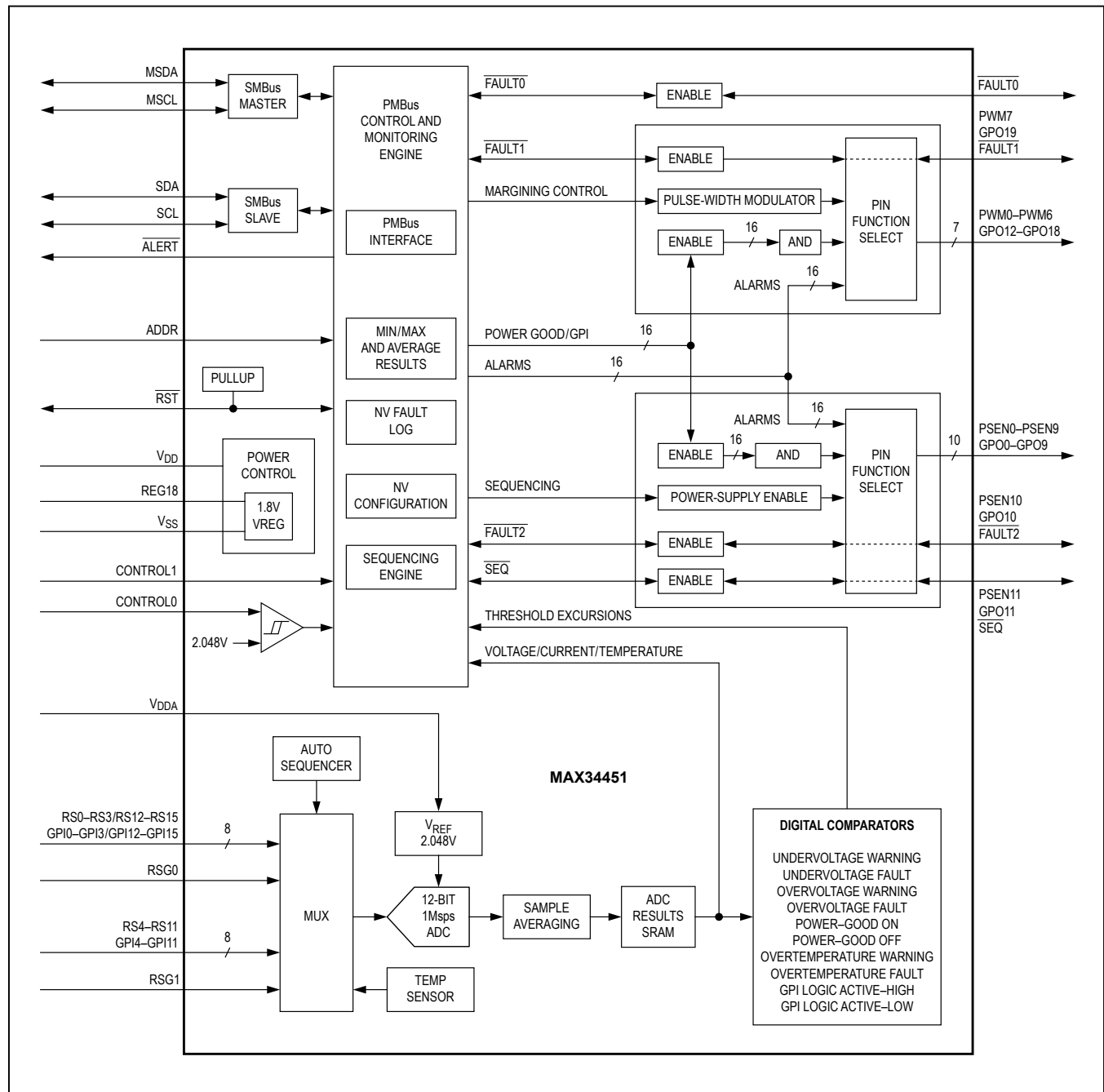
\*All pins except the power pins,  $\overline{\text{ALERT}}$ , and  $\overline{\text{ADDR}}$  are high impedance during device power-up and reset.

\*\*AI = Analog input, AO = Analog output, DI = Digital input, DIO = Digital input/output, and DO = Digital output.

## Expanded Pin Description

| PIN                                                     | FUNCTION                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
|---------------------------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| PSEN0–PSEN11                                            | The PSEN0–PSEN11 outputs are programmable with the MFR_PSEN_CONFIG command for either active-high or active-low operation and can be either open drain or push-pull. If not used for power-supply enables, these outputs can be repurposed as general-purpose outputs using the MFR_PSEN_CONFIG command. If these pins are used to enable power supplies, it is <b>highly recommended</b> that they have external pullups or pulldowns to force the supplies into an off state when the device is not active.                                                                                                                                                                                                                                                                                                                             |
| PWM0–PWM7                                               | The PWM0–PWM7 outputs are high impedance when the margining is disabled. A 100% duty cycle implies the pins are continuously high. If not used for margining, these pins can be repurposed as general-purpose outputs with the MFR_PWM_CONFIG command.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
| $\overline{\text{FAULT0}}$ – $\overline{\text{FAULT2}}$ | The $\overline{\text{FAULT0}}$ – $\overline{\text{FAULT2}}$ pins operate independently. Any global channel can be enabled with the MFR_FAULT_RESPONSE command to assert one or more of the $\overline{\text{FAULTn}}$ signals. Also, each global channel can be enabled to shut down when one or more of the $\overline{\text{FAULTn}}$ signals asserts. These pins are used to provide hardware control for power supplies across multiple devices. These outputs are unconditionally deasserted while $\overline{\text{RST}}$ is asserted or the device is power cycled. After device reset and upon device power-up, these outputs are pulled low immediately after program recall and held low until monitoring starts. Once monitoring starts, the $\overline{\text{FAULTn}}$ signals are released if no enabled faults are present. |

## Block Diagram



## Detailed Description

The MAX34451 is a highly integrated system monitor with functionality to monitor up to 16 different voltages or currents and to sequence and close-loop margin up to 12 power supplies. It also supports local and remote thermal sensing.

The power-supply manager monitors the power-supply output voltage and current and constantly checks for user-programmable overvoltage, undervoltage, and overcurrent thresholds. It also has the ability to margin the power-supply output voltage up or down by a user-programmable level. The margining is performed in a closed-loop arrangement, whereby the device automatically adjusts a PWM signal or an external current DAC

output and then measures the resultant output voltage. The power-supply manager can also sequence the supplies in any order at both power-up and power-down.

Thermal monitoring can be accomplished using up to five temperature sensors including an on-chip temperature sensor and up to four external remote DS75LV digital temperature sensors. Communications with the DS75LV temperature sensors is conducted through a dedicated I<sup>2</sup>C/SMBus interface.

The device provides  $\overline{\text{ALERT}}$  and  $\overline{\text{FAULTn}}$  output signals. Host communications are conducted through a PMBus-compatible communications port.

See [Table 1](#) and [Table 2](#) for more details on specific device operation.

**Table 1. PMBus PAGE to Pin/Resource Mapping**

| PMBus<br>PAGE | PIN NAME                               |                                       |     |                                                       |                                        |     |                                                           |                                        |     |
|---------------|----------------------------------------|---------------------------------------|-----|-------------------------------------------------------|----------------------------------------|-----|-----------------------------------------------------------|----------------------------------------|-----|
|               | RSn/GPI <sub>n</sub><br>(16 AVAILABLE) |                                       |     | PSEn <sub>n</sub> /GPO <sub>n</sub><br>(12 AVAILABLE) |                                        |     | PWM <sub>n</sub> /GPO <sub>n</sub><br>(8 AVAILABLE)       |                                        |     |
|               | VOLTAGE<br>OR<br>CURRENT<br>MONITOR    | GENERAL-<br>PURPOSE<br>INPUT<br>(GPI) | PIN | POWER-<br>SUPPLY<br>ENABLE<br>(PSEN)                  | GENERAL-<br>PURPOSE<br>OUTPUT<br>(GPO) | PIN | PWM<br>MARGIN<br>OUTPUT<br>(PWM)                          | GENERAL-<br>PURPOSE<br>OUTPUT<br>(GPO) | PIN |
| 0             | RS0                                    | GPI0                                  | 5   | PSEN0                                                 | GPO0                                   | 38  | PWM0                                                      | GPO12                                  | 24  |
| 1             | RS1                                    | GPI1                                  | 4   | PSEN1                                                 | GPO1                                   | 39  | PWM1                                                      | GPO13                                  | 25  |
| 2             | RS2                                    | GPI2                                  | 3   | PSEN2                                                 | GPO2                                   | 40  | PWM2                                                      | GPO14                                  | 26  |
| 3             | RS3                                    | GPI3                                  | 2   | PSEN3                                                 | GPO3                                   | 41  | PWM3                                                      | GPO15                                  | 27  |
| 4             | RS4                                    | GPI4                                  | 1   | PSEN4                                                 | GPO4                                   | 42  | PWM4                                                      | GPO16                                  | 28  |
| 5             | RS5                                    | GPI5                                  | 56  | PSEN5                                                 | GPO5                                   | 43  | PWM5                                                      | GPO17                                  | 29  |
| 6             | RS6                                    | GPI6                                  | 55  | PSEN6                                                 | GPO6                                   | 44  | PWM6                                                      | GPO18                                  | 32  |
| 7             | RS7                                    | GPI7                                  | 54  | PSEN7                                                 | GPO7                                   | 45  | PWM7                                                      | GPO19                                  | 33  |
| 8             | RS8                                    | GPI8                                  | 53  | PSEN8                                                 | GPO8                                   | 46  | Margin capability provided through<br>the external DS4424 |                                        |     |
| 9             | RS9                                    | GPI9                                  | 52  | PSEN9                                                 | GPO9                                   | 48  |                                                           |                                        |     |
| 10            | RS10                                   | GPI10                                 | 51  | PSEN10                                                | GPO10                                  | 19  |                                                           |                                        |     |
| 11            | RS11                                   | GPI11                                 | 50  | PSEN11                                                | GPO11                                  | 13  |                                                           |                                        |     |
| 12            | RS12                                   | GPI12                                 | 49  | Can monitor voltage or current or be assigned as GPI  |                                        |     |                                                           |                                        |     |
| 13            | RS13                                   | GPI13                                 | 47  |                                                       |                                        |     |                                                           |                                        |     |
| 14            | RS14                                   | GPI14                                 | 20  |                                                       |                                        |     |                                                           |                                        |     |
| 15            | RS15                                   | GPI15                                 | 14  |                                                       |                                        |     |                                                           |                                        |     |

**Table 2. Device Channel Capabilities and Options**

| MAX34451<br>CHANNEL | PMBus<br>COMMAND<br>PAGE | CHANNEL CAPABILITIES                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
|---------------------|--------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0–7                 | 0–7                      | <p><b>Voltage Monitor/Sequence/Margin/GPO Option:</b><br/>Pins RSn/GPIIn, PSEnN, and PWMn (where n = 0–7) have a one-to-one association for each channel that monitors for voltage (RSn) and can be used to sequence (PSEnN) and margin (PWMn) the power supply. The voltage monitored on this channel can also be configured to determine a power-good state. If not required for either sequencing or margining, the associated PSEnN and PWMn outputs can be repurposed as GPOn outputs that can either indicate a logic combination of power-good (PG) and GPI states or report alarms.</p> <p><b>Current Monitor/GPO Option:</b><br/>If the RSn/GPIIn input is used to monitor current, then the channel is not used to sequence or margin. The associated PSEnN and PWMn outputs can be repurposed as GPOn outputs that can either indicate a logic combination of power-good (PG) and GPI states or report alarms.</p> <p><b>GPI/GPO Option:</b><br/>If the RSn/GPIIn input is configured as a general-purpose input (GPI), it can be used as a term in a logic combination to determine a power-good (PG) state and assert a GPOn output or act as a condition to allow a power supply to be enabled. The associated PSEnN and PWMn outputs can be repurposed as GPOn outputs that can indicate power-good (PG) states or report alarms.</p> |
| 8–11                | 8–11                     | <p><b>Same as Channels 0–7 Except No PWM Outputs:</b><br/>Pins RSn/GPIIn, and PSEnN (where n = 8–11) are the same as channels 0–7, except the PWMn outputs for these channels do not exist and instead the device uses an external DS4424 current DAC (connected to the master I<sup>2</sup>C local bus) to margin the power supplies. These channels can also be used to monitor current or be used as GPIIn inputs just like channels 0–7.</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
| 12–15               | 12–15                    | <p>Pins RSn/GPIIn (where n = 12–15) cannot be used to control sequencing or for margining.</p> <p><b>Voltage Monitor Option:</b><br/>Monitor voltage including channel power-good (PG) and can also be configured to shut down one or more power supplies if a fault occurs.</p> <p><b>Current Monitor Option:</b><br/>Monitor current and can be configured to shut down one or more power supplies if a fault occurs.</p> <p><b>GPI Option:</b><br/>As a general-purpose input (GPI), can be used as a term in a logic combination to determine a power-good (PG) state and assert a GPOn output or act as a condition to allow a power supply to be enabled.</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |

Table 3. PMBus Command Codes

| CODE | COMMAND NAME        | TYPE      | PAGE     |       |       |     | NO. OF BYTES | FLASH STORED/<br>LOCKED<br>(NOTE 2) | DEFAULT VALUE<br>(NOTE 2) |
|------|---------------------|-----------|----------|-------|-------|-----|--------------|-------------------------------------|---------------------------|
|      |                     |           | 0–11     | 12–15 | 16–20 | 255 |              |                                     |                           |
|      |                     |           | (NOTE 1) |       |       |     |              |                                     |                           |
| 00h  | PAGE                | R/W byte  | R/W      | R/W   | R/W   | R/W | 1            | N/N                                 | 00h                       |
| 01h  | OPERATION           | R/W byte  | R/W      |       |       | W   | 1            | N/N                                 | 00h                       |
| 02h  | ON_OFF_CONFIG       | R/W byte  | R/W      | R/W   | R/W   | R/W | 1            | Y/Y                                 | 1Ah                       |
| 03h  | CLEAR_FAULTS        | Send byte | W        | W     | W     | W   | 0            | N/N                                 | —                         |
| 10h  | WRITE_PROTECT       | R/W byte  | R/W      | R/W   | R/W   | R/W | 1            | N/Y                                 | 00h                       |
| 11h  | STORE_DEFAULT_ALL   | Send byte | W        | W     | W     | W   | 0            | N/Y                                 | —                         |
| 12h  | RESTORE_DEFAULT_ALL | Send byte | W        | W     | W     | W   | 0            | N/Y                                 | —                         |
| 19h  | CAPABILITY          | Read byte | R        | R     | R     | R   | 1            | N/N                                 | 20h/30h                   |
| 20h  | VOUT_MODE           | Read byte | R        | R     | R     | R   | 1            | FIXED/N                             | 40h                       |
| 25h  | VOUT_MARGIN_HIGH    | R/W word  | R/W      | —     | —     | —   | 2            | Y/Y                                 | 0000h                     |
| 26h  | VOUT_MARGIN_LOW     | R/W word  | R/W      | —     | —     | —   | 2            | Y/Y                                 | 0000h                     |
| 2Ah  | VOUT_SCALE_MONITOR  | R/W word  | R/W      | R/W   | —     | —   | 2            | Y/Y                                 | 7FFFh                     |
| 38h  | IOUT_CAL_GAIN       | R/W word  | R/W      | R/W   | —     | —   | 2            | Y/Y                                 | 0000h                     |
| 40h  | VOUT_OV_FAULT_LIMIT | R/W word  | R/W      | R/W   | —     | —   | 2            | Y/Y                                 | 7FFFh                     |
| 42h  | VOUT_OV_WARN_LIMIT  | R/W word  | R/W      | R/W   | —     | —   | 2            | Y/Y                                 | 7FFFh                     |
| 43h  | VOUT_UV_WARN_LIMIT  | R/W word  | R/W      | R/W   | —     | —   | 2            | Y/Y                                 | 0000h                     |
| 44h  | VOUT_UV_FAULT_LIMIT | R/W word  | R/W      | R/W   | —     | —   | 2            | Y/Y                                 | 0000h                     |
| 46h  | IOUT_OC_WARN_LIMIT  | R/W word  | R/W      | R/W   | —     | —   | 2            | Y/Y                                 | 7FFFh                     |
| 4Ah  | IOUT_OC_FAULT_LIMIT | R/W word  | R/W      | R/W   | —     | —   | 2            | Y/Y                                 | 7FFFh                     |
| 4Fh  | OT_FAULT_LIMIT      | R/W word  | —        | —     | R/W   | —   | 2            | Y/Y                                 | 7FFFh                     |
| 51h  | OT_WARN_LIMIT       | R/W word  | —        | —     | R/W   | —   | 2            | Y/Y                                 | 7FFFh                     |
| 5Eh  | POWER_GOOD_ON       | R/W word  | R/W      | R/W   | —     | —   | 2            | Y/Y                                 | 0000h                     |
| 5Fh  | POWER_GOOD_OFF      | R/W word  | R/W      | R/W   | —     | —   | 2            | Y/Y                                 | 0000h                     |
| 60h  | TON_DELAY           | R/W word  | R/W      | —     | —     | —   | 2            | Y/Y                                 | 0000h                     |
| 62h  | TON_MAX_FAULT_LIMIT | R/W word  | R/W      | —     | —     | —   | 2            | Y/Y                                 | FFFFh                     |
| 64h  | TOFF_DELAY          | R/W word  | R/W      | —     | —     | —   | 2            | Y/Y                                 | 0000h                     |
| 79h  | STATUS_WORD         | Read word | R        | R     | R     | R   | 2            | N/N                                 | 0000h                     |
| 7Ah  | STATUS_VOUT         | Read byte | R        | R     | —     | —   | 1            | N/N                                 | 00h                       |
| 7Bh  | STATUS_IOUT         | Read byte | R        | R     | —     | —   | 1            | N/N                                 | 00h                       |

Table 3. PMBus Command Codes (continued)

| CODE | COMMAND NAME            | TYPE       | PAGE     |       |       |     | NO. OF BYTES | FLASH STORED/ LOCKED (NOTE 2) | DEFAULT VALUE (NOTE 2) |
|------|-------------------------|------------|----------|-------|-------|-----|--------------|-------------------------------|------------------------|
|      |                         |            | 0–11     | 12–15 | 16–20 | 255 |              |                               |                        |
|      |                         |            | (NOTE 1) |       |       |     |              |                               |                        |
| 7Dh  | STATUS_TEMPERATURE      | Read byte  | —        | —     | R     | —   | 1            | N/N                           | 00h                    |
| 7Eh  | STATUS_CML              | Read byte  | R        | R     | R     | R   | 1            | N/N                           | 00h                    |
| 80h  | STATUS_MFR_SPECIFIC     | Read byte  | R        | R     | —     | R   | 1            | N/N                           | 00h                    |
| 8Bh  | READ_VOUT               | Read word  | R        | R     | —     | —   | 2            | N/N                           | 0000h                  |
| 8Ch  | READ_IOUT               | Read word  | R        | R     | —     | —   | 2            | N/N                           | 0000h                  |
| 8Dh  | READ_TEMPERATURE_1      | Read word  | —        | —     | R     | —   | 2            | N/N                           | 0000h                  |
| 98h  | PMBUS_REVISION          | Read byte  | R        | R     | R     | R   | 1            | FIXED/N                       | 11h                    |
| 99h  | MFR_ID                  | Read byte  | R        | R     | R     | R   | 1            | FIXED/N                       | 4Dh                    |
| 9Ah  | MFR_MODEL               | Read byte  | R        | R     | R     | R   | 1            | FIXED/N                       | 59h                    |
| 9Bh  | MFR_REVISION            | Read word  | R        | R     | R     | R   | 2            | FIXED/N                       | (Note 3)               |
| 9Ch  | MFR_LOCATION            | Block R/W  | R/W      | R/W   | R/W   | R/W | 8            | Y/Y                           | (Note 4)               |
| 9Dh  | MFR_DATE                | Block R/W  | R/W      | R/W   | R/W   | R/W | 8            | Y/Y                           | (Note 4)               |
| 9Eh  | MFR_SERIAL              | Block R/W  | R/W      | R/W   | R/W   | R/W | 8            | Y/Y                           | (Note 4)               |
| D1h  | MFR_MODE                | Block R/W  | R/W      | R/W   | R/W   | R/W | 2            | Y/Y                           | 0020h                  |
| D2h  | MFR_PSEN_CONFIG         | Block R/W  | R/W      | —     | —     | —   | 4            | Y/Y                           | (Note 5)               |
| D4h  | MFR_VOUT_PEAK           | R/W word   | R/W      | R/W   | —     | —   | 2            | N/Y                           | 0000h                  |
| D5h  | MFR_IOUT_PEAK           | R/W word   | R/W      | R/W   | —     | —   | 2            | N/Y                           | 0000h                  |
| D6h  | MFR_TEMPERATURE_PEAK    | R/W word   | —        | —     | R/W   | —   | 2            | N/Y                           | 8000h                  |
| D7h  | MFR_VOUT_MIN            | R/W word   | R/W      | R/W   | —     | —   | 2            | N/Y                           | 7FFFh                  |
| D8h  | MFR_NV_LOG_CONFIG       | R/W word   | R/W      | R/W   | R/W   | R/W | 2            | Y/Y                           | 0000h                  |
| D9h  | MFR_FAULT_RESPONSE      | Block R/W  | R/W      | R/W   |       |     | 4            | Y/Y                           | (Note 5)               |
| DAh  | MFR_FAULT_RETRY         | R/W word   | R/W      | R/W   | R/W   | R/W | 2            | Y/Y                           | 0000h                  |
| DCh  | MFR_NV_FAULT_LOG        | Block read | R        | R     | R     | R   | 255          | Y/Y                           | (Note 6)               |
| DDh  | MFR_TIME_COUNT          | Block R/W  | R/W      | R/W   | R/W   | R/W | 4            | N/Y                           | (Note 5)               |
| DFh  | MFR_MARGIN_CONFIG       | R/W word   | R/W      | —     | —     | —   | 2            | Y/Y                           | 0000h                  |
| E2h  | MFR_IOUT_AVG            | R/W word   | R        | R     | —     | —   | 2            | N/Y                           | 0000h                  |
| E4h  | MFR_CHANNEL_CONFIG      | R/W word   | R/W      | R/W   | —     | —   | 2            | Y/Y                           | 0000h                  |
| E6h  | MFR_TON_SEQ_MAX         | R/W word   | R/W      | —     | —     | —   | 2            | Y/Y                           | 0000h                  |
| E7h  | MFR_PWM_CONFIG (Note 7) | Block R/W  | R/W      | —     | —     | —   | 4            | Y/Y                           | (Note 5)               |

**Table 3. PMBus Command Codes (continued)**

| CODE | COMMAND NAME           | TYPE       | PAGE     |       |       |     | NO. OF BYTES | FLASH STORED/ LOCKED (NOTE 2) | DEFAULT VALUE (NOTE 2) |
|------|------------------------|------------|----------|-------|-------|-----|--------------|-------------------------------|------------------------|
|      |                        |            | 0–11     | 12–15 | 16–20 | 255 |              |                               |                        |
|      |                        |            | (NOTE 1) |       |       |     |              |                               |                        |
| E8h  | MFR_SEQ_CONFIG         | Block R/W  | R/W      | —     | —     | —   | 4            | Y/Y                           | (Note 5)               |
| EEh  | MFR_STORE_ALL          | Write byte | W        | W     | W     | W   | 1            | N/Y                           | —                      |
| EFh  | MFR_RESTORE_ALL        | Write byte | W        | W     | W     | W   | 1            | N/Y                           | —                      |
| F0h  | MFR_TEMP_SENSOR_CONFIG | R/W word   | —        | —     | R/W   | —   | 2            | Y/Y                           | 0000h                  |
| FCh  | MFR_STORE_SINGLE       | R/W word   | R/W      | R/W   | R/W   | R/W | 2            | N/Y                           | 0000h                  |
| FEh  | MFR_CRC                | R/W word   | R/W      | R/W   | R/W   | R/W | 2            | N/Y                           | FFFFh                  |

**Note 1:** Common commands are shaded; access through any page results in the same device response.

**Note 2:** In the **Flash Stored/Locked** column, the “N” on the left indicates that this parameter is not stored in flash memory when the STORE\_DEFAULT\_ALL or MFR\_STORE\_ALL command is executed; the value shown in the **Default Value** column is automatically loaded upon power-on reset or when the RST pin is asserted. The “Y” on the left in the **Flash Stored/Locked** column indicates that the currently loaded value in this parameter is stored in flash memory when the STORE\_DEFAULT\_ALL or MFR\_STORE\_ALL command is executed and is automatically loaded upon power-on reset or when the RST pin is asserted; the value shown in the **Default Value** column is the value when shipped from the factory. “FIXED” in the **Flash Stored** column means that the value is fixed at the factory and cannot be changed. The value shown in the **Default Value** column is automatically loaded upon power-on reset or when the RST pin is asserted. The right-side Y/N indicates that when the device is locked, only the commands listed with “N” can be accessed. All other commands are ignored if written and return FFh if read. Only the PAGE, CLEAR\_FAULTS, OPERATION, and MFR\_SERIAL commands can be written to. The device unlocks if the upper 4 bytes of MFR\_SERIAL match the data written to the device.

**Note 3:** The factory-set value is dependent on the device hardware and firmware revision.

**Note 4:** The factory-set default value for this 8-byte block is 3130313031303130h.

**Note 5:** The factory-set default value for this 4-byte block is 00000000h.

**Note 6:** The factory-set default value for the complete block of the MFR\_NV\_FAULT\_LOG is FFh.

**Note 7:** MFR\_PWM\_CONFIG is only available for PAGES 0–7.

### PMBus/SMBus Address Select

On device power-up, the device samples the ADDR pin to determine the PMBus/SMBus serial-port address. The combination of the components shown in [Figure 1](#) determines the serial-port address (also see [Table 4](#)).

### SMBus/PMBus Operation

The device implements the PMBus command structure using the SMBus format. The structure of the data flow between the host and the slave is shown below for several different types of transactions. All transactions begin with a host sending a command code that is immediately preceded with a 7-bit slave address (R/W = 0). Data is sent MSB first.

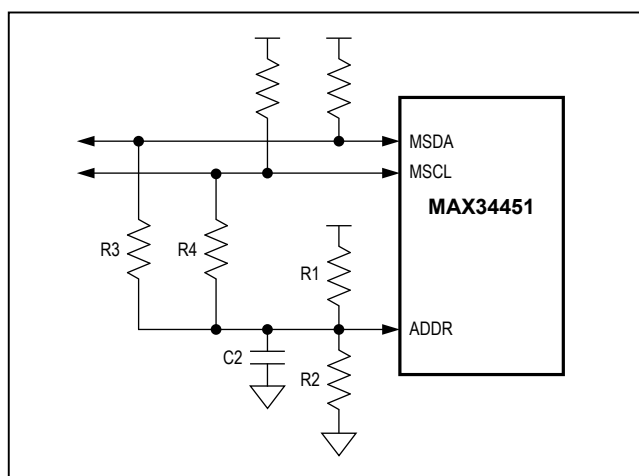


Figure 1. PMBus/SMBus Address Select



**Table 4. PMBus/SMBus Serial-Port Address**

| R1    | R2    | R3    | R4    | C2    | 7-BIT SLAVE ADDRESS |
|-------|-------|-------|-------|-------|---------------------|
| —     | 220kΩ | —     | —     | —     | 1110 100 (E8h)      |
| 220kΩ | —     | —     | —     | —     | 1110 101 (EAh)      |
| 220kΩ | —     | —     | —     | 100nF | 0010 010 (24h)      |
| 22kΩ  | —     | —     | —     | 100nF | 0010 011 (26h)      |
| —     | —     | 0kΩ   | —     | —     | 1001 100 (98h)      |
| —     | —     | 220kΩ | —     | —     | 1001 101 (9Ah)      |
| —     | —     | —     | 0kΩ   | —     | 1011 000 (B0h)      |
| —     | —     | —     | 220kΩ | —     | 1011 001 (B2h)      |
| —     | 0kΩ   | —     | —     | —     | 1001 110 (9Ch)      |

**Note:** The device also responds to a slave address of 34h (this is the factory programming address); the device should not share the same I<sup>2</sup>C bus with other devices that use this slave address.

**SMBus/PMBus Operation Examples****READ WORD FORMAT**

|   |               |   |   |              |   |    |               |   |   |               |   |                |    |   |
|---|---------------|---|---|--------------|---|----|---------------|---|---|---------------|---|----------------|----|---|
| 1 | 7             | 1 | 1 | 8            | 1 | 1  | 7             | 1 | 1 | 8             | 1 | 8              | 1  | 1 |
| S | SLAVE ADDRESS | W | A | COMMAND CODE | A | Sr | SLAVE ADDRESS | R | A | DATA BYTE LOW | A | DATA BYTE HIGH | NA | P |

**READ BYTE FORMAT**

|   |               |   |   |              |   |    |               |   |   |           |    |   |
|---|---------------|---|---|--------------|---|----|---------------|---|---|-----------|----|---|
| 1 | 7             | 1 | 1 | 8            | 1 | 1  | 7             | 1 | 1 | 8         | 1  | 1 |
| S | SLAVE ADDRESS | W | A | COMMAND CODE | A | Sr | SLAVE ADDRESS | R | A | DATA BYTE | NA | P |

**WRITE WORD FORMAT**

|   |               |   |   |              |   |               |   |                |   |   |
|---|---------------|---|---|--------------|---|---------------|---|----------------|---|---|
| 1 | 7             | 1 | 1 | 8            | 1 | 8             | 1 | 8              | 1 | 1 |
| S | SLAVE ADDRESS | W | A | COMMAND CODE | A | DATA BYTE LOW | A | DATA BYTE HIGH | A | P |

**WRITE BYTE FORMAT**

|   |               |   |   |              |   |           |   |   |
|---|---------------|---|---|--------------|---|-----------|---|---|
| 1 | 7             | 1 | 1 | 8            | 1 | 8         | 1 | 1 |
| S | SLAVE ADDRESS | W | A | COMMAND CODE | A | DATA BYTE | A | P |

**SEND BYTE FORMAT**

|   |               |   |   |              |   |   |
|---|---------------|---|---|--------------|---|---|
| 1 | 7             | 1 | 1 | 8            | 1 | 1 |
| S | SLAVE ADDRESS | W | A | COMMAND CODE | A | P |

**KEY:**

S = START

Sr = REPEATED START

P = STOP

W = WRITE BIT (0)

R = READ BIT (1)

A = ACKNOWLEDGE (0)

NA = NOT ACKNOWLEDGE (1)

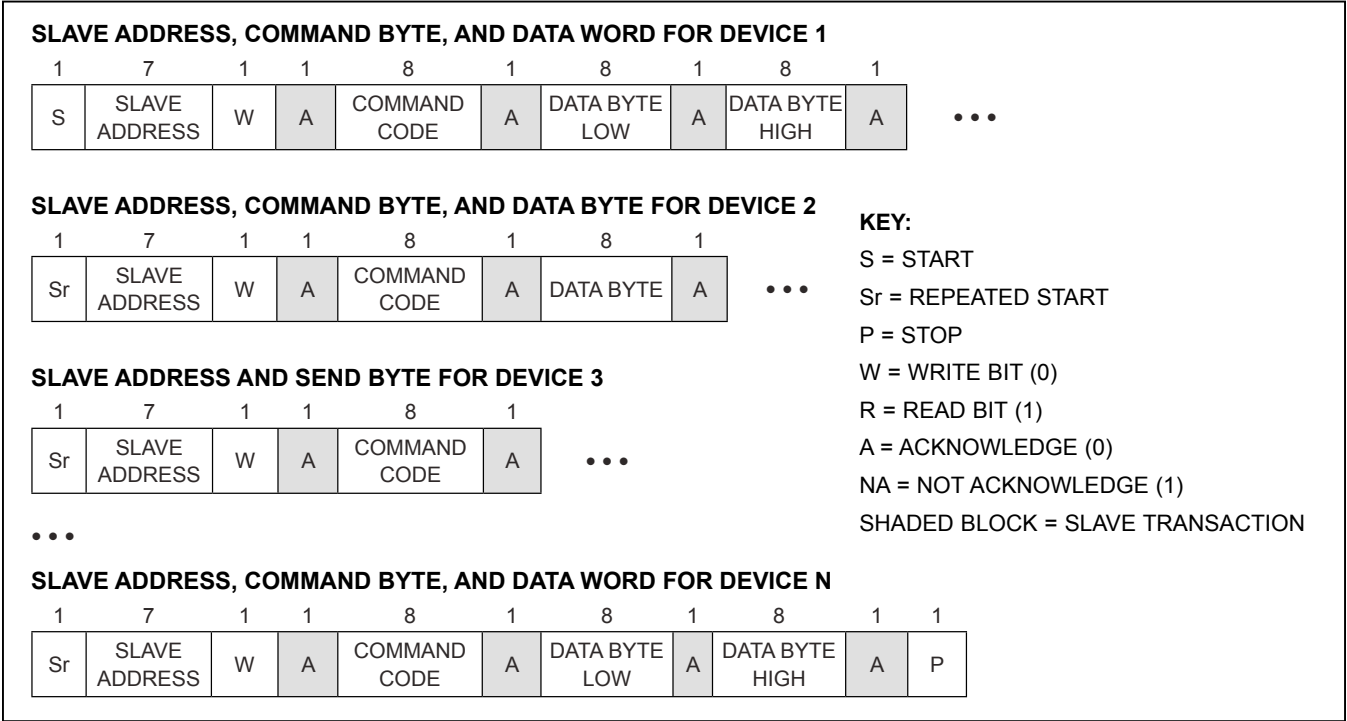
SHADED BLOCK = SLAVE TRANSACTION

Group Command

The device supports the group command. With the group command, a host can write different data to multiple

devices on the same serial bus with one long continuous data stream. All the devices addressed during this transaction wait for the host to issue a STOP before beginning to respond to the command.

Group Command Write Format



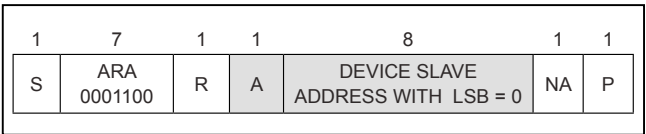
Addressing

The device responds to receiving its fixed slave address by asserting an acknowledge (ACK) on the bus. The device does not respond to a general call address; it only responds when it receives its fixed slave address or the alert response address. See the *ALERT and Alert Response Address (ARA)* section for more details.

ALERT and Alert Response Address (ARA)

If the  $\overline{\text{ALERT}}$  output is enabled (ALERT bit = 1 in MFR\_MODE) when a fault occurs, the device asserts the  $\overline{\text{ALERT}}$  signal and then waits for the host to send an ARA, as shown in the *Alert Response Address (ARA) Byte Format* section.

Alert Response Address (ARA) Byte Format



When the ARA is received and the device is asserting  $\overline{\text{ALERT}}$ , the device ACKs it and then attempts to place its fixed slave address on the bus by arbitrating the bus, since another device could also try to respond to the ARA. The rules of arbitration state that the lowest address device wins. If the device wins the arbitration, it deasserts  $\overline{\text{ALERT}}$ . If the device loses arbitration, it keeps  $\overline{\text{ALERT}}$  asserted and waits for the host to once again send the ARA.

**Host Sends or Reads Too Few Bits**

If, for any reason, the host does not complete writing a full byte or reading a full byte from the device before a START or STOP is received, the device does the following:

- 1) Ignores the command.
- 2) Sets the CML bit in STATUS\_WORD.
- 3) Sets the DATA\_FAULT bit in STATUS\_CML.
- 4) Notifies the host through  $\overline{\text{ALERT}}$  assertion (if enabled).

**Host Sends or Reads Too Few Bytes**

For each supported command, the device expects a fixed number of bytes to be written to or read from the device. If, for any reason, less than the expected number of bytes are written to or read from the device, the device completely ignores the command and takes no action.

**Host Sends Too Many Bytes or Bits**

For each supported command, the device expects a fixed number of bytes to be written to the device. If for any reason, more than the expected number of bytes or bits is written to the device, the device does the following:

- 1) Ignores the command.
- 2) Sets the CML bit in STATUS\_WORD.
- 3) Sets the DATA\_FAULT bit in STATUS\_CML.
- 4) Notifies the host through  $\overline{\text{ALERT}}$  assertion (if enabled).

**Host Reads Too Many Bytes or Bits**

For each supported command, the device expects a fixed number of bytes to be read from the device. If, for any reason, more than the expected number of bytes or bits is read from the device, the device does the following:

- 1) Sends all ones (FFh) as long as the host keeps acknowledging.
- 2) Sets the CML bit in STATUS\_WORD.
- 3) Sets the DATA\_FAULT bit in STATUS\_CML.
- 4) Notifies the host through  $\overline{\text{ALERT}}$  assertion (if enabled).

**Host Sends Improperly Set Read Bit in the Slave Address Byte**

If the device receives the R/ $\overline{\text{W}}$  bit in the slave address set to a one immediately preceding the command code, the device does the following (this does not apply to the ARA):

- 1) ACKs the address byte.
- 2) Sends all ones (FFh) as long as the host keeps acknowledging.

- 3) Sets the CML bit in STATUS\_WORD.
- 4) Sets the DATA\_FAULT bit in STATUS\_CML.
- 5) Notifies the host through  $\overline{\text{ALERT}}$  assertion (if enabled).

**Unsupported Command Code Received/Host Writes to a Read-Only Command**

If the host sends the device a command code that it does not support, or if the host sends a command code that is not supported by the current PAGE setting, the device does the following:

- 1) Ignores the command.
- 2) Sets the CML bit in STATUS\_WORD.
- 3) Sets the COMM\_FAULT bit in STATUS\_CML.
- 4) Notifies the host through  $\overline{\text{ALERT}}$  assertion (if enabled).

**Invalid Data Received**

The device checks the PAGE, OPERATION, and WRITE\_PROTECT command codes for valid data. If the host writes a data value that is invalid, the device does the following:

- 1) Ignores the command.
- 2) Sets the CML bit in STATUS\_WORD.
- 3) Sets the DATA\_FAULT bit in STATUS\_CML.
- 4) Notifies the host through  $\overline{\text{ALERT}}$  assertion (if enabled).

**Host Reads from a Write-Only Command**

When a read request is issued to a write-only command (CLEAR\_FAULTS, STORE\_DEFAULT\_ALL, RESTORE\_DEFAULT\_ALL, MFR\_STORE\_ALL, MFR\_RESTORE\_ALL, OPERATION with PAGE = 255), the device does the following:

- 1) ACKs the address byte.
- 2) Ignores the command.
- 3) Sends all ones (FFh) as long as the host keeps acknowledging.
- 4) Sets the CML bit in STATUS\_WORD.
- 5) Sets the DATA\_FAULT bit in STATUS\_CML.
- 6) Notifies the host through  $\overline{\text{ALERT}}$  assertion (if enabled).

**SMBus Timeout**

If, during an active SMBus communication sequence, the SCL signal is held low for greater than the timeout duration (nominally 27ms), the device terminates the sequence and resets the serial bus. It takes no other action. No status bits are set.

## PMBus Operation

From a software perspective, the device appears as a PMBus device capable of executing a subset of PMBus commands. A PMBus 1.1-compliant device uses the SMBus version 1.1 for transport protocol and responds to the SMBus slave address. In this data sheet, the term SMBus is used to refer to the electrical characteristics of the PMBus communication using the SMBus physical layer. The term PMBus is used to refer to the PMBus command protocol. The device employs a number of standard SMBus protocols (e.g., Write Word, Read Word, Write Byte, Read Byte, Send Byte, etc.) to program output voltage and warning/fault thresholds, read monitored data, and provide access to all manufacturer-specific commands.

The device supports the group command. The group command is used to send commands to more than one PMBus device. It is not required that all the devices receive the same command. However, no more than one command can be sent to any one device in one group command packet. The group command must not be used with commands that require receiving devices to respond with data, such as the STATUS\_WORD command. When the device receives a command through this protocol, it immediately begins execution of the received command after detecting the STOP condition.

The device supports the PAGE command and uses it to select which individual channel to access. When a data word is transmitted, the lower order byte is sent first and the higher order byte is sent last. Within any byte, the most-significant bit (MSB) is sent first and the least-significant bit (LSB) is sent last.

## PMBus Protocol Support

The device supports a subset of the commands defined in the PMBus Power System Management Protocol Specification Part II - Command Language Revision 1.1.

For detailed specifications and the complete list of PMBus commands, refer to Part II of the PMBus specification available at [www.PMBus.org](http://www.PMBus.org). The supported PMBus commands and the corresponding device behavior are described in this document. All data values are represented in DIRECT format, unless otherwise stated. Whenever the PMBus specification refers to the PMBus device, it is referring to the device operating in conjunction with a power supply. While the command can call for turning on or off the PMBus device, the device always remains on to continue communicating with the PMBus master and transfers the command to the power supply accordingly.

## Data Format

Voltage data for commanding or reading the output voltage or related parameters (such as the overvoltage threshold) are presented in DIRECT format. DIRECT format data is a 2-byte, two's complement binary value. DIRECT format data can be used with any command that sends or reads a parametric value. The DIRECT format uses an equation and defined coefficients to calculate the desired values. [Table 5](#) lists coefficients used by the device.

## Interpreting Received DIRECT Format Values

The host system uses the following equation to convert the value received from the PMBus device—in this case the MAX34451—into a reading of volts, degrees Celsius, or other units as appropriate:

$$X = (1/m) \times (Y \times 10^{-R} - b)$$

where X is the calculated real-world value in the appropriate units (V, °C, etc.); m is the slope coefficient; Y is the 2-byte, two's complement integer received from the PMBus device; b is the offset; and R is the exponent.

**Table 5. PMBus Command Code Coefficients**

| PARAMETER       | COMMANDS                                                                                                                                                                                                       | UNITS | RESOLUTION | MAXIMUM | m     | b | R |
|-----------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------|------------|---------|-------|---|---|
| Voltage         | VOUT_MARGIN_HIGH<br>VOUT_MARGIN_LOW<br>VOUT_OV_FAULT_LIMIT<br>VOUT_OV_WARN_LIMIT<br>VOUT_UV_WARN_LIMIT<br>VOUT_UV_FAULT_LIMIT<br>POWER_GOOD_ON<br>POWER_GOOD_OFF<br>READ_VOUT<br>MFR_VOUT_PEAK<br>MFR_VOUT_MIN | mV    | 1          | 32767   | 1     | 0 | 0 |
| Voltage Scaling | VOUT_SCALE_MONITOR                                                                                                                                                                                             | —     | 1/32767    | 1       | 32767 | 0 | 0 |
| Current         | IOUT_OC_FAULT_LIMIT<br>IOUT_OC_WARN_LIMIT<br>READ_IOUT<br>MFR_IOUT_PEAK<br>MFR_IOUT_AVG                                                                                                                        | A     | 0.01       | 327.67  | 1     | 0 | 2 |
| Current Scaling | IOUT_CAL_GAIN                                                                                                                                                                                                  | mΩ    | 0.1        | 3276.7  | 1     | 0 | 1 |
| Temperature     | OT_FAULT_LIMIT<br>OT_WARN_LIMIT<br>READ_TEMPERATURE_1<br>MFR_TEMPERATURE_PEAK                                                                                                                                  | °C    | 0.01       | 327.67  | 1     | 0 | 2 |
| Timing          | TON_DELAY<br>TON_MAX_FAULT_LIMIT<br>TOFF_DELAY<br>MFR_FAULT_RETRY<br>MFR_TON_SEQ_MAX                                                                                                                           | ms    | 0.2        | 6553.4  | 5     | 0 | 0 |

**Sending a DIRECT Format Value**

To send a value, the host must use the following equation to solve for Y:

$$Y = (mX + b) \times 10^R$$

where Y is the 2-byte, two's complement integer to be sent to the unit; m is the slope coefficient; X is the real-world value, in units such as volts, to be converted for transmission; b is the offset; and R is the exponent.

The following example demonstrates how the host can send and retrieve values from the device. [Table 6](#) lists the coefficients used in the following parameters.

**Table 6. Coefficients for DIRECT Format Value**

| COMMAND CODE | COMMAND NAME     | m | b | R |
|--------------|------------------|---|---|---|
| 25h          | VOUT_MARGIN_HIGH | 1 | 0 | 0 |
| 8Bh          | READ_VOUT        | 1 | 0 | 0 |

If a host wants to set the device to change the power-supply output voltage to 3.465V (or 3465mV), the corresponding VOUT\_MARGIN\_HIGH value is:

$$Y = (1 \times 3465 + 0) \times 10^0 = 3465 \text{ (decimal)} \\ = 0D89h \text{ (hex)}$$

Conversely, if the host received a value of 0D89h on a READ\_VOUT command, this is equivalent to:

$$X = (1/1) \times (0D89h \times 10^{(-0)} - 0) = 3465mV = 3.465V$$

Power supplies and power converters generally have no way of knowing how their outputs are connected to ground. Within the power supply, all output voltages are most commonly treated as positive. Accordingly, all output voltages and output-voltage-related parameters of PMBus devices are commanded and reported as positive values. It is up to the system to know that a particular output is negative if that is of interest to the system. All output-voltage-related commands use 2 data bytes.

### Fault Management and Reporting

For reporting faults/warnings to the host on a real-time basis, the device asserts the open-drain  $\overline{ALERT}$  pin (if enabled in MFR\_MODE) and sets the appropriate bit in the various status registers. On recognition of the  $\overline{ALERT}$  assertion, the host or system manager is expected to poll the I<sup>2</sup>C bus to determine the device asserting  $\overline{ALERT}$ . The host sends the SMBus ARA (0001 100). The device ACKs the SMBus ARA, transmits its slave address, and deasserts  $\overline{ALERT}$ . The system controller then communicates with PMBus commands to retrieve the fault/warning status information from the device.

See the individual command sections for more details. Faults and warnings that are latched in the status registers are cleared when any one of the following conditions occur:

- A CLEAR\_FAULTS command is received.
- The  $\overline{RST}$  pin is toggled or a soft-reset is issued.

- Bias power to the device is removed and then reapplied.

One or more latched-off power supplies are only restarted when one of the following occurs:

- OPERATION commands are received that turn off and turn on the power supplies, or the CONTROL<sub>n</sub> pins are toggled to turn off and then turn on the power supplies.
- The  $\overline{RST}$  pin is toggled or a soft-reset is issued.
- Bias power to the device is removed and then reapplied.

The device responds to fault conditions according to the configuration of the MFR\_FAULT\_RESPONSE command. This command determines how the device should respond to each particular fault and whether it should assert one or more of the  $\overline{FAULT}_n$  pins when a fault occurs.

The MFR\_FAULT\_RESPONSE command also determines whether a channel should power up if a fault is present. With the RESPONSE bits in MFR\_FAULT\_RESPONSE, each channel can be independently configured to either respond or not respond to each possible fault. Before any power-supply channel is enabled, or the  $\overline{FAULT}_n$  outputs deasserted, the device checks for overvoltage, overcurrent, and temperature faults (but not for undervoltage) if the channel is configured for a fault response to either latchoff (RESPONSE[1:0] = 01) or retry (RESPONSE[1:0] = 10) in the MFR\_FAULT\_RESPONSE command. Only after the faults clear is the channel allowed to turn on. See [Table 7](#) for fault-monitoring states.

**Table 7. Fault-Monitoring States**

| FAULT           | REQUIRED DEVICE CONFIGURATION<br>FOR ACTIVE MONITORING                                                                          | WHEN MONITORED                                                                                                |
|-----------------|---------------------------------------------------------------------------------------------------------------------------------|---------------------------------------------------------------------------------------------------------------|
| Overvoltage     | <ul style="list-style-type: none"> <li>• Voltage monitoring enabled (SELECT[5:0] = 10h or 20h in MFR_CHANNEL_CONFIG)</li> </ul> | Continuous monitoring.                                                                                        |
| Undervoltage    | <ul style="list-style-type: none"> <li>• Voltage monitoring enabled (SELECT[5:0] = 10h or 20h in MFR_CHANNEL_CONFIG)</li> </ul> | Stop monitoring while the power supply is off; start monitoring when voltage exceeds the POWER_GOOD_ON level. |
| Overcurrent     | <ul style="list-style-type: none"> <li>• Current monitoring enabled (SELECT[5:0] = 22h in MFR_CHANNEL_CONFIG)</li> </ul>        | Continuous monitoring.                                                                                        |
| Power-Up Time   | <ul style="list-style-type: none"> <li>• Sequencing enabled (SELECT[5:0] = 10h in MFR_CHANNEL_CONFIG)</li> </ul>                | Monitored only during power-on sequence.                                                                      |
| Overtemperature | <ul style="list-style-type: none"> <li>• Temperature sensor enabled (ENABLE = 1 in MFR_TEMP_SENSOR_CONFIG)</li> </ul>           | Continuous monitoring.                                                                                        |

**Note:** Device response to faults is determined by the configuration of MFR\_FAULT\_RESPONSE.

## Password Protection

The device can be password protected by using the LOCK bit in the MFR\_MODE command. Once the device is locked, only certain PMBus commands can be accessed with the serial port. See [Table 3](#) for a complete list of PMBus commands. Commands that have password protection return all ones (FFh), with the proper number of data bytes, when read. When the device is locked, only the PAGE, OPERATION, CLEAR\_FAULTS, and MFR\_SERIAL commands can be written; all other written commands are ignored. When MFR\_SERIAL is written and the upper 4 bytes match the internally flash-stored value, the device unlocks and remains unlocked until the LOCK bit in MFR\_MODE is activated once again. The LOCK status bit in STATUS\_MFR\_SPECIFIC is always available to indicate whether the device is locked or unlocked.

## Power-Supply Sequencing

Sequencing control for each of the 12 power-supply channels on the device is configured using the MFR\_SEQ\_CONFIG and ON\_OFF\_CONFIG commands.

See the descriptions of these commands for details on the exact device configuration required. Power supplies can be powered up and down in any order (even across multiple devices). See the command descriptions and [Figure 2](#) for specifics on sequencing control.

## Dual-Loop Sequencing

The device contains two independent sequencing groups, SEQUENCE0 and SEQUENCE1. Both groups do not need to be used, but every channel is assigned to one of the two groups with the SEQ\_SELECT bit in the MFR\_SEQ\_CONFIG command. The two sequencing groups operate independently. SEQUENCE0 is always associated with CONTROL0 and SEQUENCE1 is always associated with CONTROL1. The two sequencing groups can also be independently controlled with the OPERATION command. With the ON\_OFF\_CONFIG command, the device is configured to respond to the CONTROLn pins or the OPERATION command (or both). When the OPERATION command is sent to the device (when the PAGE is set to 255), both sequence groups are controlled, as shown in [Table 8](#).

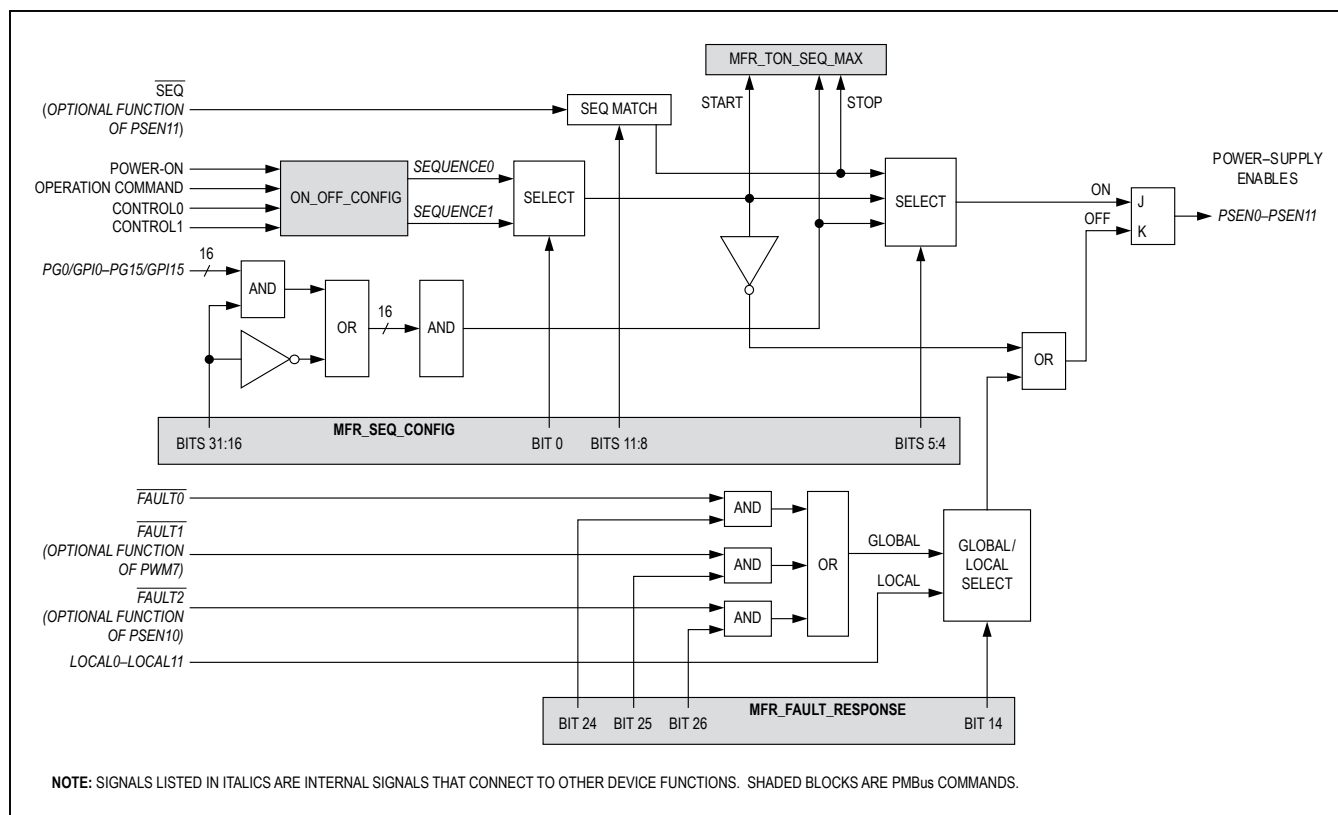


Figure 2. Sequence Control Logic



**Table 8. OPERATION Command Sequence Control Options**

| GROUP     | OPERATION COMMAND (PAGE = 255) |            |               |
|-----------|--------------------------------|------------|---------------|
|           | ON                             | SOFT-OFF   | IMMEDIATE OFF |
| SEQUENCE0 | 80h or 81h                     | 40h or 41h | 00h or 01h    |
| SEQUENCE1 | 80h or 82h                     | 40h or 42h | 00h or 02h    |

**Power-On Sequencing**

The activation of all power-supply channels (even across multiple devices) is initiated from a common START signal that can either be the CONTROL0 or CONTROL1 pin, or the OPERATION command. Each power-supply channel on the device can be sequenced on by one of the following methods:

- Power is applied to the device.
- The CONTROL0 pin goes active.
- The CONTROL1 pin goes active.
- The OPERATION command is received.
- The logic combination of power goods and GPI is valid.
- The  $\overline{\text{SEQ}}$  pin signal is matched.

Each enabled PSEN<sub>n</sub> output goes active (either active high or active low, as defined in MFR\_PSEN\_CONFIG) after the associated delay time programmed in TON\_DELAY. The power supplies can be sequenced on in any order. Each channel can be sequenced on with either time-based or event-based conditions. The output voltage of each power supply is monitored to ensure that the supply crosses the power-good-on level (as configured in the POWER\_GOOD\_ON command) within a programmable time limit, as configured in the TON\_MAX\_FAULT\_LIMIT command. This power-up time limit can be disabled by configuring TON\_MAX\_FAULT\_LIMIT to 0000h. For channels using event-based sequencing, the MFR\_TON\_SEQ\_MAX command determines the maximum time limit for the sequence-on event to occur. Like the TON\_MAX\_FAULT\_LIMIT, this limit can be disabled by configuring MFR\_TON\_SEQ\_MAX to 0000h. There is a one-to-one correspondence between the RS<sub>n</sub> inputs and the PSEN<sub>n</sub> outputs. For example, RS6 monitors the power supply controlled by PSEN6. All power-on sequencing is gated by detected faults. Before any power-supply channel is enabled (or the FAULT<sub>n</sub> output deasserted) the device checks for overvoltage, overcurrent, and temperature faults that are enabled (but not for undervoltage since the supply is off).

**Power-Off Sequencing**

The order in which the supplies are disabled is determined with the TOFF\_DELAY configuration. Alternatively,

all the power supplies can be switched off immediately, as configured in the ON\_OFF\_CONFIG command or with the OPERATION command.

As configured with the ON\_OFF\_CONFIG command, either the CONTROL0 or CONTROL1 pin or the OPERATION command is the master off switch. When either the CONTROL0 or CONTROL1 pin goes inactive, or the OPERATION off command is received (or one of the enabled FAULT<sub>n</sub> pins asserted), the power supplies are sequenced off. Neither the power-good (PG) or GPI logic combinations, nor the  $\overline{\text{SEQ}}$  pin, can be used to turn off the power supplies.

**Sequencing Example**

As an example, [Figure 3](#) details a simple sequencing scheme consisting of four power supplies using a mixture of time-based and event-based sequencing. Channels 0 and 2 use time-based sequencing and channels 1 and 5 use event-based sequencing. When either the CONTROL0 or CONTROL1 pin goes active, or the OPERATION command is received (as defined by the ON\_OFF\_CONFIG command), PSEN0 is asserted after the delay time configured in TON\_DELAY. RS0 is monitored to ensure that the PSEN0 supply crosses the power-good-on level (as configured in POWER\_GOOD\_ON) within a programmable time limit (as configured in TON\_MAX\_FAULT\_LIMIT). PSEN2 operates in a similar fashion as PSEN0, but with a different TON\_DELAY and a different TON\_MAX\_FAULT\_LIMIT. Since the power-up of channels 0 and 2 are based solely on their TON\_DELAY values, these channels are time-based.

When RS2 crosses its power-good-on level, PSEN5 is asserted after its configured TON\_DELAY and similarly, PSEN1 asserts when RS5 crosses its power-good-on level. Since the power-up of channels 5 and 1 are based on the power-good states of other channels, these channels are event-based. The MFR\_TON\_SEQ\_MAX command can be used to ensure that these events occur and the power-up sequence does not hang waiting for an event to transpire. When RS1 crosses its power-good-on level, it has been configured to generate a  $\overline{\text{SEQ}}$  pin signal to communicate to another device to turn on one or more of its power supplies.



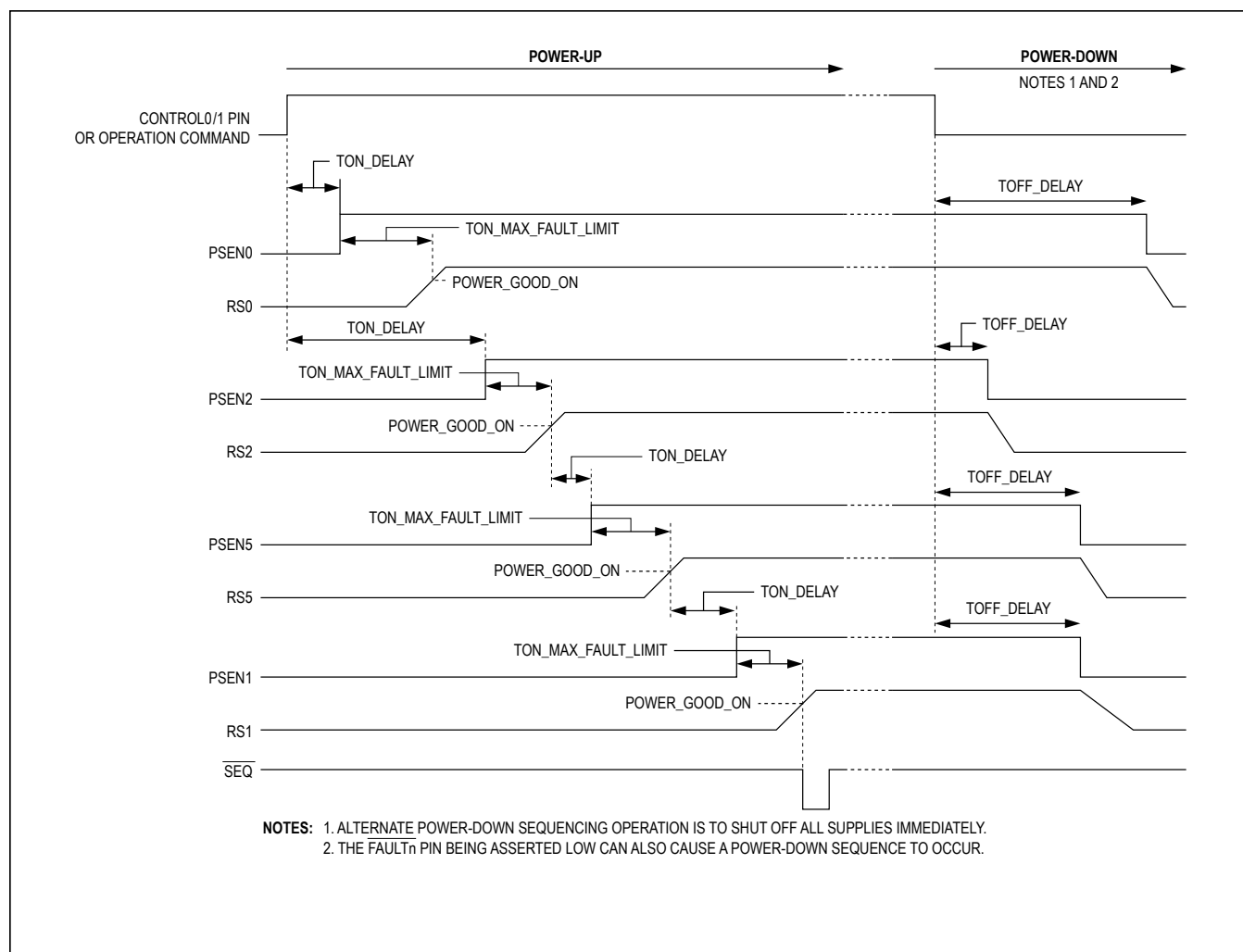


Figure 3. Sequencing Example

### Multiple Device Connections

Multiple MAX34451 devices can be connected together to increase the system channel count. [Figure 4](#) details the recommended connection scheme.

All the paralleled devices share the same CONTROL<sub>n</sub>, FAULT<sub>n</sub>, SEQ, and SMBus signals. The devices all use a common signal (either the CONTROL0 or CONTROL1 pin, or the OPERATION command) to enable/disable all the power supplies. Any of the monitored power supplies can be configured with the MFR\_FAULT\_RESPONSE command to activate one or more of the FAULT<sub>n</sub> signals and shut down all the other supplies enabled to respond

to one or more of the FAULT<sub>n</sub> signals. The FAULT<sub>0</sub> signal is always available, whereas FAULT<sub>1</sub> and FAULT<sub>2</sub> are optional signals. When they are enabled, the PWM7 and PSEN10 outputs (respectively) are disabled. The use of multiple fault signals allows more flexibility in controlling which power supplies need to shut down during a fault.

#### USER NOTE:

- All devices must be configured with the same ON\_OFF\_CONFIG configuration.
- All devices must be powered up and reset at the same time.

## SEQ Pin Operation

The  $\overline{\text{SEQ}}$  pin is another optional signal. When this function is enabled, it allows multiple devices to coordinate event-based sequencing. With the `MFR_CHANNEL_CONFIG` command, any channel can be configured to generate one of 15 signatures. When the channel crosses its power-good-on level, it generates the needed  $\overline{\text{SEQ}}$  signature if so enabled. With the `MFR_SEQ_CONFIG` command, any of the sequencing channels (PAGES 0–11) can be configured to wait for a match on the  $\overline{\text{SEQ}}$  pin before asserting the  $\text{PSEN}_n$  output. To ensure that a valid  $\overline{\text{SEQ}}$  signal is received when it should be, the maximum allowable time is configured into the `MFR_TON_SEQ_MAX` command.

### USER NOTE:

- Only one channel should be configured with any one particular  $\overline{\text{SEQ}}$  signature. If two channels have the same signature, they might reach their power-good-on levels at different times and corrupt the  $\overline{\text{SEQ}}$  signal.
- Allow more than 15ms between consecutive  $\overline{\text{SEQ}}$  signatures.

## System Watchdog Timer

The device uses an internal watchdog timer. This timer is internally reset every 5ms. In the event the device is locked up, and the watchdog reset does not occur after 210ms, the device is automatically reset. After the reset occurs, the device reloads all configuration values that were stored to flash and begins normal operation. After the reset, the device also does the following:

- 1) Sets the `MFR` bit in `STATUS_WORD`.
- 2) Sets the `WATCHDOG_INT` bit in `STATUS_MFR_SPECIFIC` (for PAGE 255).
- 3) Notifies the host through  $\overline{\text{ALERT}}$  assertion (if enabled in `MFR_MODE`).

## CRC Memory Check

Upon reset, the device runs an internal algorithm to check the integrity of the key internal nonvolatile memory. If the CRC check fails, the device does not power up and remains in a null state with all pins high impedance but asserts the  $\overline{\text{FAULT0}}$  output.

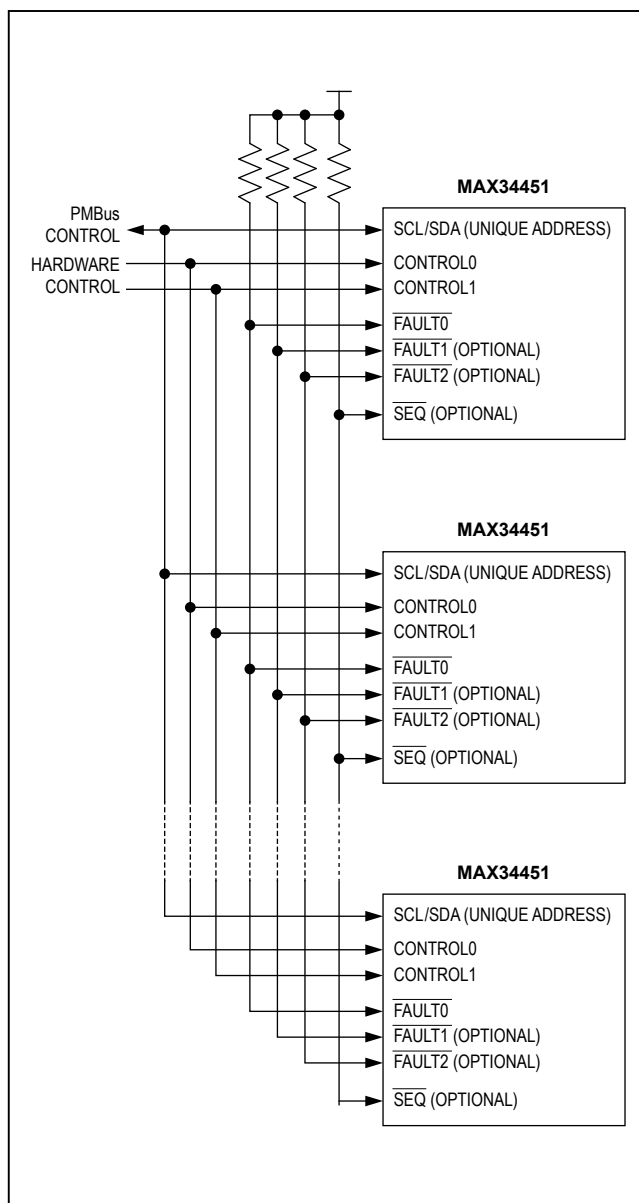


Figure 4. Multiple MAX34451 Hardware Connections

## PMBus Commands

A summary of the PMBus commands supported by the device are described in the following sections.

### PAGE (00h)

The device can monitor up to 16 voltages or currents, sequence up to 12 power supplies, and margin up to 12 power supplies. The device can monitor up to five temperature sensors, one internal local temperature sensor, plus four external remote temperature sensors (DS75LV). All the monitoring and control is accomplished using one PMBus (I<sup>2</sup>C) address. Send the

PAGE command with data 0–20 (decimal) to select which power supply or temperature sensor is affected by all the following PMBus commands. Not all commands are supported within each page. If an unsupported command is received, the CML status bit is set. Some commands are common, which means that any selected page has the same effect on and the same response from the device. See [Table 9](#) for PAGE commands.

Set the PAGE to 255 when the following PMBus commands should apply to all pages at the same time. There are only a few commands (OPERATION, CLEAR\_FAULTS) where this function has a real application.

**Table 9. PAGE (00h) Commands**

| PAGE*  | ASSOCIATED CONTROL                                                                                                                        |
|--------|-------------------------------------------------------------------------------------------------------------------------------------------|
| 0      | Power supply monitored by RS0, controlled by PSEN0, and margined with PWM0.                                                               |
| 1      | Power supply monitored by RS1, controlled by PSEN1, and margined with PWM1.                                                               |
| 2      | Power supply monitored by RS2, controlled by PSEN2, and margined with PWM2.                                                               |
| 3      | Power supply monitored by RS3, controlled by PSEN3, and margined with PWM3.                                                               |
| 4      | Power supply monitored by RS4, controlled by PSEN4, and margined with PWM4.                                                               |
| 5      | Power supply monitored by RS5, controlled by PSEN5, and margined with PWM5.                                                               |
| 6      | Power supply monitored by RS6, controlled by PSEN6, and margined with PWM6.                                                               |
| 7      | Power supply monitored by RS7, controlled by PSEN7, and margined with PWM7.                                                               |
| 8      | Power supply monitored by RS8, controlled by PSEN8, and optionally margined by OUT0 of external DS4424 at I <sup>2</sup> C address A0h.   |
| 9      | Power supply monitored by RS9, controlled by PSEN9, and optionally margined by OUT1 of external DS4424 at I <sup>2</sup> C address A0h.   |
| 10     | Power supply monitored by RS10, controlled by PSEN10, and optionally margined by OUT2 of external DS4424 at I <sup>2</sup> C address A0h. |
| 11     | Power supply monitored by RS11, controlled by PSEN11, and optionally margined by OUT3 of external DS4424 at I <sup>2</sup> C address A0h. |
| 12     | ADC channel 12 (monitors voltage or current) or GPI.                                                                                      |
| 13     | ADC channel 13 (monitors voltage or current) or GPI.                                                                                      |
| 14     | ADC channel 14 (monitors voltage or current) or GPI.                                                                                      |
| 15     | ADC channel 15 (monitors voltage or current) or GPI.                                                                                      |
| 16     | Internal temperature sensor.                                                                                                              |
| 17     | External DS75LV temperature sensor with I <sup>2</sup> C address 90h.                                                                     |
| 18     | External DS75LV temperature sensor with I <sup>2</sup> C address 92h.                                                                     |
| 19     | External DS75LV temperature sensor with I <sup>2</sup> C address 94h.                                                                     |
| 20     | External DS75LV temperature sensor with I <sup>2</sup> C address 96h.                                                                     |
| 21–254 | Reserved.                                                                                                                                 |
| 255    | Applies to all pages.                                                                                                                     |

\*PAGES 0–11 can also be used to configure GPI and GPO operation.

OPERATION (01h)

The OPERATION command is used to turn the power supply on and off in conjunction with the CONTROLn input pin. The OPERATION command is also used to cause the power supply to set the output voltage to the upper or lower margin voltages. The power supply stays in the commanded operating mode until a subsequent OPERATION command or a change in the state of the CONTROLn pin (if enabled) instructs the power supply to change to another state. The valid OPERATION command byte values are shown in [Table 10](#). The OPERATION command controls how the device responds when commanded to change the output. When the command byte is 00h, the device immediately turns the power supply off and ignores any programmed turn-off delay. When the command byte is set to 40h, 41h, or 42h the device powers down, according to the programmed turn-off delay. In [Table 10](#), [Table 11](#), and [Table 12](#), “act on any fault” means that if any warning or fault on the selected power supply is detected when the output is margined, the device treats this as a warning or fault and responds as programmed. “Ignore all faults” means that

all warnings and faults on the selected power supply are ignored. Any command value not shown in these tables is an invalid command. If the device receives a data byte that is not listed in these tables, then it treats this as invalid data, declares a data fault (sets CML bit and asserts ALERT), and responds as described in the *Fault Management and Reporting* section.

In most cases, for power-on and power-off control, the OPERATION command should be sent when the PAGE is set to 255. If the PAGE is set to 0–11, the OPERATION command is only applied to the power supply on that page and the power supply is turned on and off using the associated TON\_DELAY and TOFF\_DELAY settings without any regard to the other supplies.

For individual channel-margining control, the OPERATION command can be used with the PAGE set to 0–11. When the PAGE is set to 255, the OPERATION margining commands affect all channels.

The OPERATION command for the device contains a few special values that are not part of the PMBus standard to allow the device to offer independent control. See the shaded values in [Table 11](#).

Table 10. OPERATION (01h) Command Byte with PAGE = 0–11  
(When Bit 3 of ON\_OFF\_CONFIG = 1)

| COMMAND BYTE | POWER SUPPLY ON/OFF           | MARGIN STATE                    |
|--------------|-------------------------------|---------------------------------|
| 00h          | Immediate off (no sequencing) | —                               |
| 40h          | Soft-off (with sequencing)    | —                               |
| 80h          | On                            | Margin off                      |
| 94h          | On                            | Margin low (ignore all faults)  |
| 98h          | On                            | Margin low (act on any fault)   |
| A4h          | On                            | Margin high (ignore all faults) |
| A8h          | On                            | Margin high (act on any fault)  |

**Note:** All enabled channels must exceed POWER\_GOOD\_ON for margining to begin.

**Table 11. OPERATION (01h) Command Byte with PAGE = 255 (When Bit 3 of ON\_OFF\_CONFIG = 1)**

| COMMAND BYTE | POWER SUPPLY ON/OFF              | SEQUENCE AFFECTED          | MARGIN STATE                    |
|--------------|----------------------------------|----------------------------|---------------------------------|
| 00h          | Immediate off<br>(no sequencing) | SEQUENCE0 and<br>SEQUENCE1 | n/a                             |
| 01h          |                                  | SEQUENCE0 only             |                                 |
| 02h          |                                  | SEQUENCE1 only             |                                 |
| 40h          | Soft-off<br>(with sequencing)    | SEQUENCE0 and<br>SEQUENCE1 |                                 |
| 41h          |                                  | SEQUENCE0 only             |                                 |
| 42h          |                                  | SEQUENCE1 only             |                                 |
| 80h          | On                               | SEQUENCE0 and<br>SEQUENCE1 | Margin off                      |
| 81h          |                                  | SEQUENCE0 only             |                                 |
| 82h          |                                  | SEQUENCE1 only             |                                 |
| 94h          | On                               | SEQUENCE0 and<br>SEQUENCE1 | Margin low (ignore all faults)  |
| 98h          | On                               |                            | Margin low (act on any fault)   |
| A4h          | On                               |                            | Margin high (ignore all faults) |
| A8h          | On                               |                            | Margin high (act on any fault)  |

**Note:** Special device OPERATION commands are shaded; when the OPERATION command is read, the device always responds with the standard command; all enabled channels must exceed POWER\_GOOD\_ON for margining to begin.

**Table 12. OPERATION (01h) Command Byte (When Bit 3 of ON\_OFF\_CONFIG = 0)**

| COMMAND BYTE | POWER SUPPLY ON/OFF   | MARGIN STATE                    |
|--------------|-----------------------|---------------------------------|
| 00h          | Command has no effect | n/a                             |
| 40h          |                       |                                 |
| 80h          |                       | Margin off                      |
| 94h          |                       | Margin low (ignore all faults)  |
| 98h          |                       | Margin low (act on any fault)   |
| A4h          |                       | Margin high (ignore all faults) |
| A8h          |                       | Margin high (act on any fault)  |

**Note:** The device only takes action if the supply is enabled; all enabled channels must exceed POWER\_GOOD\_ON for margining to begin; if PAGE is set to 255, both SEQUENCE0 and SEQUENCE1 are affected.

**ON\_OFF\_CONFIG (02h)**

The ON\_OFF\_CONFIG command configures the combination of the CONTROLn input and PMBus OPERATION commands needed to turn the power supply on and off. This indicates how the power supply is command-

ed when power is applied. The ON\_OFF\_CONFIG message content is described in [Table 13](#). The host should not modify ON\_OFF\_CONFIG while the power supplies are active. The configuration of the ON\_OFF\_CONFIG command applies to both CONTROL0 and CONTROL1. See [Figure 5](#).

**Table 13. ON\_OFF\_CONFIG (02h) Command Byte**

| BIT | PURPOSE                                                                          | VALUE | MEANING                                                                                                                             |
|-----|----------------------------------------------------------------------------------|-------|-------------------------------------------------------------------------------------------------------------------------------------|
| 7:6 | Reserved.                                                                        | n/a   | Always returns 000.                                                                                                                 |
| 5   | OPERATION command and CONTROLn pin and/or select.                                | 0     | OPERATION command is ANDed with CONTROLn pin if both are enabled.                                                                   |
|     |                                                                                  | 1     | OPERATION command is ORed with CONTROLn pin if both are enabled.                                                                    |
| 4   | Turn on supplies when bias is present or use the CONTROLn pin/OPERATION command. | 0     | Turns on the supplies (with sequencing if so configured) as soon as bias is supplied to the device, regardless of the CONTROLn pin. |
|     |                                                                                  | 1     | Uses CONTROLn pins (if enabled) and/or OPERATION command (if enabled).*                                                             |
| 3   | OPERATION command enable.                                                        | 0     | On/off portion of the OPERATION command disabled.                                                                                   |
|     |                                                                                  | 1     | OPERATION command enabled.                                                                                                          |
| 2   | CONTROLn pin enable.                                                             | 0     | CONTROLn pin disabled.                                                                                                              |
|     |                                                                                  | 1     | CONTROLn pin enabled.                                                                                                               |
| 1   | CONTROLn pin polarity.                                                           | 0     | Active low (drive low to turn on the power supplies).                                                                               |
|     |                                                                                  | 1     | Active high (drive high to turn on the power supplies).                                                                             |
| 0   | CONTROLn pin turn-off action.                                                    | 0     | Uses the programmed turn-off delay (soft-off).                                                                                      |
|     |                                                                                  | 1     | Turns off the power supplies immediately.                                                                                           |

\*Unless bit 5 is set (if both bits 3:2 are set), both the CONTROL0 or CONTROL1 pin and the OPERATION command are required to turn the supplies on, and either can turn the supplies off.

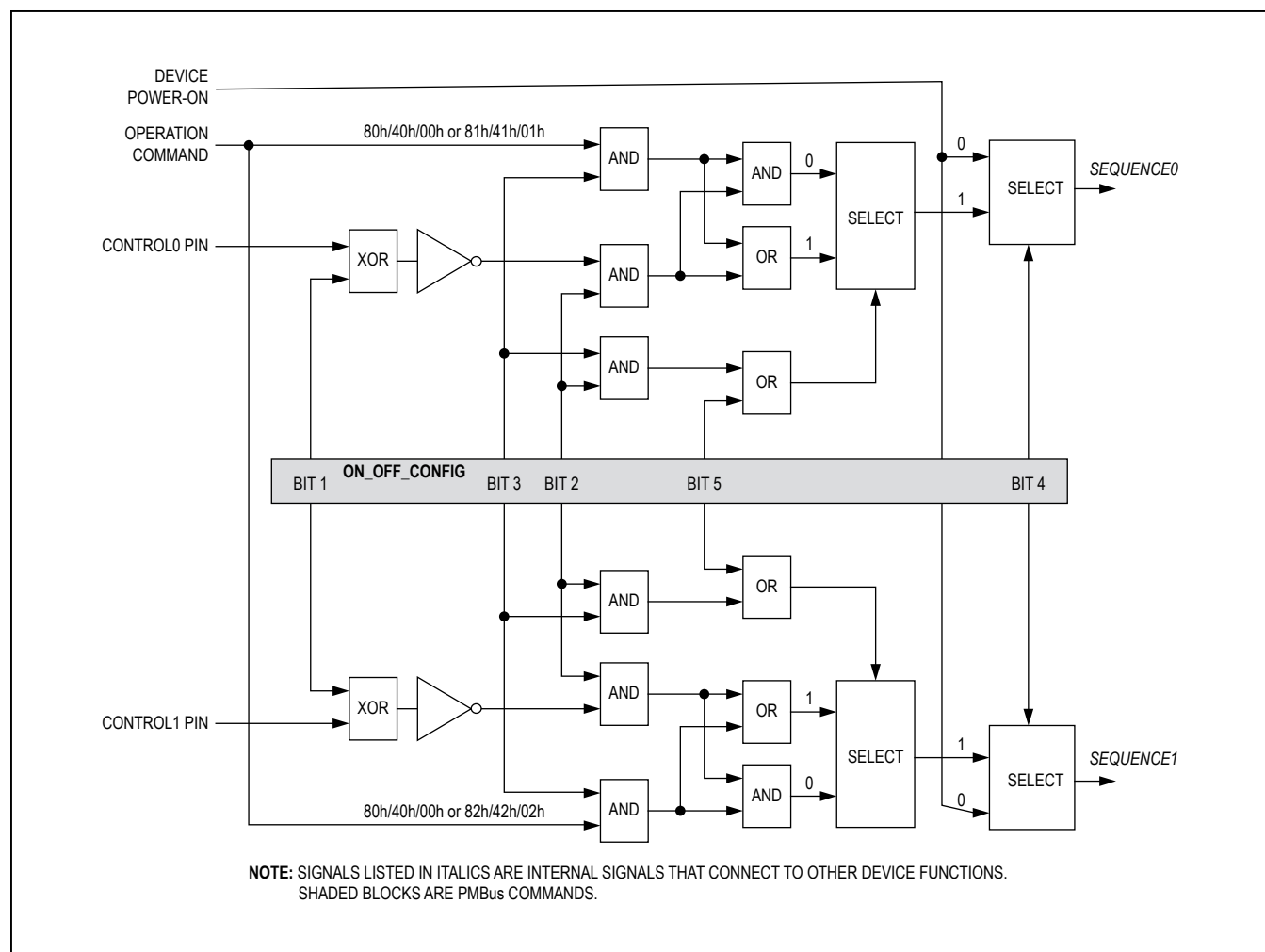


Figure 5. ON\_OFF\_CONFIG Logical Control

CLEAR\_FAULTS (03h)

The CLEAR\_FAULTS command is used to clear any latched fault or warning bits in the status registers that have been set and also unconditionally deasserts the ALERT output. This command clears all bits simultaneously. The CLEAR\_FAULTS command does not cause a power supply that has latched off for a fault condition to restart. The state of the PSENN outputs under fault conditions are not affected by this command and changes only if commanded through the OPERATION command or the CONTROLn pins. If a fault is still present after the CLEAR\_FAULTS command is executed, the fault status bit is immediately set again, but ALERT is not reasserted. ALERT is only asserted again when a new fault or warning is detected that occurs after the CLEAR\_FAULTS command is executed. This command is write-only. There is no data byte for this command.

WRITE\_PROTECT (10h)

The WRITE\_PROTECT command is used to provide protection against accidental changes to the device's operating memory. All supported commands can have their parameters read, regardless of the WRITE\_PROTECT settings. The WRITE\_PROTECT message content is described in [Table 14](#).

Device Configuration Data Management

The device stores configuration data in both nonvolatile flash memory and volatile RAM. The PMBus engine manages the device configuration data. See [Figure 6](#).

The flash memory has three separate arrays for configuration parameters, whereas the RAM only has a single array. When a PMBus command is written to the device, it is always written to the RAM. When the device is shipped from the factory, the MAIN and BACKUP flash memory arrays are identical and are configured as shown in [Table 3](#). The SINGLE array is empty.

There is a set of five PMBus commands that can be used to transfer data between the flash and RAM arrays. These commands are described in [Table 15](#).

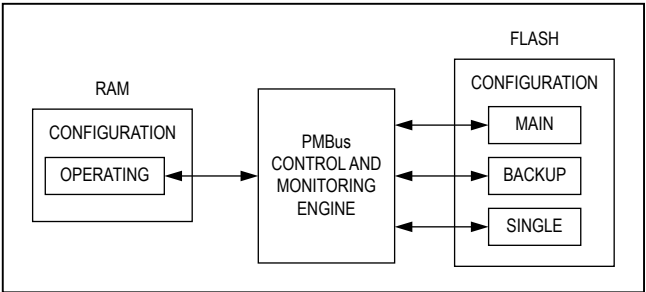


Figure 6. Device Configuration Data Management

Table 14. WRITE\_PROTECT (10h) Command Byte

| COMMAND BYTE | MEANING                                                                                    |
|--------------|--------------------------------------------------------------------------------------------|
| 80h          | Disables all writes except the WRITE_PROTECT command.                                      |
| 40h          | Disables all writes except the WRITE_PROTECT, OPERATION, and PAGE commands.                |
| 20h          | Disables all writes except the WRITE_PROTECT, OPERATION, PAGE, and ON_OFF_CONFIG commands. |
| 00h          | Enables writes for all commands (default).                                                 |

**Note:** No fault or error is generated if the host attempts to write to a protected area.

Table 15. Memory Transfer PMBus Commands

| PMBus COMMAND       |            | RESULTING MEMORY TRANSFER                                    |
|---------------------|------------|--------------------------------------------------------------|
| STORE_DEFAULT_ALL   |            | Copies RAM OPERATING to the flash MAIN.                      |
| RESTORE_DEFAULT_ALL |            | Copies the flash MAIN to RAM OPERATING.                      |
| MFR_STORE_ALL       | CODE = 00h | Copies RAM OPERATING to the flash MAIN.                      |
|                     | CODE = 01h | Copies RAM OPERATING to the flash BACKUP.                    |
| MFR_RESTORE_ALL     | CODE = 00h | Copies the flash MAIN array to RAM OPERATING.                |
|                     | CODE = 01h | Copies the flash BACKUP to RAM OPERATING.                    |
| MFR_STORE_SINGLE    |            | Copies RAM OPERATING (single parameter) to the flash SINGLE. |



**STORE\_DEFAULT\_ALL (11h)**

The STORE\_DEFAULT\_ALL command instructs the device to copy RAM OPERATING to the flash MAIN memory array. Not all information is stored. Only configuration data is stored, not any status or operational data. If an error occurs during the transfer, ALERT asserts if enabled and the CML bit in STATUS\_WORD is set to 1. No bits are set in STATUS\_CML. This command is write-only. There is no data byte for this command.

When the STORE\_DEFAULT\_ALL command is invoked, the device is unresponsive to PMBus commands and does not monitor power supplies while transferring the configuration. The time required to complete this task is listed in the *Electrical Characteristics* section. The MFR\_STORE\_SINGLE command allows a single command to be stored in much less time.

**USER NOTE:** V<sub>DD</sub> must be above 2.9V for the device to perform the STORE\_DEFAULT\_ALL command.

**RESTORE\_DEFAULT\_ALL (12h)**

The RESTORE\_DEFAULT\_ALL command instructs the device to copy the flash MAIN memory array to RAM OPERATING. The RESTORE\_DEFAULT\_ALL command should only be executed when the device is not operating the power supplies. This command is write-only. There is no data byte for this command. When RESTORE\_DEFAULT\_ALL is issued, the data is checked for validity before being transferred. If the MAIN array is corrupt, the device sets bit 1 of STATUS\_CML and loads the BACKUP copy. If the BACKUP copy is corrupt, then the device sets bit 2 of STATUS\_CML and remains in a null state with all pins (except SCL and SDA) in high impedance. The FAULT<sub>n</sub> pin(s) are also asserted. To resolve the data corruption, the configuration data must be written to RAM OPERATING and STORE\_DEFAULT\_ALL must be issued, followed by a device reset.

Upon a device power-on reset, or any device reset, this command is automatically executed by the device without PMBus action required.

**MFR\_STORE\_ALL (EEh)**

The MFR\_STORE\_ALL command instructs the device to copy RAM OPERATING to either the flash MAIN memory array (CODE = 00h) or the flash BACKUP memory array (CODE = 01h). This command is write-only. There is 1 data byte for this command, which is the CODE. The CODE is either 00h to instruct the device to copy into the MAIN array, or 01h to copy into the BACKUP array.

All other CODE values are ignored. Not all information is stored. Only configuration data is stored, not any status or operational data. If an error occurs during the transfer, ALERT asserts if enabled and the CML bit in STATUS\_WORD is set to 1. No bits are set in STATUS\_CML. Note that if the CODE is 00h, then this command operates the same as STORE\_DEFAULT\_ALL.

|            |                                    |
|------------|------------------------------------|
| CODE = 00h | Copy RAM OPERATING to flash MAIN   |
| CODE = 01h | Copy RAM OPERATING to flash BACKUP |

When the MFR\_STORE\_ALL command is invoked, the device is unresponsive to PMBus commands and does not monitor power supplies while transferring the configuration. The time required to complete this task is listed in the *Electrical Characteristics* section. The MFR\_STORE\_SINGLE command allows a single command to be stored in much less time.

**USER NOTE:** V<sub>DD</sub> must be above 2.9V for the device to perform the MFR\_STORE\_ALL command.

**MFR\_RESTORE\_ALL (EFh)**

The MFR\_RESTORE\_ALL command instructs the device to copy either the flash MAIN memory array (CODE = 00h) or the flash BACKUP memory array (CODE = 01h) to RAM OPERATING. This command is write-only. There is 1 data byte for this command, which is the CODE. The CODE is either 00h to instruct the device to copy from the MAIN array or 01h to copy from the BACKUP array. All other CODE values are ignored. Note that if the CODE is 00h, then this command operates the same as RESTORE\_DEFAULT\_ALL.

|            |                                    |
|------------|------------------------------------|
| CODE = 00h | Copy flash MAIN to RAM OPERATING   |
| CODE = 01h | Copy flash BACKUP to RAM OPERATING |

The MFR\_RESTORE\_ALL command should only be executed when the device is not operating the power supplies.

When MFR\_RESTORE\_ALL is issued, the data is checked for validity before being transferred. If the MAIN array is corrupt, the device sets bit 1 of STATUS\_CML. If the BACKUP array is corrupt, then the device sets bit 2 of STATUS\_CML. No other action is taken by the device. To resolve the data corruption, the configuration data must be written to RAM OPERATING and STORE\_DEFAULT\_ALL or MFR\_STORE\_ALL must be issued.

MFR\_STORE\_SINGLE (FCh)

MFR\_STORE\_SINGLE is a read/write word command that instructs the device to transfer a single configuration parameter from RAM OPERATING to the flash SINGLE memory array. The upper byte contains the PAGE and the lower byte contains the PMBus command that should be stored. For example, if the TON\_DELAY parameter for the power supply controlled by PAGE 4 needs to be stored to flash, 0460h would be written with this command. When read, this command reports the last single PAGE/command written to flash. This command can be used while the device is operating the power supplies. If an error occurs during the transfer, ALERT asserts if enabled and the CML bit in STATUS\_WORD is set to 1. No bits are set in STATUS\_CML. The MFR\_STORE\_SINGLE command should only be invoked a maximum of 85 times before either a device reset is issued or a device power cycle occurs, or the RESTORE\_DEFAULT\_ALL

command is invoked. Once the MFR\_STORE\_SINGLE command is invoked, the STORE\_DEFAULT\_ALL and MFR\_STORE\_ALL commands should not be used until either a device reset is issued or a device power cycle occurs, or the RESTORE\_DEFAULT\_ALL command is invoked. Also, MFR\_STORE\_SINGLE should not be used for commands that are not stored in flash. See Table 3 for a list of commands that are stored in flash.

**USER NOTE:** V<sub>DD</sub> must be above 2.9V for the device to perform the MFR\_STORE\_SINGLE command.

MFR\_CRC (FEh)

MFR\_CRC is a read/write word command that instructs the device to report the calculated 16-bit CRC value of either the RAM OPERATING or the flash MAIN or BACKUP memory arrays. A CRC value for the flash SINGLE array is not available. Only one 16-bit CRC is reported with each read of MFR\_CRC. The CRC value to be reported is determined by the most previous written CODE value, as shown in Table 16. For example, if MFR\_CRC is first written with a CODE of 0001h, then the next read of MFR\_CRC reports the CRC for the flash BACKUP array. If no CODE value is written, than MFR\_CRC returns FFFFh when read. See Table 16.

CAPABILITY (19h)

The CAPABILITY command is used to determine some key capabilities of the device. The CAPABILITY command is read-only. The message content is described in Table 17.

Table 16. MFR\_CRC (FEh) Command Byte

| MFR_CRC CODE VALUE | MEMORY ARRAY CRC VALUE TO BE REPORTED ON NEXT READ OF MFR_CRC |
|--------------------|---------------------------------------------------------------|
| 0000h              | Flash MAIN                                                    |
| 0001h              | Flash BACKUP                                                  |
| 0002h              | RAM OPERATING                                                 |

Table 17. CAPABILITY (19h) Command Byte

| BIT | NAME                  | MEANING                                                                                                                                                                                                       |
|-----|-----------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7   | Packet-error checking | 0 = PEC not supported.                                                                                                                                                                                        |
| 6:5 | PMBus speed           | 01 = Maximum supported bus speed is 400kHz.                                                                                                                                                                   |
| 4   | ALERT                 | 1 = Device supports an $\overline{\text{ALERT}}$ output ( $\overline{\text{ALERT}}$ is enabled in MFR_MODE).<br>0 = Device does not support $\overline{\text{ALERT}}$ output (ALERT is disabled in MFR_MODE). |
| 3:0 | Reserved              | Always returns 0000.                                                                                                                                                                                          |

**VOUT\_MODE (20h)**

The VOUT\_MODE command is used to report the data format of the device. The device uses the DIRECT format for all the voltage-related commands. The value returned is 40h, indicating DIRECT data format. This command is read-only. If a host attempts to write this command, the CML status bit is asserted. See [Table 5](#) for the m, b, and R values for the various commands.

**VOUT\_MARGIN\_HIGH (25h)**

The VOUT\_MARGIN\_HIGH command loads the device with the voltage to which the power-supply output is to be changed when the OPERATION command is set to margin high. If the power supply is already operating at margin high, changing VOUT\_MARGIN\_HIGH has no effect on the output voltage. The device only adjusts the power supply to the new VOUT\_MARGIN\_HIGH voltage after receiving a new margin-high OPERATION command. The 2 data bytes are in DIRECT format. If the device cannot successfully close-loop margin the power supply, the device keeps attempting to margin the supply and does the following:

- 1) Sets the MARGIN bit in STATUS\_WORD.
- 2) Sets the MARGIN\_FAULT bit in STATUS\_MFR\_SPECIFIC (PAGES 0–11).
- 3) Notifies the host through  $\overline{\text{ALERT}}$  assertion (if enabled in MFR\_MODE).

**VOUT\_MARGIN\_LOW (26h)**

The VOUT\_MARGIN\_LOW command loads the device with the voltage to which the power-supply output changes to when the OPERATION command is set to margin low. If the power supply is already operating at

margin low, changing VOUT\_MARGIN\_LOW has no effect on the output voltage. The device only adjusts the power supply to the new VOUT\_MARGIN\_LOW voltage after receiving a new margin-low OPERATION command. The 2 data bytes are in DIRECT format. If the device cannot successfully close-loop margin the power supply, the device keeps attempting to margin the supply and does the following:

- 1) Sets the MARGIN bit in STATUS\_WORD
- 2) Sets the MARGIN\_FAULT bit in STATUS\_MFR\_SPECIFIC (PAGES 0–11)
- 3) Notifies the host through  $\overline{\text{ALERT}}$  assertion (if enabled in MFR\_MODE).

**VOUT\_SCALE\_MONITOR (2Ah)**

In applications where the measured power-supply voltage is not equal to the voltage at the ADC input, VOUT\_SCALE\_MONITOR is used. For example, if the ADC input expects a 1.8V input for a 12V output, VOUT\_SCALE\_MONITOR =  $1.8\text{V}/12\text{V} = 0.15$ . In applications where the power-supply output voltage is greater than the device input range of 2.048V, the output voltage of the power supply is sensed through a resistive voltage-divider. The resistive voltage-divider reduces or scales the output voltage. The PMBus commands specify the actual power-supply output voltages and not the input voltage to the ADC. To allow the device to map between the high power-supply voltages (such as 12V) and the voltage at the ADC input, the VOUT\_SCALE\_MONITOR command is used. The 2 data bytes are in DIRECT format. This value is dimensionless. As an example, if the required scaling factor is 0.15, then VOUT\_SCALE\_MONITOR should be set to 1333h ( $4915/32,767 = 0.15$ ). See [Table 18](#).

**Table 18. VOUT\_SCALE\_MONITOR (2Ah) Examples**

| NOMINAL VOLTAGE LEVEL MONITORED | NOMINAL ADC INPUT VOLTAGE LEVEL* | RESISTIVE DIVIDER RATIO | VOUT_SCALE_MONITOR VALUE |
|---------------------------------|----------------------------------|-------------------------|--------------------------|
| 1.8V or less                    | 1.8V                             | 1.0                     | 7FFFh                    |
| 2.5V                            | 1.8V                             | 0.72                    | 5C28h                    |
| 3.3V                            | 1.8V                             | 0.545454                | 45D1h                    |
| 5V                              | 1.8V                             | 0.36                    | 2E14h                    |
| 12V                             | 1.8V                             | 0.15                    | 1333h                    |

\*The full-scale ADC voltage on the device is 2.048V. A scaling factor where a 1.8V ADC input represents a nominal 100% voltage level is recommended to allow headroom for margining. Resistor-dividers must be used to measure voltage greater than 1.8V. The maximum source impedance of the resistor-divider is limited by the setting of the ADC\_TIME bits in MFR\_MODE. See the Recommended Operating Conditions section for details.

**IOUT\_CAL\_GAIN (38h)**

The IOUT\_CAL\_GAIN command is used to set the ratio of the voltage at the ADC input to the sensed current. The units of the IOUT\_CAL\_GAIN factor are 0.1mΩ. The 2 data bytes are in DIRECT format. As an example, if a 10mΩ sense resistor is used in conjunction with a 50V/V current-sense amplifier, the IOUT\_CAL\_GAIN should be set to 500mΩ or 1388h.

**USER NOTE:** The full-scale ADC voltage on the device is 2.048V. The value of the sense resistor and current-sense amplifier gain must be scaled appropriately. Also, the maximum voltage at the RSn inputs must be less than 4V. The maximum output impedance of the current-sense amplifier is limited by the setting of the ADC\_TIME bits in MFR\_MODE. See the *Recommended Operating Conditions* section for details.

**VOUT\_OV\_FAULT\_LIMIT (40h)**

The VOUT\_OV\_FAULT\_LIMIT command sets the value of the output voltage that causes an output overvoltage fault. The monitored voltage must drop by at least 2% below the limit before the fault is allowed to clear. The 2 data bytes are in DIRECT format. In response to the VOUT\_OV\_FAULT\_LIMIT being exceeded, the device does the following:

- 1) Sets the VOUT\_OV bit and the VOUT bit in STATUS\_WORD.
- 2) Sets the VOUT\_OV\_FAULT bit in STATUS\_VOUT.
- 3) Responds as specified in the MFR\_FAULT\_RESPONSE.
- 4) Notifies the host through  $\overline{\text{ALERT}}$  assertion (if enabled in MFR\_MODE).

**VOUT\_OV\_WARN\_LIMIT (42h)**

The VOUT\_OV\_WARN\_LIMIT command sets the value of the output voltage that causes an output-voltage high warning. The monitored voltage must drop by at least 2% below the limit before the warning is allowed to clear. This value is typically less than the output overvoltage threshold in VOUT\_OV\_FAULT\_LIMIT. The 2 data bytes are in DIRECT format. In response to the VOUT\_OV\_WARN\_LIMIT being exceeded, the device does the following:

- 1) Sets the VOUT bit in STATUS\_WORD.
- 2) Sets the VOUT\_OV\_WARN bit in STATUS\_VOUT.
- 3) Notifies the host using  $\overline{\text{ALERT}}$  assertion (if enabled in MFR\_MODE).

**VOUT\_UV\_WARN\_LIMIT (43h)**

The VOUT\_UV\_WARN\_LIMIT command sets the value of the output voltage that causes an output-voltage low warning. The monitored voltage must increase by at least 2% above the limit before the warning is allowed to clear. This value is typically greater than the output undervoltage-fault threshold in VOUT\_UV\_FAULT\_LIMIT. This warning is masked until the output voltage reaches the programmed POWER\_GOOD\_ON for the first time and also during turn-off when the power supply is disabled. If voltage is being monitored, this should be set to a value greater than 100mV. The 2 data bytes are in DIRECT format. In response to violation of the VOUT\_UV\_WARN\_LIMIT, the device does the following:

- 1) Sets the VOUT bit in STATUS\_WORD.
- 2) Sets the VOUT\_UV\_WARN bit in STATUS\_VOUT.
- 3) Notifies the host using  $\overline{\text{ALERT}}$  assertion (if enabled in MFR\_MODE).

**VOUT\_UV\_FAULT\_LIMIT (44h)**

The VOUT\_UV\_FAULT\_LIMIT command sets the value of the output voltage that causes an output undervoltage fault. The monitored voltage must increase by at least 2% above the limit before the fault is allowed to clear. This fault is masked until the output voltage reaches the programmed POWER\_GOOD\_ON for the first time and also during turn-off when the power supply is disabled. If voltage is being monitored, this should be set to a value greater than 100mV. The 2 data bytes are in DIRECT format. In response to violation of the VOUT\_UV\_FAULT\_LIMIT, the device does the following:

- 1) Sets the VOUT bit in STATUS\_WORD.
- 2) Sets the VOUT\_UV\_FAULT bit in STATUS\_VOUT.
- 3) Responds as specified in MFR\_FAULT\_RESPONSE.
- 4) Notifies the host using  $\overline{\text{ALERT}}$  assertion (if enabled in MFR\_MODE).

**IOUT\_OC\_WARN\_LIMIT (46h)**

The IOUT\_OC\_WARN\_LIMIT command sets the value of the current that causes an overcurrent warning. The monitored current must decrease by at least 5% below the limit before the warning is allowed to clear. This value is typically less than the overcurrent-fault threshold in IOUT\_OC\_FAULT\_LIMIT. The 2 data bytes are in DIRECT format. In response to violation of the IOUT\_OC\_WARN\_LIMIT, the device does the following:

- 1) Sets the IOUT bit in STATUS\_WORD.
- 2) Sets the IOUT\_OC\_WARN bit in STATUS\_IOUT.
- 3) Notifies the host using  $\overline{\text{ALERT}}$  assertion (if enabled in MFR\_MODE).

**IOUT\_OC\_FAULT\_LIMIT (4Ah)**

The IOUT\_OC\_FAULT\_LIMIT command sets the value of the current that causes an overcurrent fault. The monitored current must decrease by at least 5% below the limit before the fault is allowed to clear. This fault is masked until the current is below this limit for the first time. The 2 data bytes are in DIRECT format. In response to violation of the IOUT\_OC\_FAULT\_LIMIT, the device does the following:

- 1) Sets the IOUT bit in STATUS\_WORD.
- 2) Sets the IOUT\_OC\_FAULT bit in STATUS\_IOUT.
- 3) Responds as specified in the MFR\_FAULT\_RESPONSE.
- 4) Notifies the host using  $\overline{\text{ALERT}}$  assertion (if enabled in MFR\_MODE).

**OT\_FAULT\_LIMIT (4Fh)**

The OT\_FAULT\_LIMIT command sets the temperature, in degrees Celsius, of the selected temperature sensor at which an overtemperature fault is detected. The monitored temperature must drop by at least 4°C below the limit before the fault is allowed to clear. The 2 data bytes are in DIRECT format. In response to the OT\_FAULT\_LIMIT being exceeded, the device does the following:

- 1) Sets the TEMPERATURE bit in STATUS\_WORD.
- 2) Sets the OT\_FAULT bit in STATUS\_TEMPERATURE register.
- 3) Responds as specified in the MFR\_FAULT\_RESPONSE.
- 4) Notifies the host using  $\overline{\text{ALERT}}$  assertion (if enabled in MFR\_MODE).

**OT\_WARN\_LIMIT (51h)**

The OT\_WARN\_LIMIT command sets the temperature, in degrees Celsius, of the selected temperature sensor at which an overtemperature warning is detected. The monitored temperature must drop by at least 4°C below the limit before the warning is allowed to clear. The 2 data bytes are in DIRECT format. In response to the OT\_WARN\_LIMIT being exceeded, the device does the following:

- 1) Sets the TEMPERATURE bit in STATUS\_WORD.
- 2) Sets the OT\_WARN bit in STATUS\_TEMPERATURE register.
- 3) Notifies the host through  $\overline{\text{ALERT}}$  assertion (if enabled in MFR\_MODE).

**POWER\_GOOD\_ON (5Eh)**

The POWER\_GOOD\_ON command sets the value of the output voltage that the channel must exceed for a power-good state to be declared on this channel. All power supplies must also be above POWER\_GOOD\_ON for power-supply margining to begin. The POWER\_GOOD\_ON threshold is also used to determine if TON\_MAX\_FAULT\_LIMIT is exceeded. The POWER\_GOOD\_ON level is normally set higher than the POWER\_GOOD\_OFF level. The 2 data bytes are in DIRECT format.

**POWER\_GOOD\_OFF (5Fh)**

The POWER\_GOOD\_OFF command sets the value of the output voltage that causes the power-good state on this channel to deassert after it has been asserted. The POWER\_GOOD\_OFF level is normally set lower than the POWER\_GOOD\_ON level. The 2 data bytes are in DIRECT format.

When the VOUT level of a power supply falls from greater than POWER\_GOOD\_ON to less than POWER\_GOOD\_OFF, the device does the following:

- 1) Sets the POWER\_GOOD# bit in STATUS\_WORD.
- 2) Sets the POWER\_GOOD# bit in STATUS\_MFR\_SPECIFIC register (PAGES 0–11).

**TON\_DELAY (60h)**

In the PMBus sequencing configuration, TON\_DELAY sets the time, in milliseconds, from when a START condition is received until the PSENn output is asserted. If the PSENn/GPOn output has been configured (with the MFR\_PSEN\_CONFIG command) as a PG/GPI or alarm, then this command can be used to delay the assertion of the output. The 2 data bytes are in DIRECT format.

**TOFF\_DELAY (64h)**

TOFF\_DELAY sets the time, in milliseconds, from when a STOP condition is received (a soft-off OPERATION command, or through the CONTROLn pins when enabled) until the PSENn output is deasserted. When commanded to turn off immediately (either through the OPERATION command or the CONTROLn pins), the TOFF\_DELAY value is ignored. If the PSENn/GPOn output has been configured (with the MFR\_PSEN\_CONFIG command) as a PG/GPI or alarm, then this command can be used to delay the deassertion of the output. The 2 data bytes are in DIRECT format.

TON\_MAX\_FAULT\_LIMIT sets an upper time limit, in milliseconds, from when the PSENn output is asserted until the output voltage crosses the POWER\_GOOD\_ON threshold. The 2 data bytes are in DIRECT format. If the value is zero, then the limit is disabled. In response to the TON\_MAX\_FAULT\_LIMIT being exceeded, the device does the following:

- 1) Sets the VOUT bit in STATUS\_WORD.
- 2) Sets the TON\_MAX\_FAULT bit in STATUS\_VOUT.
- 3) Responds as specified in the MFR\_FAULT\_RESPONSE.
- 4) Notifies the host using  $\overline{\text{ALERT}}$  assertion (if enabled in MFR\_MODE).



**STATUS\_WORD (79h)**

The STATUS\_WORD command returns 2 bytes of information with a summary of the reason for a fault. The STATUS\_WORD message content is described in [Table 19](#).

**STATUS\_VOUT (7Ah)**

The STATUS\_VOUT command returns 1 byte of information with contents, as described in [Table 20](#). All the bits in STATUS\_VOUT are latched. When cleared, the bits are set again if the condition persists, or in the case of TON\_MAX\_FAULT, when the event occurs again.

**Table 19. STATUS\_WORD (79h)**

| BIT | NAME        | MEANING                                                                                                                                             |
|-----|-------------|-----------------------------------------------------------------------------------------------------------------------------------------------------|
| 15  | VOUT        | An output voltage fault or warning, or TON_MAX_FAULT_LIMIT or MFR_TON_SEQ_MAX has occurred.                                                         |
| 14  | IOUT        | An overcurrent fault or warning has occurred.                                                                                                       |
| 13  | 0           | This bit always returns a 0.                                                                                                                        |
| 12  | MFR         | A bit in STATUS_MFR_SPECIFIC (PAGE = 255) has been set.                                                                                             |
| 11  | POWER_GOOD# | Any power-supply voltage has fallen from POWER_GOOD_ON to less than POWER_GOOD_OFF (logical OR of all the POWER_GOOD# bits in STATUS_MFR_SPECIFIC). |
| 10  | 0           | This bit always returns a 0.                                                                                                                        |
| 9   | 0           | This bit always returns a 0.                                                                                                                        |
| 8   | MARGIN      | A margining fault has occurred.                                                                                                                     |
| 7   | 0           | This bit always returns a 0.                                                                                                                        |
| 6   | SYS_OFF     | Set when any of the power supplies are sequenced off (logical OR of all the OFF bits in STATUS_MFR_SPECIFIC).                                       |
| 5   | VOUT_OV     | An overvoltage fault has occurred.                                                                                                                  |
| 4   | IOUT_OC     | An overcurrent fault has occurred.                                                                                                                  |
| 3   | 0           | This bit always returns a 0.                                                                                                                        |
| 2   | TEMPERATURE | A temperature fault or warning has occurred.                                                                                                        |
| 1   | CML         | A communication, memory, or logic fault has occurred.                                                                                               |
| 0   | 0           | This bit always returns a 0.                                                                                                                        |

**Note:** The setting of the SYS\_OFF and POWER\_GOOD# bits do not assert the ALERT signal.

**Table 20. STATUS\_VOUT (7Ah)**

| BIT | NAME          | MEANING                                       | LATCHED |
|-----|---------------|-----------------------------------------------|---------|
| 7   | VOUT_OV_FAULT | VOUT overvoltage fault.                       | Yes     |
| 6   | VOUT_OV_WARN  | VOUT overvoltage warning.                     | Yes     |
| 5   | VOUT_UV_WARN  | VOUT undervoltage warning.                    | Yes     |
| 4   | VOUT_UV_FAULT | VOUT undervoltage fault.                      | Yes     |
| 3   | 0             | This bit always returns a 0.                  | —       |
| 2   | TON_MAX_FAULT | TON_MAX_FAULT_LIMIT or MFR_TON_SEQ_MAX fault. | Yes     |
| 1   | 0             | This bit always returns a 0.                  | —       |
| 0   | 0             | This bit always returns a 0.                  | —       |

**STATUS\_IOUT (7Bh)**

The STATUS\_IOUT command returns 1 byte of information with contents, as described in [Table 21](#). All the bits in STATUS\_IOUT are latched. When cleared, the bits are set again if the condition persists.

**STATUS\_TEMPERATURE (7Dh)**

The STATUS\_TEMPERATURE command returns 1 byte of information with contents, as described in [Table 22](#). All

the bits in STATUS\_VOUT are latched. When cleared, the bits are set again if the condition persists.

**STATUS\_CML (7Eh)**

The STATUS\_CML command returns 1 byte of information with contents, as described in [Table 23](#). The COMM\_FAULT, DATA\_FAULT, MAIN\_FAULT, and BACKUP\_FAULT bits are latched. When cleared, the bits are set again when the event occurs again. The FAULT\_LOG\_FULL bit reflects the current real-time state of the fault log.

**Table 21. STATUS\_IOUT (7Bh)**

| BIT | NAME          | MEANING                      | LATCHED |
|-----|---------------|------------------------------|---------|
| 7   | IOUT_OC_FAULT | IOUT overcurrent fault.      | Yes     |
| 6   | 0             | This bit always returns a 0. | —       |
| 5   | IOUT_OC_WARN  | IOUT overcurrent warning.    | Yes     |
| 4   | 0             | This bit always returns a 0. | —       |
| 3   | 0             | This bit always returns a 0. | —       |
| 2   | 0             | This bit always returns a 0. | —       |
| 1   | 0             | This bit always returns a 0. | —       |
| 0   | 0             | This bit always returns a 0. | —       |

**Table 22. STATUS\_TEMPERATURE (7Dh)**

| BIT | NAME     | MEANING                      | LATCHED |
|-----|----------|------------------------------|---------|
| 7   | OT_FAULT | Overtemperature fault.       | Yes     |
| 6   | OT_WARN  | Overtemperature warning.     | Yes     |
| 5   | 0        | This bit always returns a 0. | —       |
| 4   | 0        | This bit always returns a 0. | —       |
| 3   | 0        | This bit always returns a 0. | —       |
| 2   | 0        | This bit always returns a 0. | —       |
| 1   | 0        | This bit always returns a 0. | —       |
| 0   | 0        | This bit always returns a 0. | —       |

**Table 23. STATUS\_CML (7Eh)**

| BIT | NAME           | MEANING                                              | LATCHED |
|-----|----------------|------------------------------------------------------|---------|
| 7   | COMM_FAULT     | An invalid or unsupported command has been received. | Yes     |
| 6   | DATA_FAULT     | An invalid or unsupported data has been received.    | Yes     |
| 5   | 0              | This bit always returns a 0.                         | —       |
| 4   | 0              | This bit always returns a 0.                         | —       |
| 3   | 0              | This bit always returns a 0.                         | —       |
| 2   | BACKUP_FAULT   | Flash BACKUP memory array is corrupt.                | Yes     |
| 1   | MAIN_FAULT     | Flash MAIN memory array is corrupt.                  | Yes     |
| 0   | FAULT_LOG_FULL | MFR_NV_FAULT_LOG is full and needs to be cleared.    | No      |

**Notes:** When the NV fault log overwrite is enabled (NV\_LOG\_OVERWRITE = 1 in MFR\_MODE), FAULT\_LOG\_FULL is set when the fault log is full, but clears when the fault log is overwritten since two fault logs are cleared before each overwrite; the setting of the BACKUP\_FAULT and MAIN\_FAULT bits do not assert the ALERT signal.



**STATUS\_MFR\_SPECIFIC (80h)**

The STATUS\_MFR\_SPECIFIC message content varies based on the selected PAGE, and is described in [Table 24](#) and [Table 25](#).

**Table 24. STATUS\_MFR\_SPECIFIC (80h) (for PAGES 0–11)**

| BIT | NAME         | MEANING                                                                                                                                                                                                                                                                                                                                        | LATCHED |
|-----|--------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------|
| 7   | OFF          | For enabled channels, this bit reflects the output state of the sequencer and is set when PSENN is not asserted due to either a sequencing delay or a fault, or the power supply being turned off. This bit is always cleared when the channel is disabled. If PSENN is reconfigured as a GPO, this bit does not reflect the state of the pin. | No      |
| 6   | 0            | This bit always returns a 0.                                                                                                                                                                                                                                                                                                                   | —       |
| 5   | 0            | This bit always returns a 0.                                                                                                                                                                                                                                                                                                                   | —       |
| 4   | 0            | This bit always returns a 0.                                                                                                                                                                                                                                                                                                                   | —       |
| 3   | MARGIN_FAULT | This bit is set if the device cannot properly close-loop margin the power supply.                                                                                                                                                                                                                                                              | Yes     |
| 2   | POWER_GOOD#  | This bit is set when the power-supply voltage has fallen from POWER_GOOD_ON to less than POWER_GOOD_OFF. On device reset, this bit is set until the power supply is greater than POWER_GOOD_ON.                                                                                                                                                | No      |
| 1   | 0            | This bit always returns a 0.                                                                                                                                                                                                                                                                                                                   | —       |
| 0   | 0            | This bit always returns a 0.                                                                                                                                                                                                                                                                                                                   | —       |

**Note:** The setting of the OFF and POWER\_GOOD# bits do not assert the  $\overline{\text{ALERT}}$  signal.

**Table 25. STATUS\_MFR\_SPECIFIC (for PAGE 255)**

| BIT | NAME         | MEANING                                                                              | LATCHED |
|-----|--------------|--------------------------------------------------------------------------------------|---------|
| 7   | LOCK         | Set when the device is password protected (Note 1).                                  | No      |
| 6   | FAULT_INPUT  | Set each time any of the $\overline{\text{FAULT}}_n$ inputs are pulled low (Note 2). | Yes     |
| 5   | 0            | This bit always returns a 0.                                                         | —       |
| 4   | WATCHDOG_INT | Set upon device reset when the internal watchdog has caused the device reset.        | Yes     |
| 3   | CONTROL#     | Set each time the $\text{CONTROL}_n$ inputs are deasserted (Note 3).                 | Yes     |
| 2   | 0            | This bit always returns a 0.                                                         | —       |
| 1   | 0            | This bit always returns a 0.                                                         | —       |
| 0   | 0            | This bit always returns a 0.                                                         | —       |

**Note 1:** Setting the LOCK bit does not assert the  $\overline{\text{ALERT}}$  signal.

**Note 2:** Applies to all  $\overline{\text{FAULT}}_n$  inputs. The fault status bit is set even if the  $\overline{\text{FAULT}}_n$  pin is configured in MFR\_NV\_LOG\_CONFIG to ignore  $\overline{\text{FAULT}}_n$  pins. If FAULT1 and FAULT2 are disabled, they do not affect this bit.

**Note 3:** Either the CONTROL0 or CONTROL1 pin can set this bit. ON\_OFF\_CONFIG must be configured to use the  $\text{CONTROL}_n$  pins for this status bit to function.

**READ\_VOUT (8Bh)**

The READ\_VOUT command returns the actual measured(notcommanded)outputvoltage.READ\_VOUTis measured and updated every 5ms. If the RSn/GPIIn is configured to be a general-purpose input (GPI), by configuring the SELECT bits in MFR\_CHANNEL\_CONFIG to either 30h or 34h, then READ\_VOUT reports 0000h when the GPIIn input is inactive and 0001h when the GPIIn input is active. The 2 data bytes are in DIRECT format.

**READ\_IOUT (8Ch)**

The READ\_IOUT command returns the latest measured current value. READ\_IOUT is measured and updated every 5ms. The 2 data bytes are in DIRECT format.

**READ\_TEMPERATURE\_1 (8Dh)**

The READ\_TEMPERATURE\_1 command returns the temperature returned from the temperature sensor. READ\_TEMPERATURE\_1 returns 7FFFh if the sensor is faulty and 0000h if the sensor is disabled. READ\_TEMPERATURE\_1 is measured and updated once per second. The 2 data bytes are in DIRECT format.

**PMBUS\_REVISION (98h)**

The PMBUS\_REVISION command returns the revision of the PMBus specification to which the device is compliant. The command has 1 data byte. Bits 7:4 indicate the revision of the PMBus specification Part I to which the device is compliant. Bits 3:0 indicate the revision of the PMBus specification Part II to which the device is compliant. This command is read-only. The PMBUS\_REVISION value returned is always 11h, which indicates that the device is compliant with Part I, Rev 1.1 and Part II, Rev 1.1.

**MFR\_ID (99h)**

The MFR\_ID command returns the text (ISO/IEC 8859-1) character of the manufacturer's (Maxim) identification. The default MFR\_ID value is 4Dh (M). This command is read-only.

**MFR\_MODEL (9Ah)**

The MFR\_MODEL command returns the text (ISO/IEC 8859-1) character of the device model number. The default MFR\_MODEL value is 59h (Y). This command is read-only.

**MFR\_REVISION (9Bh)**

The MFR\_REVISION command returns two text (ISO/IEC 8859-1) characters that contain the device revision numbers for hardware (upper byte) and firmware (lower byte). This command is read-only.

**MFR\_LOCATION (9Ch)**

The MFR\_LOCATION command loads the device with text (ISO/IEC 8859-1) characters that identify the facility that manufactures the power supply. The maximum number of characters is 8. This data is written to internal flash using the STORE\_DEFAULT\_ALL command. The factory-default text string value is 10101010.

**MFR\_DATE (9Dh)**

The MFR\_DATE command loads the device with text (ISO/IEC 8859-1) characters that identify the date of manufacture of the power supply. The maximum number of characters is 8. This data is written to internal flash using the STORE\_DEFAULT\_ALL command. The factory-default text string value is 10101010.

**MFR\_SERIAL (9Eh)**

The MFR\_SERIAL command loads the device with text (ISO/IEC 8859-1) characters that uniquely identify the device. The maximum number of characters is 8. This data is written to internal flash using the STORE\_DEFAULT\_ALL command. The factory default text string value is 10101010. The upper 4 bytes of MFR\_SERIAL are used to unlock a device that has been password protected. The lower 4 bytes of MFR\_SERIAL are not used to unlock a device and they can be set to any value.

**MFR\_MODE (D1h)**

The MFR\_MODE command is used to configure the device to support manufacturer-specific commands. The MFR\_MODE command should not be changed while power supplies are operating. The MFR\_MODE command is described in [Table 26](#).

Table 26. MFR\_MODE (D1h)

| BIT                     | NAME                       | MEANING                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |                         |                            |                      |                  |      |                   |      |                   |      |                   |      |             |      |           |      |              |      |           |      |              |      |            |      |              |      |            |      |              |      |            |      |                |      |             |      |                |
|-------------------------|----------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------------------|----------------------------|----------------------|------------------|------|-------------------|------|-------------------|------|-------------------|------|-------------|------|-----------|------|--------------|------|-----------|------|--------------|------|------------|------|--------------|------|------------|------|--------------|------|------------|------|----------------|------|-------------|------|----------------|
| 15:14                   | 0                          | These bits always return a 0.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |                         |                            |                      |                  |      |                   |      |                   |      |                   |      |             |      |           |      |              |      |           |      |              |      |            |      |              |      |            |      |              |      |            |      |                |      |             |      |                |
| 13                      | ALERT                      | 0 = $\overline{\text{ALERT}}$ disabled (device does not respond to ARA).<br>1 = $\overline{\text{ALERT}}$ enabled (device does respond to ARA).                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |                         |                            |                      |                  |      |                   |      |                   |      |                   |      |             |      |           |      |              |      |           |      |              |      |            |      |              |      |            |      |              |      |            |      |                |      |             |      |                |
| 12                      | 0                          | This bit always returns a 0.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |                         |                            |                      |                  |      |                   |      |                   |      |                   |      |             |      |           |      |              |      |           |      |              |      |            |      |              |      |            |      |              |      |            |      |                |      |             |      |                |
| 11                      | SOFT_RESET                 | This bit must be set, then cleared and set again within 8ms for a soft reset to occur.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |                         |                            |                      |                  |      |                   |      |                   |      |                   |      |             |      |           |      |              |      |           |      |              |      |            |      |              |      |            |      |              |      |            |      |                |      |             |      |                |
| 10                      | LOCK                       | This bit must be set, then cleared and set again within 8ms for the device to become password protected. This bit is cleared when the password is unlocked. The device should only be locked and then unlocked a maximum of 256 times before either a device reset is issued or a device power cycle occurs.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |                         |                            |                      |                  |      |                   |      |                   |      |                   |      |             |      |           |      |              |      |           |      |              |      |            |      |              |      |            |      |              |      |            |      |                |      |             |      |                |
| 9:8                     | 0                          | These bits always return a 0.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |                         |                            |                      |                  |      |                   |      |                   |      |                   |      |             |      |           |      |              |      |           |      |              |      |            |      |              |      |            |      |              |      |            |      |                |      |             |      |                |
| 7:6                     | ADC_TIME[1:0]              | <div>These bits select the ADC conversion time:</div> <table><thead><tr><th><u>ADC_TIME[1:0]</u></th><th><u>ADC CONVERSION TIME</u></th></tr></thead><tbody><tr><td>00</td><td>1μs</td></tr><tr><td>01</td><td>2μs</td></tr><tr><td>10</td><td>4μs</td></tr><tr><td>11</td><td>8μs</td></tr></tbody></table>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          | <u>ADC_TIME[1:0]</u>    | <u>ADC CONVERSION TIME</u> | 00                   | 1μs              | 01   | 2μs               | 10   | 4μs               | 11   | 8μs               |      |             |      |           |      |              |      |           |      |              |      |            |      |              |      |            |      |              |      |            |      |                |      |             |      |                |
| <u>ADC_TIME[1:0]</u>    | <u>ADC CONVERSION TIME</u> |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |                         |                            |                      |                  |      |                   |      |                   |      |                   |      |             |      |           |      |              |      |           |      |              |      |            |      |              |      |            |      |              |      |            |      |                |      |             |      |                |
| 00                      | 1μs                        |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |                         |                            |                      |                  |      |                   |      |                   |      |                   |      |             |      |           |      |              |      |           |      |              |      |            |      |              |      |            |      |              |      |            |      |                |      |             |      |                |
| 01                      | 2μs                        |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |                         |                            |                      |                  |      |                   |      |                   |      |                   |      |             |      |           |      |              |      |           |      |              |      |            |      |              |      |            |      |              |      |            |      |                |      |             |      |                |
| 10                      | 4μs                        |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |                         |                            |                      |                  |      |                   |      |                   |      |                   |      |             |      |           |      |              |      |           |      |              |      |            |      |              |      |            |      |              |      |            |      |                |      |             |      |                |
| 11                      | 8μs                        |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |                         |                            |                      |                  |      |                   |      |                   |      |                   |      |             |      |           |      |              |      |           |      |              |      |            |      |              |      |            |      |              |      |            |      |                |      |             |      |                |
| 5:4                     | ADC_AVERAGE[1:0]           | <div>These bits select the post ADC conversion averaging:</div> <table><thead><tr><th><u>ADC_AVERAGE[1:0]</u></th><th><u>ADC AVERAGING</u></th></tr></thead><tbody><tr><td>00</td><td>No Averaging</td></tr><tr><td>01</td><td>Average 2 Samples</td></tr><tr><td>10</td><td>Average 4 Samples</td></tr><tr><td>11</td><td>Average 8 Samples</td></tr></tbody></table>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                | <u>ADC_AVERAGE[1:0]</u> | <u>ADC AVERAGING</u>       | 00                   | No Averaging     | 01   | Average 2 Samples | 10   | Average 4 Samples | 11   | Average 8 Samples |      |             |      |           |      |              |      |           |      |              |      |            |      |              |      |            |      |              |      |            |      |                |      |             |      |                |
| <u>ADC_AVERAGE[1:0]</u> | <u>ADC AVERAGING</u>       |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |                         |                            |                      |                  |      |                   |      |                   |      |                   |      |             |      |           |      |              |      |           |      |              |      |            |      |              |      |            |      |              |      |            |      |                |      |             |      |                |
| 00                      | No Averaging               |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |                         |                            |                      |                  |      |                   |      |                   |      |                   |      |             |      |           |      |              |      |           |      |              |      |            |      |              |      |            |      |              |      |            |      |                |      |             |      |                |
| 01                      | Average 2 Samples          |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |                         |                            |                      |                  |      |                   |      |                   |      |                   |      |             |      |           |      |              |      |           |      |              |      |            |      |              |      |            |      |              |      |            |      |                |      |             |      |                |
| 10                      | Average 4 Samples          |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |                         |                            |                      |                  |      |                   |      |                   |      |                   |      |             |      |           |      |              |      |           |      |              |      |            |      |              |      |            |      |              |      |            |      |                |      |             |      |                |
| 11                      | Average 8 Samples          |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |                         |                            |                      |                  |      |                   |      |                   |      |                   |      |             |      |           |      |              |      |           |      |              |      |            |      |              |      |            |      |              |      |            |      |                |      |             |      |                |
| 3:0                     | IOUT_AVG[3:0]              | <div>These bits determine the number of samples to average before reporting the value in MFR_IOUT_AVG:</div> <table><thead><tr><th><u>IOUT_AVG[3:0]</u></th><th><u>AVERAGING</u></th><th><u>IOUT_AVG[3:0]</u></th><th><u>AVERAGING</u></th></tr></thead><tbody><tr><td>0000</td><td>1 Sample</td><td>1000</td><td>256 Samples</td></tr><tr><td>0001</td><td>2 Samples</td><td>1001</td><td>512 Samples</td></tr><tr><td>0010</td><td>4 Samples</td><td>1010</td><td>1024 Samples</td></tr><tr><td>0011</td><td>8 Samples</td><td>1011</td><td>2048 Samples</td></tr><tr><td>0100</td><td>16 Samples</td><td>1100</td><td>4096 Samples</td></tr><tr><td>0101</td><td>32 Samples</td><td>1101</td><td>8192 Samples</td></tr><tr><td>0110</td><td>64 Samples</td><td>1110</td><td>16,384 Samples</td></tr><tr><td>0111</td><td>128 Samples</td><td>1111</td><td>32,768 Samples</td></tr></tbody></table> | <u>IOUT_AVG[3:0]</u>    | <u>AVERAGING</u>           | <u>IOUT_AVG[3:0]</u> | <u>AVERAGING</u> | 0000 | 1 Sample          | 1000 | 256 Samples       | 0001 | 2 Samples         | 1001 | 512 Samples | 0010 | 4 Samples | 1010 | 1024 Samples | 0011 | 8 Samples | 1011 | 2048 Samples | 0100 | 16 Samples | 1100 | 4096 Samples | 0101 | 32 Samples | 1101 | 8192 Samples | 0110 | 64 Samples | 1110 | 16,384 Samples | 0111 | 128 Samples | 1111 | 32,768 Samples |
| <u>IOUT_AVG[3:0]</u>    | <u>AVERAGING</u>           | <u>IOUT_AVG[3:0]</u>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  | <u>AVERAGING</u>        |                            |                      |                  |      |                   |      |                   |      |                   |      |             |      |           |      |              |      |           |      |              |      |            |      |              |      |            |      |              |      |            |      |                |      |             |      |                |
| 0000                    | 1 Sample                   | 1000                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  | 256 Samples             |                            |                      |                  |      |                   |      |                   |      |                   |      |             |      |           |      |              |      |           |      |              |      |            |      |              |      |            |      |              |      |            |      |                |      |             |      |                |
| 0001                    | 2 Samples                  | 1001                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  | 512 Samples             |                            |                      |                  |      |                   |      |                   |      |                   |      |             |      |           |      |              |      |           |      |              |      |            |      |              |      |            |      |              |      |            |      |                |      |             |      |                |
| 0010                    | 4 Samples                  | 1010                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  | 1024 Samples            |                            |                      |                  |      |                   |      |                   |      |                   |      |             |      |           |      |              |      |           |      |              |      |            |      |              |      |            |      |              |      |            |      |                |      |             |      |                |
| 0011                    | 8 Samples                  | 1011                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  | 2048 Samples            |                            |                      |                  |      |                   |      |                   |      |                   |      |             |      |           |      |              |      |           |      |              |      |            |      |              |      |            |      |              |      |            |      |                |      |             |      |                |
| 0100                    | 16 Samples                 | 1100                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  | 4096 Samples            |                            |                      |                  |      |                   |      |                   |      |                   |      |             |      |           |      |              |      |           |      |              |      |            |      |              |      |            |      |              |      |            |      |                |      |             |      |                |
| 0101                    | 32 Samples                 | 1101                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  | 8192 Samples            |                            |                      |                  |      |                   |      |                   |      |                   |      |             |      |           |      |              |      |           |      |              |      |            |      |              |      |            |      |              |      |            |      |                |      |             |      |                |
| 0110                    | 64 Samples                 | 1110                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  | 16,384 Samples          |                            |                      |                  |      |                   |      |                   |      |                   |      |             |      |           |      |              |      |           |      |              |      |            |      |              |      |            |      |              |      |            |      |                |      |             |      |                |
| 0111                    | 128 Samples                | 1111                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  | 32,768 Samples          |                            |                      |                  |      |                   |      |                   |      |                   |      |             |      |           |      |              |      |           |      |              |      |            |      |              |      |            |      |              |      |            |      |                |      |             |      |                |

**MFR\_PSEN\_CONFIG (D2h)**

The MFR\_PSEN\_CONFIG command is used to configure the individual PSEn/GPOn (where n = 0–11) outputs. This command should not be changed while the power supplies are operating. The MFR\_PSEN\_CONFIG command is described in [Table 27](#) and shown in [Figure 8](#).

Each PSEn/GPOn pin can be independently configured using the SELECT[2:0] bits to one of the following:

- Enable and disabled power supplies (SELECT[2:0] = 000)
- Force pin assertion (SELECT[2:0] = 001)
- Force pin deassertion (SELECT[2:0] = 010)
- Assert when all enabled channel power-good (PG) or GPI are asserted (SELECT[2:0] = 011)
- Assert when any enabled alarm goes active (SELECT[2:0] = 100)

If the PSEn/GPOn output is configured to enable and disable power supplies (SELECT[2:0] = 000), then the associated input channel must also be configured to monitor voltage and to sequence by setting the SELECT bits in MFR\_CHANNEL\_CONFIG to 10h. See the *MFR\_CHANNEL\_CONFIG (E4h)* for more details.

Also, each PSEn/GPOn pin can be independently configured to be active high or active low and either push-pull or open drain using the HI\_LO and PP\_OD bits, respectively.

If SELECT[2:0] = 011, the PSEn/GPOn output is configured to assert when some combination of power goods (PGs) and general-purpose inputs (GPIs) from each channel are asserted. The channels that should be used in this combination are selected using the PG\_GPI\_SELECT bits 31:16. If the PG\_GPI\_SELECT bit is cleared, then the associated channel is not used in the logical combination to assert the GPOn output. If the PG\_GPI\_SELECT bit is set, then the PG or GPI from this channel is used in the logical combination to assert the GPOn output. This function is useful in creating system power-good signals.

If SELECT[2:0] = 100, the PSEn/GPOn output is configured to assert when any of the enabled channel alarms goes active. The channel alarms are enabled with the ALARM\_SELECT bits 31:16. If the ALARM\_SELECT bit is cleared, then the alarm from this channel is blocked. If the ALARM\_SELECT bit is set, the alarm from this channel is routed to an OR function such that any enabled alarm asserts the GPOn output. The alarm function is chosen with the ALARM\_CONFIG bits in the MFR\_FAULT\_RESPONSE command. This function is useful in system debug or for enabling system status LEDs.

**Table 27. MFR\_PSEN\_CONFIG (D2h)**

| BIT   | NAME                          | MEANING                                                                                                                                                                                                                                                              |
|-------|-------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:16 | PG_GPI_SELECT<br>ALARM_SELECT | These bits are only used if SELECT[2:0] = 011 or 100. Each bit corresponds to one channel (device channel N + 16 = bit number):                                                                                                                                      |
|       |                               | <div><div><u>SELECT[2:0]</u></div><div>011</div></div> <div><u>BIT FUNCTION</u><br/>When this bit is cleared, the power good (PG) or GPI from channel N is not used in the logical AND to assert the GPON output. When this bit is set, the PG or GPI is used.</div> |
|       |                               | <div><div>100</div></div> <div>When this bit is cleared, the alarm from channel N is blocked from the logical OR to assert the GPON output. When this bit is set, the alarm signal is routed to the logical OR.</div>                                                |
| 15:8  | 0                             | These bits always return a 0.                                                                                                                                                                                                                                        |
| 7     | PP_OD                         | 0 = PSEN/GPO push-pull output<br>1 = PSEN/GPO open-drain output                                                                                                                                                                                                      |
| 6     | HI_LO                         | 0 = PSEN/GPO active low<br>1 = PSEN/GPO active high                                                                                                                                                                                                                  |
| 5:3   | 0                             | These bits always return a 0.                                                                                                                                                                                                                                        |

Table 27. MFR\_PSEN\_CONFIG (D2h) (continued)

| BIT | NAME        | MEANING                                                                                           |
|-----|-------------|---------------------------------------------------------------------------------------------------|
| 2:0 | SELECT[2:0] | These bits determine the function selected on the pin:                                            |
|     |             | <u>SELECT[2:0]</u> <u>PSEn/GPOn PIN FUNCTION SELECTED</u>                                         |
|     |             | 000                  PSEN operation.*                                                             |
|     |             | 001                  Force GPO assertion.                                                         |
|     |             | 010                  Force GPO deassertion.                                                       |
|     |             | 011                  PG/GPI operation (use bits 31:16).                                           |
|     |             | 100                  Alarm operation (use bits 31:16).                                            |
|     |             | 101 <u>FAULT2</u> special function (only PAGE 10);<br><u>SEQ</u> special function (only PAGE 11). |
|     |             | 11x                  Reserved.                                                                    |

\*For proper sequencing, the SELECT bits in MFR\_CHANNEL\_CONFIG must set to 10h.

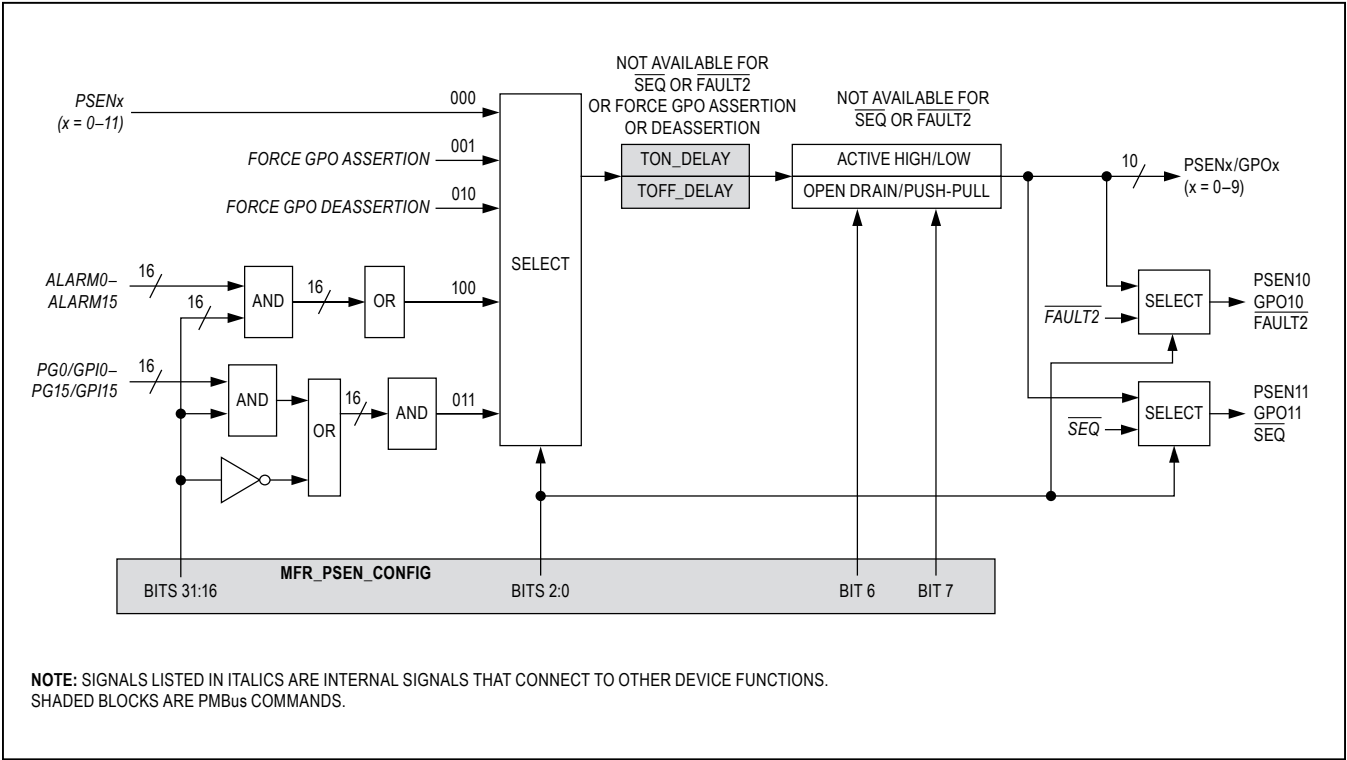


Figure 8. MFR\_PSEN\_CONFIG Functional Logic

**Delay Function**

If a delay is configured either on or off, the input must be continuously static through the delay time before the output changes state. See the [Figure 9](#).

**MFR\_VOUT\_PEAK (D4h)**

The MFR\_VOUT\_PEAK command returns the maximum actual measured output voltage. To reset this value to 0, write to this command with a data value of 0. Any values written to this command are used as a comparison for future peak updates. The 2 data bytes are in DIRECT format.

**MFR\_IOUT\_PEAK (D5h)**

The MFR\_IOUT\_PEAK command returns the maximum actual measured current. To reset this value to 0, write to this command with a data value of 0. Any values written to this command are used as a comparison for future peak updates. The 2 data bytes are in DIRECT format.

**MFR\_TEMPERATURE\_PEAK (D6h)**

The MFR\_TEMPERATURE\_PEAK command returns the maximum measured temperature. To reset this value to its lowest value, write to this command with a data value

of 8000h. Any other values written by this command are used as a comparison for future peak updates. The 2 data bytes are in DIRECT format.

**MFR\_VOUT\_MIN (D7h)**

The MFR\_VOUT\_MIN command returns the minimum actual measured output voltage. To reset this value, write to this command with a data value of 7FFFh. Any values written to this command are used as a comparison for future minimum updates. The 2 data bytes are in DIRECT format.

**MFR\_IOUT\_AVG (E2h)**

The MFR\_IOUT\_AVG command returns the calculated average current. The number of samples collected in the average before reporting the value in MFR\_IOUT\_AVG is configured using the IOUT\_AVG bits in MFR\_MODE. Writes to this command are ignored. The 2 data bytes are in DIRECT format.

**MFR\_NV\_LOG\_CONFIG (D8h)**

The MFR\_NV\_LOG\_CONFIG command is used to configure the operation of the nonvolatile fault logging in the device. The MFR\_NV\_LOG\_CONFIG command is described in [Table 28](#).

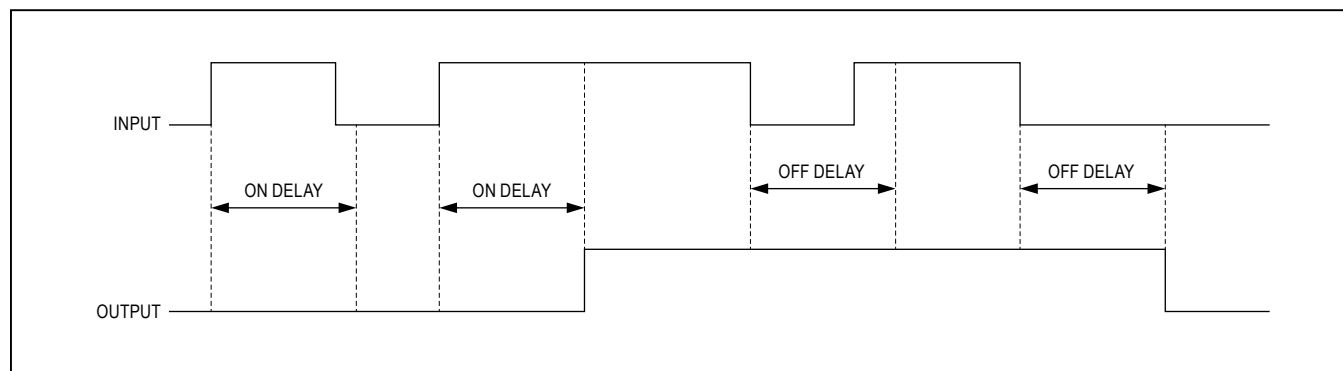


Figure 9. Input-to-Output Delay Action

Table 28. MFR\_NV\_LOG\_CONFIG (D8h)

| BIT                   | NAME               | MEANING                                                                                                                                                                                                                                                                                                                                                                                                                                                    |                       |  |  |                   |          |                    |    |     |      |    |      |      |    |      |       |    |       |       |
|-----------------------|--------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------|--|--|-------------------|----------|--------------------|----|-----|------|----|------|------|----|------|-------|----|-------|-------|
| 15                    | FORCE_NV_FAULT_LOG | Setting this bit to a 1, forces the device to log data into the nonvolatile fault log. Once set, the device clears this bit when the action is completed. Host must set again for subsequent action. If an error occurs during this action, the device sets the CML bit in STATUS_WORD; no bits are set in STATUS_CML.                                                                                                                                     |                       |  |  |                   |          |                    |    |     |      |    |      |      |    |      |       |    |       |       |
| 14                    | CLEAR_NV_FAULT_LOG | Setting this bit to a 1, forces the device to clear the nonvolatile fault log by writing FFh to all byte locations. Once set, the device clears this bit when the action is completed. Host must set again for subsequent action. If an error occurs during this action, the device sets the CML bit in STATUS_WORD; no bits are set in STATUS_CML. While clearing the fault log, monitoring is stopped and commands should not be sent to the PMBus port. |                       |  |  |                   |          |                    |    |     |      |    |      |      |    |      |       |    |       |       |
| 13:11                 | 0                  | These bits always return a 0.                                                                                                                                                                                                                                                                                                                                                                                                                              |                       |  |  |                   |          |                    |    |     |      |    |      |      |    |      |       |    |       |       |
| 10                    | NV_LOG_T0_CONFIG   | This bit determines the source of the data written into the T0 location of each page when a nonvolatile fault log is written.<br>0 = Log the last regular collection interval ADC reading<br>1 = Read the latest ADC value before logging                                                                                                                                                                                                                  |                       |  |  |                   |          |                    |    |     |      |    |      |      |    |      |       |    |       |       |
| 9                     | NV_LOG_OVERWRITE   | 0 = Do not overwrite the NV fault log<br>1 = Overwrite the NV fault log once it is full*                                                                                                                                                                                                                                                                                                                                                                   |                       |  |  |                   |          |                    |    |     |      |    |      |      |    |      |       |    |       |       |
| 8:7                   | NV_LOG_DEPTH[1:0]  | These bits determine the depth of the NV fault log:<br><table> <tr> <th colspan="3">ADC RESULT COLLECTION</th></tr> <tr> <th>NV_LOG_DEPTH[1:0]</th><th>INTERVAL</th><th>NV FAULT LOG DEPTH</th></tr> <tr> <td>00</td><td>5ms</td><td>15ms</td></tr> <tr> <td>01</td><td>20ms</td><td>60ms</td></tr> <tr> <td>10</td><td>80ms</td><td>240ms</td></tr> <tr> <td>11</td><td>160ms</td><td>480ms</td></tr> </table>                                            | ADC RESULT COLLECTION |  |  | NV_LOG_DEPTH[1:0] | INTERVAL | NV FAULT LOG DEPTH | 00 | 5ms | 15ms | 01 | 20ms | 60ms | 10 | 80ms | 240ms | 11 | 160ms | 480ms |
| ADC RESULT COLLECTION |                    |                                                                                                                                                                                                                                                                                                                                                                                                                                                            |                       |  |  |                   |          |                    |    |     |      |    |      |      |    |      |       |    |       |       |
| NV_LOG_DEPTH[1:0]     | INTERVAL           | NV FAULT LOG DEPTH                                                                                                                                                                                                                                                                                                                                                                                                                                         |                       |  |  |                   |          |                    |    |     |      |    |      |      |    |      |       |    |       |       |
| 00                    | 5ms                | 15ms                                                                                                                                                                                                                                                                                                                                                                                                                                                       |                       |  |  |                   |          |                    |    |     |      |    |      |      |    |      |       |    |       |       |
| 01                    | 20ms               | 60ms                                                                                                                                                                                                                                                                                                                                                                                                                                                       |                       |  |  |                   |          |                    |    |     |      |    |      |      |    |      |       |    |       |       |
| 10                    | 80ms               | 240ms                                                                                                                                                                                                                                                                                                                                                                                                                                                      |                       |  |  |                   |          |                    |    |     |      |    |      |      |    |      |       |    |       |       |
| 11                    | 160ms              | 480ms                                                                                                                                                                                                                                                                                                                                                                                                                                                      |                       |  |  |                   |          |                    |    |     |      |    |      |      |    |      |       |    |       |       |
| N                     | NV_LOG_FAULT0      | 0 = Do not write NV fault log when $\overline{\text{FAULT0}}$ pin is externally pulled low.<br>1 = Write NV fault log when $\overline{\text{FAULT0}}$ pin is externally pulled low.                                                                                                                                                                                                                                                                        |                       |  |  |                   |          |                    |    |     |      |    |      |      |    |      |       |    |       |       |
| 5                     | NV_LOG_FAULT1      | 0 = Do not write NV fault log when $\overline{\text{FAULT1}}$ pin is externally pulled low.<br>1 = Write NV fault log when $\overline{\text{FAULT1}}$ pin is externally pulled low and the $\overline{\text{FAULT1}}$ pin is enabled.                                                                                                                                                                                                                      |                       |  |  |                   |          |                    |    |     |      |    |      |      |    |      |       |    |       |       |
| 4                     | NV_LOG_FAULT2      | 0 = Do not write NV fault log when $\overline{\text{FAULT2}}$ pin is externally pulled low.<br>1 = Write NV fault log when $\overline{\text{FAULT2}}$ pin is externally pulled low and the $\overline{\text{FAULT2}}$ pin is enabled.                                                                                                                                                                                                                      |                       |  |  |                   |          |                    |    |     |      |    |      |      |    |      |       |    |       |       |
| 3:0                   | 0                  | These bits always return a 0.                                                                                                                                                                                                                                                                                                                                                                                                                              |                       |  |  |                   |          |                    |    |     |      |    |      |      |    |      |       |    |       |       |

\*The device clears two fault logs at a time when overwrite is enabled.



**MFR\_FAULT\_RESPONSE (D9h)**

The MFR\_FAULT\_RESPONSE command specifies the response to each fault or warning condition supported by the device. In response to a fault/warning, the device always reports the fault/warning in the appropriate status register and asserts the  $\overline{\text{ALERT}}$  output (if enabled in MFR\_MODE). A CML fault cannot cause any device action other than setting the status bit and asserting the  $\overline{\text{ALERT}}$  output. The MFR\_FAULT\_RESPONSE command is described in [Table 30](#) and shown in [Figure 10](#).

For each fault type (overvoltage or overcurrent, undervoltage, sequencing error, and overtemperature), each channel can be independently configured to respond in the required manner with the RESPONSE bits in MFR\_FAULT\_RESPONSE. If channels 0–11 are configured to latch off for a particular fault, the channel turns off (either immediately or after the TOFF\_DELAY as configured or commanded) and also assert one or more of the  $\overline{\text{FAULTn}}$  pins if they are enabled with bits 18:16 in MFR\_FAULT\_RESPONSE. The channel remains off and the  $\overline{\text{FAULTn}}$  outputs remain asserted until either the master power control is toggled using the OPERATION command or CONTROLn pins as configured in the ON\_OFF\_CONFIG command or the device is reset or power cycled. When the device attempts to sequence the power supplies on, all enabled faults must be cleared before the channel is allowed to power-on or the  $\overline{\text{FAULTn}}$  pins deasserted. If channels 12–15 are configured to latch off, they respond like channels 0–11; however, all the power supplies must be turned off before they are allowed to turn back on.

If the channel is configured to retry for a particular fault, the channel turns off (either immediately or after the TOFF\_DELAY as configured or commanded) and also assert one or more the  $\overline{\text{FAULTn}}$  pins if they are enabled with bits 18:16 in MFR\_FAULT\_RESPONSE. The channel remains off and the  $\overline{\text{FAULTn}}$  outputs remain asserted for the time configured in MFR\_FAULT\_RETRY. After the time in MFR\_FAULT\_RETRY expires, the device attempts to sequence the power supplies back on as long as all the enabled faults in the channel are cleared. If all the enabled faults are cleared, then the device deasserts all the  $\overline{\text{FAULTn}}$  pins it asserted and as long as no other channels have asserted the  $\overline{\text{FAULTn}}$  pins it has been

configured to monitor with bits 26:24 in MFR\_FAULT\_RESPONSE, the power-up sequencing begins.

Global channels must assert a  $\overline{\text{FAULTn}}$  pin and respond to that  $\overline{\text{FAULTn}}$  pin for the channel to shut down.

**LOCAL vs. GLOBAL Channels**

With the MFR\_FAULT\_RESPONSE command (bit 14), each power-supply channel can be tagged as either being LOCAL or GLOBAL. When bit 14 is cleared, the channel is configured as a LOCAL channel, which means that a detected fault only affects this channel (or page). With the RESPONSE bits in the MFR\_FAULT\_RESPONSE command, the device can be configured to respond differently to each possible fault. When bit 14 is set, the channel is configured as a GLOBAL channel which means that a detected fault on this channel can assert all enabled  $\overline{\text{FAULTn}}$  outputs. The  $\overline{\text{FAULTn}}$  outputs that are enabled are selected with bits 18:16. Only GLOBAL channels respond to  $\overline{\text{FAULTn}}$  pins that are asserted. The  $\overline{\text{FAULTn}}$  pins that the channel should respond to are assigned with bits 26:24. LOCAL channels do not respond to the fault pins.

**GLOBAL Channels Respond to  $\overline{\text{FAULTn}}$  Assertion**

Bits 26:24 in the MFR\_FAULT\_RESPONSE command are used to configure GLOBAL channels to respond or ignore one or more of the  $\overline{\text{FAULTn}}$  pins when they are asserted. When one or more of the enabled  $\overline{\text{FAULTn}}$  pins is asserted, the channel either deasserts the PSENn output immediately or after the TOFF\_DELAY according to the configuration of bit 0 in the ON\_OFF\_CONFIG command. The channel continues to deassert the PSENn output until all enabled  $\overline{\text{FAULTn}}$  pins deassert. When all enabled  $\overline{\text{FAULTn}}$  pins deassert, the channel sequences on as configured if no channel faults are present.

**Temperature Fault Response**

A temperature fault is declared when any of the enabled temperature sensors detect a fault. A temperature fault acts globally and can affect all of the power supplies. For all global supplies, the worst-case fault response of all global channels is applied. If this response is latching or retry, all  $\overline{\text{FAULTn}}$  pins that are programmed to be asserted by any of the global channels will be asserted. All local channels respond independently, as programmed in that channel's MFR\_FAULT\_RESPONSE.



**Fault Detection Before Power-On Sequencing**

Before any power-supply channel is enabled or  $\overline{\text{FAULTn}}$  output deasserted, the device checks for overvoltage, overcurrent, and overtemperature faults (but not for undervoltage) if the channel is configured for a fault response to either latch off ( $\text{RESPONSE}[1:0] = 01$ ) or retry ( $\text{RESPONSE}[1:0] = 10$ ) in the  $\text{MFR\_FAULT\_RESPONSE}$  command. Undervoltage faults are detected when the power supply turns on and fails to reach the power-good level, and the  $\text{TON\_MAX\_FAULT\_LIMIT}$  is exceeded and the device takes fault action as configured. See [Table 29](#).

**Logging Faults into MFR\_NV\_FAULT\_LOG**

If bit 15 of  $\text{MFR\_FAULT\_RESPONSE}$  is set, faults are logged into the on-board nonvolatile fault log for this channel unless the response for the associated fault is configured to take no action ( $\text{RESPONSE}[1:0] = 00$ ). To keep from needlessly filling the fault log with excessive data, the following rules are applied when subsequent faults occur. When overvoltage faults occurs, subsequent overvoltage faults on this channel are not written to the fault log until either the  $\text{CLEAR\_FAULTS}$  command is issued or a device reset occurs. The same rule applies to overcurrent, undervoltage, overtemperature, and sequencing faults (see [Table 30](#) and [Figure 10](#)).

**Table 29. Fault Monitoring States**

| FAULT           | REQUIRED DEVICE CONFIGURATION<br>FOR ACTIVE MONITORING                                                                                                                                               | WHEN MONITORED                                                                                                          |
|-----------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------------------------------------------------------------------------------------------------------------------|
| Overvoltage     | <ul style="list-style-type: none"><li>Voltage Monitoring Enabled<br/>(<math>\text{SELECT}[5:0] = 10\text{h}</math> or <math>20\text{h}</math> in <math>\text{MFR\_CHANNEL\_CONFIG}</math>)</li></ul> | Continuous monitoring                                                                                                   |
| Undervoltage    | <ul style="list-style-type: none"><li>Voltage Monitoring Enabled<br/>(<math>\text{SELECT}[5:0] = 10\text{h}</math> or <math>20\text{h}</math> in <math>\text{MFR\_CHANNEL\_CONFIG}</math>)</li></ul> | Stop monitoring while the power supply is off; start monitoring when voltage exceeds the $\text{POWER\_GOOD\_ON}$ level |
| Overcurrent     | <ul style="list-style-type: none"><li>Current Monitoring Enabled<br/>(<math>\text{SELECT}[5:0] = 22\text{h}</math> in <math>\text{MFR\_CHANNEL\_CONFIG}</math>)</li></ul>                            | Continuous monitoring                                                                                                   |
| Power-Up Time   | <ul style="list-style-type: none"><li>Sequencing Enabled<br/>(<math>\text{SELECT}[5:0] = 10\text{h}</math> in <math>\text{MFR\_CHANNEL\_CONFIG}</math>)</li></ul>                                    | Monitored only during power on sequence                                                                                 |
| Overtemperature | <ul style="list-style-type: none"><li>Temperature Sensor Enabled<br/>(<math>\text{ENABLE} = 1</math> in <math>\text{MFR\_TEMP\_SENSOR\_CONFIG}</math>)</li></ul>                                     | Continuous monitoring                                                                                                   |

**Note:** Device response to faults is determined by the configuration of  $\text{MFR\_FAULT\_RESPONSE}$ .

Table 30. MFR\_FAULT\_RESPONSE (D9h)

| BIT   | NAME                                                                   | MEANING                                                                                                                                             |
|-------|------------------------------------------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:27 | 0                                                                      | These bits always return a 0.                                                                                                                       |
| 26    | FAULT2_RESPONSE_ENABLE                                                 | 0 = $\overline{\text{FAULT2}}$ response disabled<br>1 = $\overline{\text{FAULT2}}$ response enabled                                                 |
| 25    | FAULT1_RESPONSE_ENABLE                                                 | 0 = $\overline{\text{FAULT1}}$ response disabled<br>1 = $\overline{\text{FAULT1}}$ response enabled                                                 |
| 24    | FAULT0_RESPONSE_ENABLE                                                 | 0 = $\overline{\text{FAULT0}}$ response disabled<br>1 = $\overline{\text{FAULT0}}$ response enabled                                                 |
| 23:19 | 0                                                                      | These bits always return a 0.                                                                                                                       |
| 18    | FAULT2_ASSERT_ENABLE                                                   | 0 = $\overline{\text{FAULT2}}$ assertion disabled<br>1 = $\overline{\text{FAULT2}}$ assertion enabled                                               |
| 17    | FAULT1_ASSERT_ENABLE                                                   | 0 = $\overline{\text{FAULT1}}$ assertion disabled<br>1 = $\overline{\text{FAULT1}}$ assertion enabled                                               |
| 16    | FAULT0_ASSERT_ENABLE                                                   | 0 = $\overline{\text{FAULT0}}$ assertion disabled<br>1 = $\overline{\text{FAULT0}}$ assertion enabled                                               |
| 15    | NV_LOG                                                                 | 0 = Do not log the fault into MFR_NV_FAULT_LOG<br>1 = Log the fault into MFR_NV_FAULT_LOG                                                           |
| 14    | GLOBAL                                                                 | 0 = LOCAL (affect only the selected page)<br>1 = GLOBAL (Note 1).                                                                                   |
| 13:12 | FILTER[1:0]                                                            | Continuous excursion time before a fault or warning is declared and action is taken (Note 2).<br>00 = Immediate<br>01 = 2ms<br>10 = 3ms<br>11 = 4ms |
| 11    | 0                                                                      | This bit always returns a 0.                                                                                                                        |
| 10:8  | ALARM_CONFIG[2:0]                                                      | See Table 31.                                                                                                                                       |
| 7:6   | OT_FAULT_LIMIT_RESPONSE[1:0]                                           | See Tables 32 and 33 (Note 3).                                                                                                                      |
| 5:4   | TON_MAX_FAULT_LIMIT_RESPONSE[1:0]<br>(also applies to MFR_TON_SEQ_MAX) | See Tables 32 and 33 (Notes 4 and 5).                                                                                                               |
| 3:2   | VOUT_UV_FAULT_LIMIT_RESPONSE[1:0]                                      | See Tables 32 and 33 (Note 4).                                                                                                                      |
| 1:0   | VOUT_OV_FAULT_LIMIT_RESPONSE[1:0]<br>IOUT_OC_FAULT_LIMIT_RESPONSE[1:0] | See Tables 32 and 33 (Note 6).                                                                                                                      |

**Note 1:** Channels configured to monitor current must be configured as GLOBAL. Also PAGES 12–15 must be configured as GLOBAL.

**Note 2:** The FILTER selection does not apply to temperature or sequencing faults.

**Note 3:** All enabled temperature sensor faults are logically ORed together.

**Note 4:** If the channel is configured to measure current, these bits are ignored.

**Note 5:** These bits are ignored for PAGES 12–15.

**Note 6:** Depends on whether the channel is configured to monitor voltage or current.

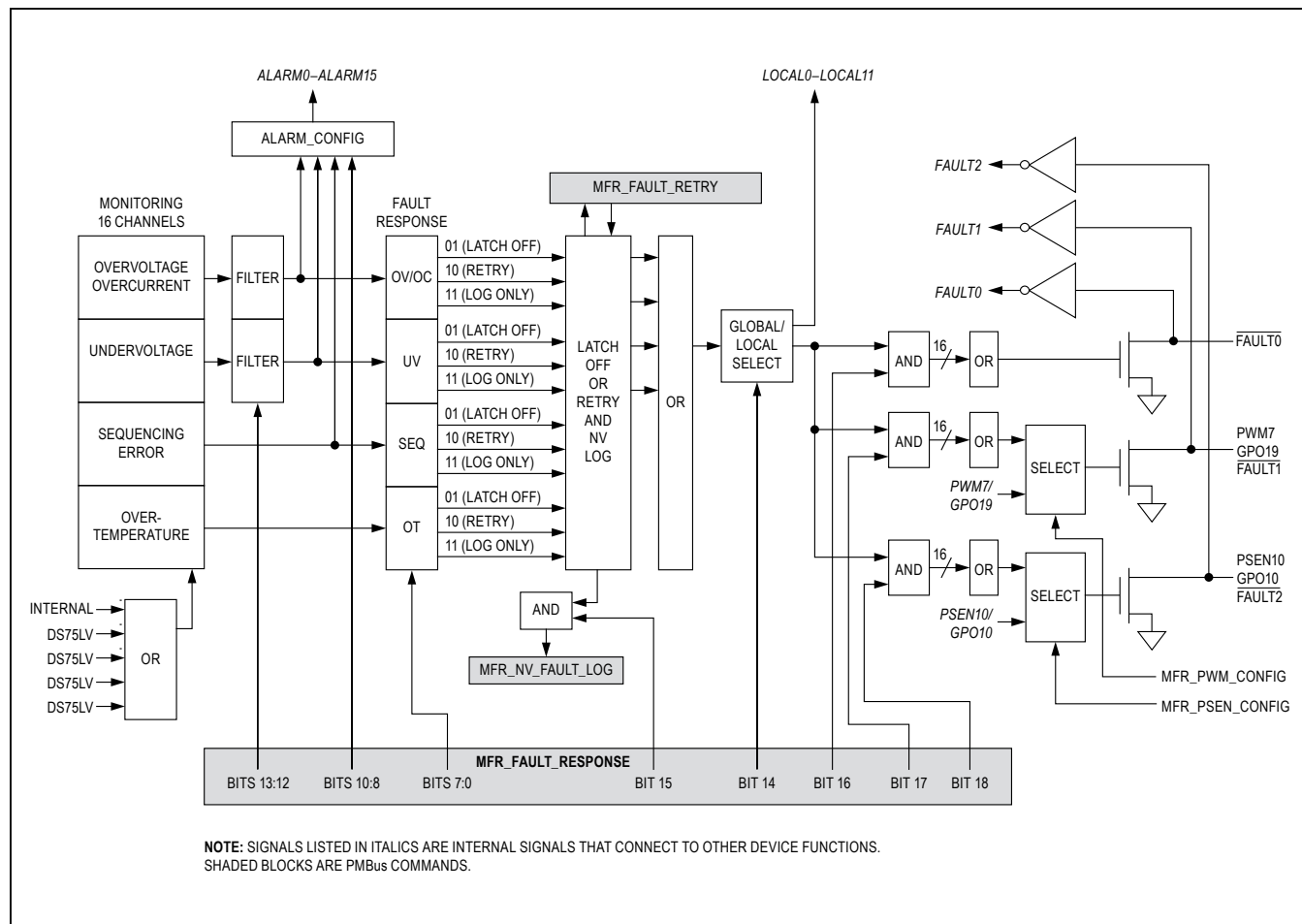


Figure 10. MFR\_FAULT\_RESPONSE Operation

Table 31. ALARM\_CONFIG Codes

| ALARM_CONFIG[2:0] | ALARM CONDITION                         | ALARM CRITERIA   |
|-------------------|-----------------------------------------|------------------|
| 000               | None                                    | —                |
| 001               | Sequencing fault                        | Fault only       |
| 010               | Undervoltage only                       | Fault only       |
| 011               | Undervoltage only                       | Fault or warning |
| 100               | Overvoltage/overcurrent only            | Fault only       |
| 101               | Overvoltage/overcurrent only            | Fault or warning |
| 110               | Undervoltage or overvoltage/overcurrent | Fault only       |
| 111               | Undervoltage or overvoltage/overcurrent | Fault or warning |

**Table 32. MFR\_FAULT\_RESPONSE Codes for GLOBAL Channels**

| RESPONSE[1:0]     | FAULT RESPONSE                                                                                                                                                                                                                                                                                                                                                                                                                                           |
|-------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 11                | <ul style="list-style-type: none"> <li>• Sets the corresponding fault bit in the appropriate status register (Note 1).</li> <li>• Logs fault into MFR_NV_FAULT_LOG if NV_LOG = 1.</li> <li>• Continues operation.</li> </ul>                                                                                                                                                                                                                             |
| 10<br>(Retry)     | <ul style="list-style-type: none"> <li>• Asserts all enabled <math>\overline{\text{FAULT}}_n</math> outputs.</li> <li>• Sets the corresponding fault bit in the appropriate status register (Note 1).</li> <li>• Logs fault into MFR_NV_FAULT_LOG if NV_LOG = 1.</li> <li>• Waits for the time configured in MFR_FAULT_RETRY and then deasserts the <math>\overline{\text{FAULT}}_n</math> outputs that were asserted if fault-free (Note 2).</li> </ul> |
| 01<br>(Latch off) | <ul style="list-style-type: none"> <li>• Asserts all enabled <math>\overline{\text{FAULT}}_n</math> outputs.</li> <li>• Sets the corresponding fault bit in the appropriate status register (Note 1).</li> <li>• Logs fault into MFR_NV_FAULT_LOG if NV_LOG = 1.</li> </ul>                                                                                                                                                                              |
| 00                | <ul style="list-style-type: none"> <li>• Sets the corresponding fault bit in the appropriate status register (Note 1).</li> <li>• Continues operation without any action.</li> </ul>                                                                                                                                                                                                                                                                     |

**Note 1:**  $\overline{\text{ALERT}}$  is asserted if enabled when a new status bit is set. A status bit is latched when a particular fault occurs that causes a fault response.

**Note 2:** Fault-free does not include undervoltage.

**Table 33. MFR\_FAULT\_RESPONSE Codes for LOCAL Channels**

| RESPONSE[1:0]     | FAULT RESPONSE                                                                                                                                                                                                                                                                                                                                                                   |
|-------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 11                | <ul style="list-style-type: none"> <li>• Sets the corresponding fault bit in the appropriate status register (Note 1).</li> <li>• Logs fault into MFR_NV_FAULT_LOG if NV_LOG = 1.</li> <li>• Continues operation.</li> </ul>                                                                                                                                                     |
| 10<br>(Retry)     | <ul style="list-style-type: none"> <li>• Shuts down the power supply by deasserting the PSENn output.</li> <li>• Sets the corresponding fault bit in the appropriate status register (Note 1).</li> <li>• Logs fault into MFR_NV_FAULT_LOG if NV_LOG = 1.</li> <li>• Waits for the time configured in MFR_FAULT_RETRY and restarts the supply if fault-free (Note 2).</li> </ul> |
| 01<br>(Latch off) | <ul style="list-style-type: none"> <li>• Latches off the power supply by deasserting the PSENn output.</li> <li>• Sets the corresponding fault bit in the appropriate status register (Note 1).</li> <li>• Logs fault into MFR_NV_FAULT_LOG if NV_LOG = 1.</li> </ul>                                                                                                            |
| 00                | <ul style="list-style-type: none"> <li>• Sets the corresponding fault bit in the appropriate status register (Note 1).</li> <li>• Continues operation without any action.</li> </ul>                                                                                                                                                                                             |

**Note 1:**  $\overline{\text{ALERT}}$  is asserted if enabled when a new status bit is set. A status bit is latched when a particular fault occurs that causes a fault response.

**Note 2:** Fault-free does not include undervoltage.

**Alarm Output Functionality**

Any of the GPOn pins can be configured to output the alarm signals. See the MFR\_PWM\_CONFIG and MFR\_PSEN\_CONFIG commands for details. When an undervoltage or overvoltage/overcurrent alarm is occurring, the output remains asserted as long as the alarm continues. When a sequencing fault occurs, the alarm pin remains asserted until either a CLEAR\_FAULTS command is received, or a master power control off input is received with either the OPERATION command or the CONTROLn pins.

**MFR\_FAULT\_RETRY (DAh)**

The MFR\_FAULT\_RETRY command sets the delay time between a fault occurring that results in a power supply being shut down for retry and the power supply restarting. This command value is used for all fault responses that require delay retry. The retry timer starts when the fault occurs. If the faulty channel has been configured to assert one or more FAULTn pins, the FAULTn pins are asserted until the retry timer expires, and then they are allowed to deassert as long as no enabled faults are still present and no other channel sharing the same FAULTn pins have not also asserted. MFR\_FAULT\_RETRY should be configured with a value larger than the largest system TOFF\_DELAY. The 2 data bytes are in DIRECT format.

**MFR\_NV\_FAULT\_LOG (DCh)**

Each time the MFR\_NV\_FAULT\_LOG command is executed, the device returns a block of 255 bytes containing one of the 15 nonvolatile fault logs. The MFR\_NV\_FAULT\_LOG command must be executed 15 times to dump the complete nonvolatile fault log. If the returned fault log is all FFs (except bytes 0 and 1), this indicates that this fault log has not been written by the device. As the device is operating, it is reading the latest operating conditions for voltage, current, and temperature and updating the status registers. All this information is stored in on-board RAM. When a fault is detected (if so enabled in MFR\_FAULT\_RESPONSE), the device automatically logs this information to one of the 15 nonvolatile fault logs. After 15 faults have been written, bit 0 of STATUS\_CML is set and the device can be configured (with the NV\_LOG\_OVERWRITE bit in MFR\_NV\_LOG\_CONFIG) to either stop writing additional fault logs or write over the oldest data. The host can clear the fault log by setting the CLEAR\_NV\_FAULT\_LOG bit in MFR\_NV\_LOG\_CONFIG. If a power supply is not enabled to measure voltage, current, or if a temperature sensor is disabled, the associated fault log position returns 0000h (see [Figure 11](#)).

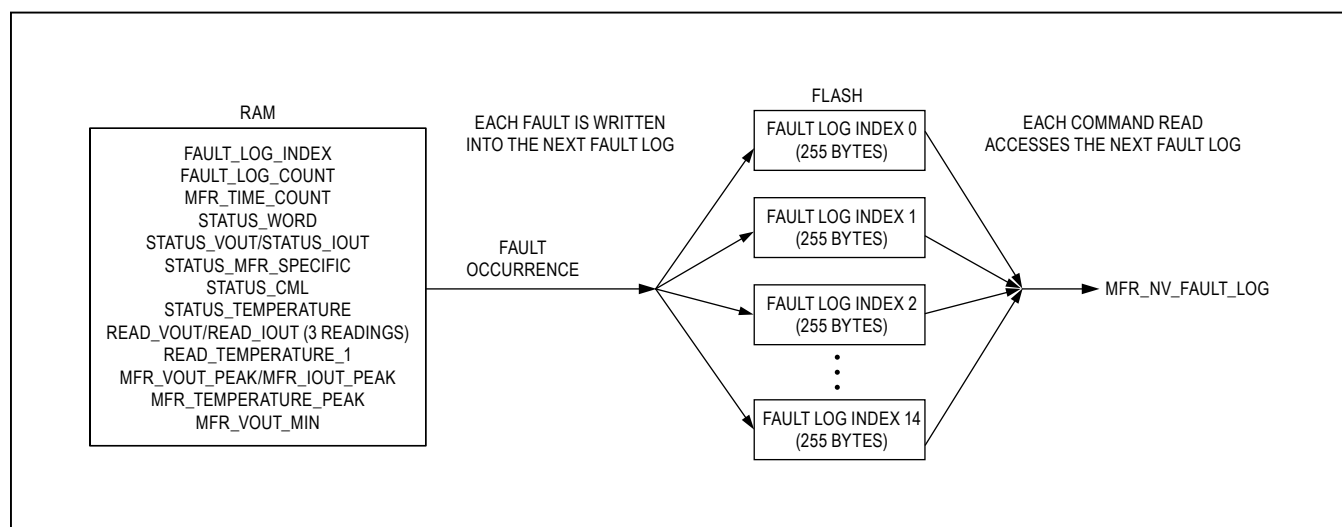


Figure 11. MFR\_NV\_FAULT\_LOG

There is a **FAULT\_LOG\_COUNT** (16-bit counter) at the beginning of each fault log that indicates which fault log is the latest. This counter rolls over should more than 65,535 faults be logged. This counter is not cleared when the **CLEAR\_NV\_FAULT\_LOG** bit in **MFR\_NV\_LOG\_CONFIG** is toggled. The 255 bytes returned by the **MFR\_NV\_FAULT\_LOG** command are described in [Table 34](#).

If an error occurs while the device is attempting to write to or clear the **MFR\_NV\_FAULT\_LOG**, the device sets the **CML** bit in **STATUS\_WORD** (no bits are set in **STATUS\_CML**) and **ALERT** is asserted (if enabled in **MFR\_MODE**).

**USER NOTE:**  $V_{DD}$  must be above 2.9V for the device to clear or log data into **MFR\_NV\_FAULT\_LOG**.

**Table 34. MFR\_NV\_FAULT\_LOG (DCh)**

| BYTE | PARAMETER                           | BYTE | PARAMETER                           |
|------|-------------------------------------|------|-------------------------------------|
| 0    | 00h/FAULT_LOG_INDEX                 | 128  | READ_VOUT/READ_IOUT T1 PAGE 11      |
| 2    | FAULT_LOG_COUNT                     | 130  | READ_VOUT/READ_IOUT T2 PAGE 11      |
| 4    | MFR_TIME_COUNT (LSW)                | 132  | READ_VOUT/READ_IOUT T0 PAGE 12      |
| 6    | MFR_TIME_COUNT (MSW)                | 134  | READ_VOUT/READ_IOUT T1 PAGE 12      |
| 8    | 0000h                               | 136  | READ_VOUT/READ_IOUT T2 PAGE 12      |
| 10   | STATUS_CML/00h                      | 138  | READ_VOUT/READ_IOUT T0 PAGE 13      |
| 12   | STATUS_WORD                         | 140  | READ_VOUT/READ_IOUT T1 PAGE 13      |
| 14   | STATUS_VOUT/STATUS_IOUT PAGES 0/1   | 142  | READ_VOUT/READ_IOUT T2 PAGE 13      |
| 16   | STATUS_VOUT/STATUS_IOUT PAGES 2/3   | 144  | READ_VOUT/READ_IOUT T0 PAGE 14      |
| 18   | STATUS_VOUT/STATUS_IOUT PAGES 4/5   | 146  | READ_VOUT/READ_IOUT T1 PAGE 14      |
| 20   | STATUS_VOUT/STATUS_IOUT PAGES 6/7   | 148  | READ_VOUT/READ_IOUT T2 PAGE 14      |
| 22   | STATUS_VOUT/STATUS_IOUT PAGES 8/9   | 150  | READ_VOUT/READ_IOUT T0 PAGE 15      |
| 24   | STATUS_VOUT/STATUS_IOUT PAGES 10/11 | 152  | READ_VOUT/READ_IOUT T1 PAGE 15      |
| 26   | STATUS_VOUT/STATUS_IOUT PAGES 12/13 | 154  | READ_VOUT/READ_IOUT T2 PAGE 15      |
| 28   | STATUS_VOUT/STATUS_IOUT PAGES 14/15 | 156  | 0000h                               |
| 30   | STATUS_MFR_SPECIFIC PAGES 0/1       | 158  | 0000h                               |
| 32   | STATUS_MFR_SPECIFIC PAGES 2/3       | 160  | 0000h                               |
| 34   | STATUS_MFR_SPECIFIC PAGES 4/5       | 162  | 0000h                               |
| 36   | STATUS_MFR_SPECIFIC PAGES 6/7       | 164  | MFR_VOUT_PEAK/MFR_IOUT_PEAK PAGE 0  |
| 38   | STATUS_MFR_SPECIFIC PAGES 8/9       | 166  | MFR_VOUT_PEAK/MFR_IOUT_PEAK PAGE 1  |
| 40   | STATUS_MFR_SPECIFIC PAGES 10/11     | 168  | MFR_VOUT_PEAK/MFR_IOUT_PEAK PAGE 2  |
| 42   | STATUS_MFR_SPECIFIC PAGES 12/13     | 170  | MFR_VOUT_PEAK/MFR_IOUT_PEAK PAGE 3  |
| 44   | STATUS_MFR_SPECIFIC PAGES 14/15     | 172  | MFR_VOUT_PEAK/MFR_IOUT_PEAK PAGE 4  |
| 46   | STATUS_MFR_SPECIFIC PAGE 255/00h    | 174  | MFR_VOUT_PEAK/MFR_IOUT_PEAK PAGE 5  |
| 48   | STATUS_TEMPERATURE PAGES 16/17      | 176  | MFR_VOUT_PEAK/MFR_IOUT_PEAK PAGE 6  |
| 50   | STATUS_TEMPERATURE PAGES 18/19      | 178  | MFR_VOUT_PEAK/MFR_IOUT_PEAK PAGE 7  |
| 52   | STATUS_TEMPERATURE PAGE 20/00h      | 180  | MFR_VOUT_PEAK/MFR_IOUT_PEAK PAGE 8  |
| 54   | CURRENT_CHANNELS (Note 4)           | 182  | MFR_VOUT_PEAK/MFR_IOUT_PEAK PAGE 9  |
| 56   | 0000h                               | 184  | MFR_VOUT_PEAK/MFR_IOUT_PEAK PAGE 10 |
| 58   | 0000h                               | 186  | MFR_VOUT_PEAK/MFR_IOUT_PEAK PAGE 11 |

Table 34. MFR\_NV\_FAULT\_LOG (DCh) (continued)

| BYTE | PARAMETER                                  | BYTE | PARAMETER                           |
|------|--------------------------------------------|------|-------------------------------------|
| 60   | READ_VOUT/READ_IOUT T0 PAGE 0 (Notes 2, 3) | 188  | MFR_VOUT_PEAK/MFR_IOUT_PEAK PAGE 12 |
| 62   | READ_VOUT/READ_IOUT T1 PAGE 0 (Notes 2, 3) | 190  | MFR_VOUT_PEAK/MFR_IOUT_PEAK PAGE 13 |
| 64   | READ_VOUT/READ_IOUT T2 PAGE 0 (Notes 2, 3) | 192  | MFR_VOUT_PEAK/MFR_IOUT_PEAK PAGE 14 |
| 66   | READ_VOUT/READ_IOUT T0 PAGE 1              | 194  | MFR_VOUT_PEAK/MFR_IOUT_PEAK PAGE 15 |
| 68   | READ_VOUT/READ_IOUT T1 PAGE 1              | 196  | MFR_VOUT_MIN PAGE 0                 |
| 70   | READ_VOUT/READ_IOUT T2 PAGE 1              | 198  | MFR_VOUT_MIN PAGE 1                 |
| 72   | READ_VOUT/READ_IOUT T0 PAGE 2              | 200  | MFR_VOUT_MIN PAGE 2                 |
| 74   | READ_VOUT/READ_IOUT T1 PAGE 2              | 202  | MFR_VOUT_MIN PAGE 3                 |
| 76   | READ_VOUT/READ_IOUT T2 PAGE 2              | 204  | MFR_VOUT_MIN PAGE 4                 |
| 78   | READ_VOUT/READ_IOUT T0 PAGE 3              | 206  | MFR_VOUT_MIN PAGE 5                 |
| 80   | READ_VOUT/READ_IOUT T1 PAGE 3              | 208  | MFR_VOUT_MIN PAGE 6                 |
| 82   | READ_VOUT/READ_IOUT T2 PAGE 3              | 210  | MFR_VOUT_MIN PAGE 7                 |
| 84   | READ_VOUT/READ_IOUT T0 PAGE 4              | 212  | MFR_VOUT_MIN PAGE 8                 |
| 86   | READ_VOUT/READ_IOUT T1 PAGE 4              | 214  | MFR_VOUT_MIN PAGE 9                 |
| 88   | READ_VOUT/READ_IOUT T2 PAGE 4              | 216  | MFR_VOUT_MIN PAGE 10                |
| 90   | READ_VOUT/READ_IOUT T0 PAGE 5              | 218  | MFR_VOUT_MIN PAGE 11                |
| 92   | READ_VOUT/READ_IOUT T1 PAGE 5              | 220  | MFR_VOUT_MIN PAGE 12                |
| 94   | READ_VOUT/READ_IOUT T2 PAGE 5              | 222  | MFR_VOUT_MIN PAGE 13                |
| 96   | READ_VOUT/READ_IOUT T0 PAGE 6              | 224  | MFR_VOUT_MIN PAGE 14                |
| 98   | READ_VOUT/READ_IOUT T1 PAGE 6              | 226  | MFR_VOUT_MIN PAGE 15                |
| 100  | READ_VOUT/READ_IOUT T2 PAGE 6              | 228  | 0000h                               |
| 102  | READ_VOUT/READ_IOUT T0 PAGE 7              | 230  | 0000h                               |
| 104  | READ_VOUT/READ_IOUT T1 PAGE 7              | 232  | READ_TEMPERATURE_1 PAGE 16          |
| 106  | READ_VOUT/READ_IOUT T2 PAGE 7              | 234  | READ_TEMPERATURE_1 PAGE 17          |
| 108  | READ_VOUT/READ_IOUT T0 PAGE 8              | 236  | READ_TEMPERATURE_1 PAGE 18          |
| 110  | READ_VOUT/READ_IOUT T1 PAGE 8              | 238  | READ_TEMPERATURE_1 PAGE 19          |
| 112  | READ_VOUT/READ_IOUT T2 PAGE 8              | 240  | READ_TEMPERATURE_1 PAGE 20          |
| 114  | READ_VOUT/READ_IOUT T0 PAGE 9              | 242  | MFR_TEMPERATURE_PEAK PAGE 16        |
| 116  | READ_VOUT/READ_IOUT T1 PAGE 9              | 244  | MFR_TEMPERATURE_PEAK PAGE 17        |
| 118  | READ_VOUT/READ_IOUT T2 PAGE 9              | 246  | MFR_TEMPERATURE_PEAK PAGE 18        |
| 120  | READ_VOUT/READ_IOUT T0 PAGE 10             | 248  | MFR_TEMPERATURE_PEAK PAGE 19        |
| 122  | READ_VOUT/READ_IOUT T1 PAGE 10             | 250  | MFR_TEMPERATURE_PEAK PAGE 20        |
| 124  | READ_VOUT/READ_IOUT T2 PAGE 10             | 252  | 0000h                               |
| 126  | READ_VOUT/READ_IOUT T0 PAGE 11             | 254  | LOG_VALID (Note 1)                  |

**Note 1:** LOG\_VALID is set to DDh if the fault log contains valid data.

**Note 2:** For READ\_VOUT, READ\_IOUT, T2 is the oldest reading and T0 is the newest reading.

**Note 3:** STATUS\_VOUT/STATUS\_IOUT and READ\_VOUT/STATUS\_IOUT depend on whether the channel is configured to monitor voltage or current.

**Note 4:** CURRENT\_CHANNELS is a bitmask (0 = voltage/1 = current) indicating which channels are enabled for current measurement.

**MFR\_TIME\_COUNT (DDh)**

The MFR\_TIME\_COUNT command returns the current value of a real-time counter that increments every 5ms, 20ms, 80ms, or 160ms depending on the configuration of the NV\_LOG\_DEPTH bits in MFR\_NV\_LOG\_CONFIG. This counter is useful in determining the time between multiple faults. The counter is a 32-bit value that rolls over. The count is reset to zero upon device power cycle or RST action, or a soft-reset. MFR\_TIME\_COUNT can be preset to any value and starts counting up from the preset value.

**MFR\_CHANNEL\_CONFIG (E4h)**

The MFR\_CHANNEL\_CONFIG command is used to configure the monitoring channels (PAGES 0–15). This command should not be changed while the power supplies are operating. The MFR\_CHANNEL\_CONFIG command is described in [Table 35](#) and shown in [Figure 12](#).

Each RSn/GPI pin can be independently configured using the SELECT[5:0] bits to one of the following:

- Monitor voltage; use the monitored voltage for sequencing (SELECT[5:0] = 10h)
- Monitor voltage; do not use for sequencing (SELECT[5:0] = 20h)
- Monitor current (SELECT[5:0] = 22h)
- Read voltage only; do not monitor for voltage faults or warnings (SELECT[5:0] = 21h)
- Read current only; do not monitor for current faults or warnings (SELECT[5:0] = 23h)
- General-purpose input (GPI); active low (SELECT[5:0] = 30h)
- General-purpose input (GPI); active high (SELECT[5:0] = 34h)
- Input is disabled (SELECT[5:0] = 00h)

If the monitoring channel is configured to monitor voltage for sequencing (SELECT[5:0] = 10h), then the associated PSENn output channel must also be configured for controlling power supplies by setting the SELECT bits in MFR\_PSEN\_CONFIG to 000. See the MFR\_PSEN\_CONFIG command description for more details.

When the RSn/GPI pins are configured as general-purpose inputs (GPIs) the READ\_VOUT command reports 0000h when the pin is inactive and 0001h when the pin is active.

Also, when the RSn/GPI pins are configured to monitor voltage (SELECT[5:0] = 10h or 20h) or act as GPI (SELECT[5:0] = 30h or 34h), each channel can be independently configured to generate a signature signal at the SEQ output. This would facilitate event-based sequencing (in multiple device systems), by indicating that this power supply has reached its POWER\_GOOD\_ON level and other channels can now proceed with their power-up.



**Table 35. MFR\_CHANNEL\_CONFIG (E4h)**

| BIT          | NAME                                                         | MEANING                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |              |                           |              |                                                              |              |                                    |              |                    |              |                   |              |                   |              |                                  |              |                                   |              |             |      |              |      |             |      |              |      |             |      |              |      |             |      |              |
|--------------|--------------------------------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------|---------------------------|--------------|--------------------------------------------------------------|--------------|------------------------------------|--------------|--------------------|--------------|-------------------|--------------|-------------------|--------------|----------------------------------|--------------|-----------------------------------|--------------|-------------|------|--------------|------|-------------|------|--------------|------|-------------|------|--------------|------|-------------|------|--------------|
| 15:12        | 0                                                            | These bits always return a 0.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |              |                           |              |                                                              |              |                                    |              |                    |              |                   |              |                   |              |                                  |              |                                   |              |             |      |              |      |             |      |              |      |             |      |              |      |             |      |              |
| 11:8         | SEQ_GENERATE                                                 | <p>These bits determine which <math>\overline{\text{SEQ}}</math> signature the channel should generate after crossing the POWER_GOOD_ON level:</p> <table><tr><td>0000</td><td>Disabled</td><td>1000</td><td>Signature 8</td></tr><tr><td>0001</td><td>Signature 1</td><td>1001</td><td>Signature 9</td></tr><tr><td>0010</td><td>Signature 2</td><td>1010</td><td>Signature 10</td></tr><tr><td>0011</td><td>Signature 3</td><td>1011</td><td>Signature 11</td></tr><tr><td>0100</td><td>Signature 4</td><td>1100</td><td>Signature 12</td></tr><tr><td>0101</td><td>Signature 5</td><td>1101</td><td>Signature 13</td></tr><tr><td>0110</td><td>Signature 6</td><td>1110</td><td>Signature 14</td></tr><tr><td>0111</td><td>Signature 7</td><td>1111</td><td>Signature 15</td></tr></table> | 0000         | Disabled                  | 1000         | Signature 8                                                  | 0001         | Signature 1                        | 1001         | Signature 9        | 0010         | Signature 2       | 1010         | Signature 10      | 0011         | Signature 3                      | 1011         | Signature 11                      | 0100         | Signature 4 | 1100 | Signature 12 | 0101 | Signature 5 | 1101 | Signature 13 | 0110 | Signature 6 | 1110 | Signature 14 | 0111 | Signature 7 | 1111 | Signature 15 |
| 0000         | Disabled                                                     | 1000                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          | Signature 8  |                           |              |                                                              |              |                                    |              |                    |              |                   |              |                   |              |                                  |              |                                   |              |             |      |              |      |             |      |              |      |             |      |              |      |             |      |              |
| 0001         | Signature 1                                                  | 1001                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          | Signature 9  |                           |              |                                                              |              |                                    |              |                    |              |                   |              |                   |              |                                  |              |                                   |              |             |      |              |      |             |      |              |      |             |      |              |      |             |      |              |
| 0010         | Signature 2                                                  | 1010                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          | Signature 10 |                           |              |                                                              |              |                                    |              |                    |              |                   |              |                   |              |                                  |              |                                   |              |             |      |              |      |             |      |              |      |             |      |              |      |             |      |              |
| 0011         | Signature 3                                                  | 1011                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          | Signature 11 |                           |              |                                                              |              |                                    |              |                    |              |                   |              |                   |              |                                  |              |                                   |              |             |      |              |      |             |      |              |      |             |      |              |      |             |      |              |
| 0100         | Signature 4                                                  | 1100                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          | Signature 12 |                           |              |                                                              |              |                                    |              |                    |              |                   |              |                   |              |                                  |              |                                   |              |             |      |              |      |             |      |              |      |             |      |              |      |             |      |              |
| 0101         | Signature 5                                                  | 1101                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          | Signature 13 |                           |              |                                                              |              |                                    |              |                    |              |                   |              |                   |              |                                  |              |                                   |              |             |      |              |      |             |      |              |      |             |      |              |      |             |      |              |
| 0110         | Signature 6                                                  | 1110                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          | Signature 14 |                           |              |                                                              |              |                                    |              |                    |              |                   |              |                   |              |                                  |              |                                   |              |             |      |              |      |             |      |              |      |             |      |              |      |             |      |              |
| 0111         | Signature 7                                                  | 1111                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          | Signature 15 |                           |              |                                                              |              |                                    |              |                    |              |                   |              |                   |              |                                  |              |                                   |              |             |      |              |      |             |      |              |      |             |      |              |      |             |      |              |
| 7:6          | 0                                                            | These bits always return a 0.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |              |                           |              |                                                              |              |                                    |              |                    |              |                   |              |                   |              |                                  |              |                                   |              |             |      |              |      |             |      |              |      |             |      |              |      |             |      |              |
| 5:0          | SELECT[5:0]                                                  | <p>These bits select the function of the RSn/GPI n pins:</p> <table><tr><th>SELECT[5:0]</th><th>SELECTED CHANNEL FUNCTION</th></tr><tr><td>010000 (10h)</td><td>Sequencing + voltage monitoring (only valid for PAGES 0–11)*</td></tr><tr><td>100000 (20h)</td><td>Voltage monitoring (no sequencing)</td></tr><tr><td>100010 (22h)</td><td>Current monitoring</td></tr><tr><td>100001 (21h)</td><td>Voltage read only</td></tr><tr><td>100011 (23h)</td><td>Current read only</td></tr><tr><td>110000 (30h)</td><td>General-purpose input active low</td></tr><tr><td>110100 (34h)</td><td>General-purpose input active high</td></tr><tr><td>000000 (00h)</td><td>Disabled</td></tr></table>                                                                                                | SELECT[5:0]  | SELECTED CHANNEL FUNCTION | 010000 (10h) | Sequencing + voltage monitoring (only valid for PAGES 0–11)* | 100000 (20h) | Voltage monitoring (no sequencing) | 100010 (22h) | Current monitoring | 100001 (21h) | Voltage read only | 100011 (23h) | Current read only | 110000 (30h) | General-purpose input active low | 110100 (34h) | General-purpose input active high | 000000 (00h) | Disabled    |      |              |      |             |      |              |      |             |      |              |      |             |      |              |
| SELECT[5:0]  | SELECTED CHANNEL FUNCTION                                    |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |              |                           |              |                                                              |              |                                    |              |                    |              |                   |              |                   |              |                                  |              |                                   |              |             |      |              |      |             |      |              |      |             |      |              |      |             |      |              |
| 010000 (10h) | Sequencing + voltage monitoring (only valid for PAGES 0–11)* |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |              |                           |              |                                                              |              |                                    |              |                    |              |                   |              |                   |              |                                  |              |                                   |              |             |      |              |      |             |      |              |      |             |      |              |      |             |      |              |
| 100000 (20h) | Voltage monitoring (no sequencing)                           |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |              |                           |              |                                                              |              |                                    |              |                    |              |                   |              |                   |              |                                  |              |                                   |              |             |      |              |      |             |      |              |      |             |      |              |      |             |      |              |
| 100010 (22h) | Current monitoring                                           |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |              |                           |              |                                                              |              |                                    |              |                    |              |                   |              |                   |              |                                  |              |                                   |              |             |      |              |      |             |      |              |      |             |      |              |      |             |      |              |
| 100001 (21h) | Voltage read only                                            |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |              |                           |              |                                                              |              |                                    |              |                    |              |                   |              |                   |              |                                  |              |                                   |              |             |      |              |      |             |      |              |      |             |      |              |      |             |      |              |
| 100011 (23h) | Current read only                                            |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |              |                           |              |                                                              |              |                                    |              |                    |              |                   |              |                   |              |                                  |              |                                   |              |             |      |              |      |             |      |              |      |             |      |              |      |             |      |              |
| 110000 (30h) | General-purpose input active low                             |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |              |                           |              |                                                              |              |                                    |              |                    |              |                   |              |                   |              |                                  |              |                                   |              |             |      |              |      |             |      |              |      |             |      |              |      |             |      |              |
| 110100 (34h) | General-purpose input active high                            |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |              |                           |              |                                                              |              |                                    |              |                    |              |                   |              |                   |              |                                  |              |                                   |              |             |      |              |      |             |      |              |      |             |      |              |      |             |      |              |
| 000000 (00h) | Disabled                                                     |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |              |                           |              |                                                              |              |                                    |              |                    |              |                   |              |                   |              |                                  |              |                                   |              |             |      |              |      |             |      |              |      |             |      |              |      |             |      |              |

\*For proper sequencing, the SELECT bits in MFR\_PSEN\_CONFIG must be set to 000.

**Table 36. Fault-Monitoring States**

| FAULT           | REQUIRED DEVICE CONFIGURATION<br>FOR ACTIVE MONITORING                                                                        | WHEN MONITORED                                                                                                  |
|-----------------|-------------------------------------------------------------------------------------------------------------------------------|-----------------------------------------------------------------------------------------------------------------|
| Overvoltage     | <ul style="list-style-type: none"> <li>Voltage monitoring enabled (SELECT[5:0] = 10h or 20h in MFR_CHANNEL_CONFIG)</li> </ul> | Continuous monitoring.                                                                                          |
| Undervoltage    | <ul style="list-style-type: none"> <li>Voltage monitoring enabled (SELECT[5:0] = 10h or 20h in MFR_CHANNEL_CONFIG)</li> </ul> | Stops monitoring while the power supply is off; starts monitoring when voltage exceeds the POWER_GOOD_ON level. |
| Overcurrent     | <ul style="list-style-type: none"> <li>Current monitoring enabled (SELECT[5:0] = 22h in MFR_CHANNEL_CONFIG)</li> </ul>        | Continuous monitoring.                                                                                          |
| Power-Up Time   | <ul style="list-style-type: none"> <li>Sequencing enabled (SELECT[5:0] = 10h in MFR_CHANNEL_CONFIG)</li> </ul>                | Monitored only during power-on sequence.                                                                        |
| Overtemperature | <ul style="list-style-type: none"> <li>Temperature sensor enabled (ENABLE = 1 in MFR_TEMP_SENSOR_CONFIG)</li> </ul>           | Continuous monitoring.                                                                                          |

**Note:** Device response to faults is determined by the configuration of MFR\_FAULT\_RESPONSE.

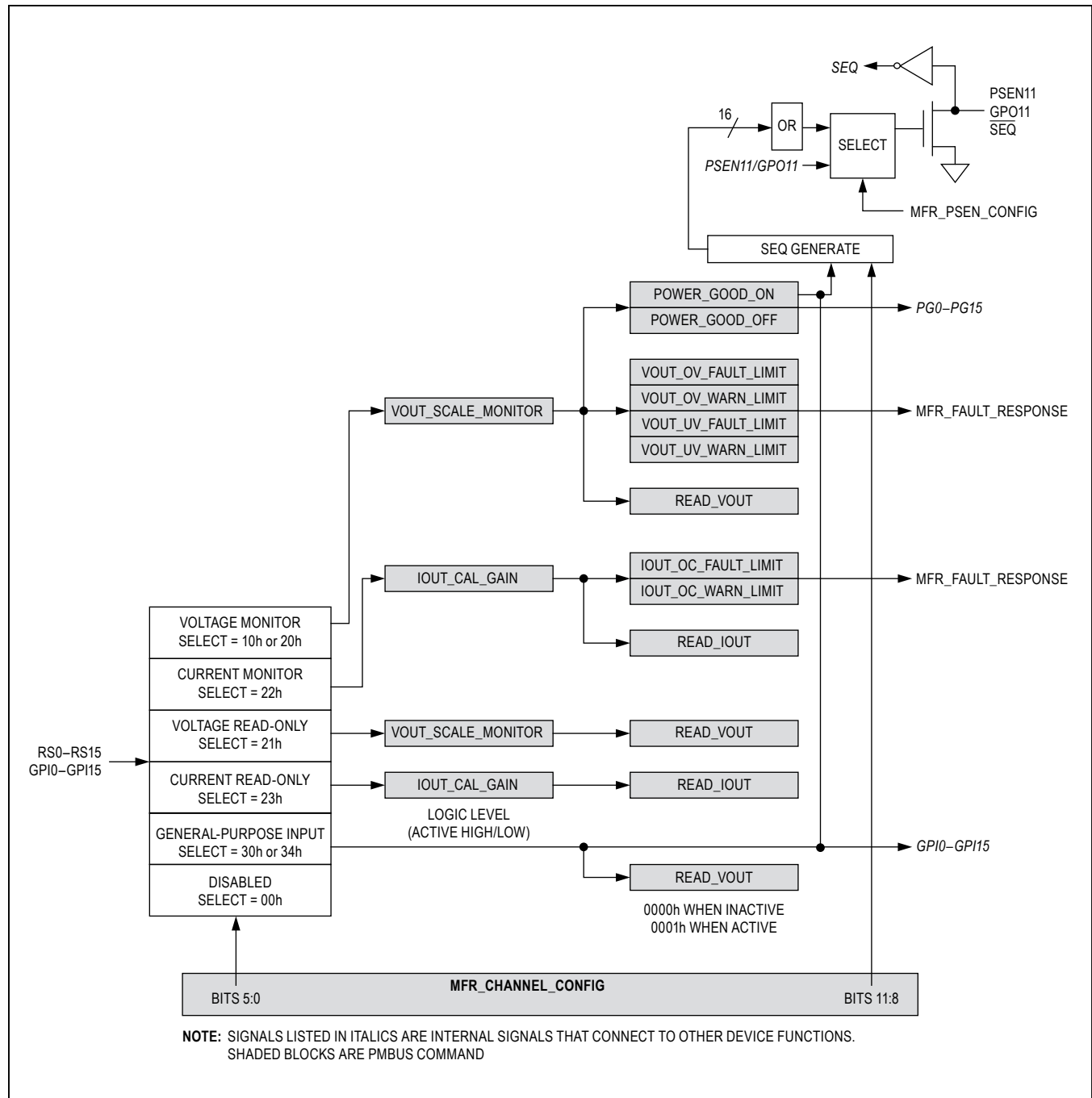


Figure 12. MFR\_CHANNEL\_CONFIG Command

**MFR\_TON\_SEQ\_MAX (E6h)**

The MFR\_TON\_SEQ\_MAX command sets an upper limit, in milliseconds, from a sequencing group (either SEQUENCE0 or SEQUENCE1, as chosen by the SEQ\_SELECT bit in the MFR\_SEQ\_CONFIG command), initiating the power-up sequence until the channel expects to begin its power-up based on an event, which could be either a logic combination of power-good (PG) and GPI signals or a match on the SEQ pin, as configured with the SELECT bits in MFR\_SEQ\_CONFIG. The 2 data bytes are in DIRECT format. If this value is zero, then the limit is disabled. In response to the MFR\_TON\_SEQ\_MAX being exceeded, the device does the following:

- 1) Sets the VOUT bit in STATUS\_WORD.
- 2) Sets the TON\_MAX\_FAULT bit in STATUS\_VOUT.
- 3) Responds as specified in the MFR\_FAULT\_RESPONSE.
- 4) Notifies the host using  $\overline{\text{ALERT}}$  assertion (if enabled in MFR\_MODE).

**MFR\_PWM\_CONFIG (E7h)**

The MFR\_PWM\_CONFIG command is used to configure the individual PWMx/GPOy (x = 0–7/y = 12–19) outputs. This command should not be changed while the power supplies are being PWM margined. The MFR\_PWM\_CONFIG command is described in [Table 37](#) and shown in [Figure 13](#).

Each PWMn/GPOn pin can be independently configured using the SELECT[2:0] bits to perform one of the following:

- PWM margining operation (SELECT[2:0] = 000)

- Force pin assertion (SELECT[2:0] = 001)
- Force pin deassertion (SELECT[2:0] = 010)
- Assert when all enabled channel power-good (PG) or GPI are asserted (SELECT[2:0] = 011)
- Assert when any enabled alarm goes active (SELECT[2:0] = 100)

Also, each PWMn/GPOn pin can be independently configured to be active high or active low and either push-pull or open drain using the HI\_LO and PP\_OD bits, respectively.

If SELECT[2:0] = 011, the PWMn/GPOn output is configured to assert when some combination of power-goods (PGs) and GPIs from each channel are asserted. The channels that should be used in this combination are selected using the PG\_GPI\_SELECT bits 31:16. If the PG\_GPI\_SELECT bit is cleared, then the associated channel is not used in the logical combination to assert the GPO output. If the PG\_GPI\_SELECT bit is set, then the PG or GPI from that channel is used in the logical combination to assert the GPOn output. This function is useful in creating system power-good signals.

If SELECT[2:0] = 100, the PWMn/GPOn output is configured to assert when any of the enabled channel alarms go active. The channel alarms are enabled with the ALARM\_SELECT bits 31:16. If the ALARM\_SELECT bit is cleared, then the alarm from that channel is blocked. If the ALARM\_SELECT bit is set, then the alarm from that channel is routed to an OR function, such that any enabled alarm asserts the GPOn output. The alarm function is chosen with the ALARM\_CONFIG bits in the MFR\_FAULT\_RESPONSE command. This function is useful for system debug or for enabling system status LEDs.

Table 37. MFR\_PWM\_CONFIG (E7h)

| BIT            | NAME                                                                                                                                                                            | MEANING                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |                |                                 |                |                                                                                                                                                                            |      |                                                                                                                                                                                 |      |                       |      |                                   |      |                                  |      |                                       |      |          |      |      |      |       |      |      |      |        |      |      |      |        |      |      |      |        |      |       |      |        |
|----------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------|---------------------------------|----------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------|-----------------------|------|-----------------------------------|------|----------------------------------|------|---------------------------------------|------|----------|------|------|------|-------|------|------|------|--------|------|------|------|--------|------|------|------|--------|------|-------|------|--------|
| 31:16          | PG_GPI_SELECT<br>ALARM_SELECT                                                                                                                                                   | <p>These bits are only used if SELECT[2:0] = 011 or 100; each bit corresponds to one channel (device channel N + 16 = bit number):</p> <table><thead><tr><th>SELECT[2:0]</th><th>BIT FUNCTION</th></tr></thead><tbody><tr><td>011</td><td>When this bit is cleared, the power good (PG) or GPI from channel N is not used in the logical AND to assert the GPOn output. When this bit is set, the PG or GPI is used.</td></tr><tr><td>100</td><td>When this bit is cleared, the alarm from channel N is blocked from the logical OR to assert the GPO output. When this bit is set, the alarm signal is routed to the logical OR.</td></tr></tbody></table>                                                                                                                                                    | SELECT[2:0]    | BIT FUNCTION                    | 011            | When this bit is cleared, the power good (PG) or GPI from channel N is not used in the logical AND to assert the GPOn output. When this bit is set, the PG or GPI is used. | 100  | When this bit is cleared, the alarm from channel N is blocked from the logical OR to assert the GPO output. When this bit is set, the alarm signal is routed to the logical OR. |      |                       |      |                                   |      |                                  |      |                                       |      |          |      |      |      |       |      |      |      |        |      |      |      |        |      |      |      |        |      |       |      |        |
| SELECT[2:0]    | BIT FUNCTION                                                                                                                                                                    |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |                |                                 |                |                                                                                                                                                                            |      |                                                                                                                                                                                 |      |                       |      |                                   |      |                                  |      |                                       |      |          |      |      |      |       |      |      |      |        |      |      |      |        |      |      |      |        |      |       |      |        |
| 011            | When this bit is cleared, the power good (PG) or GPI from channel N is not used in the logical AND to assert the GPOn output. When this bit is set, the PG or GPI is used.      |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |                |                                 |                |                                                                                                                                                                            |      |                                                                                                                                                                                 |      |                       |      |                                   |      |                                  |      |                                       |      |          |      |      |      |       |      |      |      |        |      |      |      |        |      |      |      |        |      |       |      |        |
| 100            | When this bit is cleared, the alarm from channel N is blocked from the logical OR to assert the GPO output. When this bit is set, the alarm signal is routed to the logical OR. |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |                |                                 |                |                                                                                                                                                                            |      |                                                                                                                                                                                 |      |                       |      |                                   |      |                                  |      |                                       |      |          |      |      |      |       |      |      |      |        |      |      |      |        |      |      |      |        |      |       |      |        |
| 15:12          | OFF_DELAY                                                                                                                                                                       | <p>These bits determine the delay time to pin deassertion; when the pin is operating as a PGn/GPIIn or alarm pin (SELECT[2:0] = 011 or 100):</p> <table><thead><tr><th>OFF_DELAY[3:0]</th><th>DELAY TIME</th><th>OFF_DELAY[3:0]</th><th>DELAY TIME</th></tr></thead><tbody><tr><td>0000</td><td>0ms</td><td>1000</td><td>200ms</td></tr><tr><td>0001</td><td>5ms</td><td>1001</td><td>400ms</td></tr><tr><td>0010</td><td>10ms</td><td>1010</td><td>600ms</td></tr><tr><td>0011</td><td>20ms</td><td>1011</td><td>800ms</td></tr><tr><td>0100</td><td>40ms</td><td>1100</td><td>1000ms</td></tr><tr><td>0101</td><td>60ms</td><td>1101</td><td>1500ms</td></tr><tr><td>0110</td><td>80ms</td><td>1110</td><td>2000ms</td></tr><tr><td>0111</td><td>100ms</td><td>1111</td><td>4000ms</td></tr></tbody></table> | OFF_DELAY[3:0] | DELAY TIME                      | OFF_DELAY[3:0] | DELAY TIME                                                                                                                                                                 | 0000 | 0ms                                                                                                                                                                             | 1000 | 200ms                 | 0001 | 5ms                               | 1001 | 400ms                            | 0010 | 10ms                                  | 1010 | 600ms    | 0011 | 20ms | 1011 | 800ms | 0100 | 40ms | 1100 | 1000ms | 0101 | 60ms | 1101 | 1500ms | 0110 | 80ms | 1110 | 2000ms | 0111 | 100ms | 1111 | 4000ms |
| OFF_DELAY[3:0] | DELAY TIME                                                                                                                                                                      | OFF_DELAY[3:0]                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 | DELAY TIME     |                                 |                |                                                                                                                                                                            |      |                                                                                                                                                                                 |      |                       |      |                                   |      |                                  |      |                                       |      |          |      |      |      |       |      |      |      |        |      |      |      |        |      |      |      |        |      |       |      |        |
| 0000           | 0ms                                                                                                                                                                             | 1000                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           | 200ms          |                                 |                |                                                                                                                                                                            |      |                                                                                                                                                                                 |      |                       |      |                                   |      |                                  |      |                                       |      |          |      |      |      |       |      |      |      |        |      |      |      |        |      |      |      |        |      |       |      |        |
| 0001           | 5ms                                                                                                                                                                             | 1001                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           | 400ms          |                                 |                |                                                                                                                                                                            |      |                                                                                                                                                                                 |      |                       |      |                                   |      |                                  |      |                                       |      |          |      |      |      |       |      |      |      |        |      |      |      |        |      |      |      |        |      |       |      |        |
| 0010           | 10ms                                                                                                                                                                            | 1010                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           | 600ms          |                                 |                |                                                                                                                                                                            |      |                                                                                                                                                                                 |      |                       |      |                                   |      |                                  |      |                                       |      |          |      |      |      |       |      |      |      |        |      |      |      |        |      |      |      |        |      |       |      |        |
| 0011           | 20ms                                                                                                                                                                            | 1011                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           | 800ms          |                                 |                |                                                                                                                                                                            |      |                                                                                                                                                                                 |      |                       |      |                                   |      |                                  |      |                                       |      |          |      |      |      |       |      |      |      |        |      |      |      |        |      |      |      |        |      |       |      |        |
| 0100           | 40ms                                                                                                                                                                            | 1100                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           | 1000ms         |                                 |                |                                                                                                                                                                            |      |                                                                                                                                                                                 |      |                       |      |                                   |      |                                  |      |                                       |      |          |      |      |      |       |      |      |      |        |      |      |      |        |      |      |      |        |      |       |      |        |
| 0101           | 60ms                                                                                                                                                                            | 1101                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           | 1500ms         |                                 |                |                                                                                                                                                                            |      |                                                                                                                                                                                 |      |                       |      |                                   |      |                                  |      |                                       |      |          |      |      |      |       |      |      |      |        |      |      |      |        |      |      |      |        |      |       |      |        |
| 0110           | 80ms                                                                                                                                                                            | 1110                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           | 2000ms         |                                 |                |                                                                                                                                                                            |      |                                                                                                                                                                                 |      |                       |      |                                   |      |                                  |      |                                       |      |          |      |      |      |       |      |      |      |        |      |      |      |        |      |      |      |        |      |       |      |        |
| 0111           | 100ms                                                                                                                                                                           | 1111                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           | 4000ms         |                                 |                |                                                                                                                                                                            |      |                                                                                                                                                                                 |      |                       |      |                                   |      |                                  |      |                                       |      |          |      |      |      |       |      |      |      |        |      |      |      |        |      |      |      |        |      |       |      |        |
| 11:8           | ON_DELAY                                                                                                                                                                        | <p>These bits determine the delay time to pin assertion; when the pin is operating as a PGn/GPIIn or alarm pin (SELECT[2:0] = 011 or 100):</p> <table><thead><tr><th>ON_DELAY[3:0]</th><th>DELAY TIME</th><th>ON_DELAY[3:0]</th><th>DELAY TIME</th></tr></thead><tbody><tr><td>0000</td><td>0ms</td><td>1000</td><td>200ms</td></tr><tr><td>0001</td><td>5ms</td><td>1001</td><td>400ms</td></tr><tr><td>0010</td><td>10ms</td><td>1010</td><td>600ms</td></tr><tr><td>0011</td><td>20ms</td><td>1011</td><td>800ms</td></tr><tr><td>0100</td><td>40ms</td><td>1100</td><td>1000ms</td></tr><tr><td>0101</td><td>60ms</td><td>1101</td><td>1500ms</td></tr><tr><td>0110</td><td>80ms</td><td>1110</td><td>2000ms</td></tr><tr><td>0111</td><td>100ms</td><td>1111</td><td>4000ms</td></tr></tbody></table>     | ON_DELAY[3:0]  | DELAY TIME                      | ON_DELAY[3:0]  | DELAY TIME                                                                                                                                                                 | 0000 | 0ms                                                                                                                                                                             | 1000 | 200ms                 | 0001 | 5ms                               | 1001 | 400ms                            | 0010 | 10ms                                  | 1010 | 600ms    | 0011 | 20ms | 1011 | 800ms | 0100 | 40ms | 1100 | 1000ms | 0101 | 60ms | 1101 | 1500ms | 0110 | 80ms | 1110 | 2000ms | 0111 | 100ms | 1111 | 4000ms |
| ON_DELAY[3:0]  | DELAY TIME                                                                                                                                                                      | ON_DELAY[3:0]                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  | DELAY TIME     |                                 |                |                                                                                                                                                                            |      |                                                                                                                                                                                 |      |                       |      |                                   |      |                                  |      |                                       |      |          |      |      |      |       |      |      |      |        |      |      |      |        |      |      |      |        |      |       |      |        |
| 0000           | 0ms                                                                                                                                                                             | 1000                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           | 200ms          |                                 |                |                                                                                                                                                                            |      |                                                                                                                                                                                 |      |                       |      |                                   |      |                                  |      |                                       |      |          |      |      |      |       |      |      |      |        |      |      |      |        |      |      |      |        |      |       |      |        |
| 0001           | 5ms                                                                                                                                                                             | 1001                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           | 400ms          |                                 |                |                                                                                                                                                                            |      |                                                                                                                                                                                 |      |                       |      |                                   |      |                                  |      |                                       |      |          |      |      |      |       |      |      |      |        |      |      |      |        |      |      |      |        |      |       |      |        |
| 0010           | 10ms                                                                                                                                                                            | 1010                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           | 600ms          |                                 |                |                                                                                                                                                                            |      |                                                                                                                                                                                 |      |                       |      |                                   |      |                                  |      |                                       |      |          |      |      |      |       |      |      |      |        |      |      |      |        |      |      |      |        |      |       |      |        |
| 0011           | 20ms                                                                                                                                                                            | 1011                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           | 800ms          |                                 |                |                                                                                                                                                                            |      |                                                                                                                                                                                 |      |                       |      |                                   |      |                                  |      |                                       |      |          |      |      |      |       |      |      |      |        |      |      |      |        |      |      |      |        |      |       |      |        |
| 0100           | 40ms                                                                                                                                                                            | 1100                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           | 1000ms         |                                 |                |                                                                                                                                                                            |      |                                                                                                                                                                                 |      |                       |      |                                   |      |                                  |      |                                       |      |          |      |      |      |       |      |      |      |        |      |      |      |        |      |      |      |        |      |       |      |        |
| 0101           | 60ms                                                                                                                                                                            | 1101                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           | 1500ms         |                                 |                |                                                                                                                                                                            |      |                                                                                                                                                                                 |      |                       |      |                                   |      |                                  |      |                                       |      |          |      |      |      |       |      |      |      |        |      |      |      |        |      |      |      |        |      |       |      |        |
| 0110           | 80ms                                                                                                                                                                            | 1110                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           | 2000ms         |                                 |                |                                                                                                                                                                            |      |                                                                                                                                                                                 |      |                       |      |                                   |      |                                  |      |                                       |      |          |      |      |      |       |      |      |      |        |      |      |      |        |      |      |      |        |      |       |      |        |
| 0111           | 100ms                                                                                                                                                                           | 1111                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           | 4000ms         |                                 |                |                                                                                                                                                                            |      |                                                                                                                                                                                 |      |                       |      |                                   |      |                                  |      |                                       |      |          |      |      |      |       |      |      |      |        |      |      |      |        |      |      |      |        |      |       |      |        |
| 7              | PP_OD                                                                                                                                                                           | 0 = PWMn/GPOn push-pull output<br>1 = PWMn/GPOn open-drain output                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |                |                                 |                |                                                                                                                                                                            |      |                                                                                                                                                                                 |      |                       |      |                                   |      |                                  |      |                                       |      |          |      |      |      |       |      |      |      |        |      |      |      |        |      |      |      |        |      |       |      |        |
| 6              | HI_LO                                                                                                                                                                           | 0 = PWMn/GPOn active low<br>1 = PWMn/GPOn active high                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |                |                                 |                |                                                                                                                                                                            |      |                                                                                                                                                                                 |      |                       |      |                                   |      |                                  |      |                                       |      |          |      |      |      |       |      |      |      |        |      |      |      |        |      |      |      |        |      |       |      |        |
| 5:3            | 0                                                                                                                                                                               | These bits always return a 0.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |                |                                 |                |                                                                                                                                                                            |      |                                                                                                                                                                                 |      |                       |      |                                   |      |                                  |      |                                       |      |          |      |      |      |       |      |      |      |        |      |      |      |        |      |      |      |        |      |       |      |        |
| 2:0            | SELECT[2:0]                                                                                                                                                                     | <p>These bits determine the function selected on the pin:</p> <table><thead><tr><th>SELECT[2:0]</th><th>PWMn/GPOn PIN SELECTED FUNCTION</th></tr></thead><tbody><tr><td>000</td><td>PWM operation</td></tr><tr><td>001</td><td>Force GPO assertion</td></tr><tr><td>010</td><td>Force GPO deassertion</td></tr><tr><td>011</td><td>PG/GPI operation (use bits 31:16)</td></tr><tr><td>100</td><td>Alarm operation (use bits 31:16)</td></tr><tr><td>101</td><td>FAULT1 special function (only PAGE 7)</td></tr><tr><td>11x</td><td>Reserved</td></tr></tbody></table>                                                                                                                                                                                                                                          | SELECT[2:0]    | PWMn/GPOn PIN SELECTED FUNCTION | 000            | PWM operation                                                                                                                                                              | 001  | Force GPO assertion                                                                                                                                                             | 010  | Force GPO deassertion | 011  | PG/GPI operation (use bits 31:16) | 100  | Alarm operation (use bits 31:16) | 101  | FAULT1 special function (only PAGE 7) | 11x  | Reserved |      |      |      |       |      |      |      |        |      |      |      |        |      |      |      |        |      |       |      |        |
| SELECT[2:0]    | PWMn/GPOn PIN SELECTED FUNCTION                                                                                                                                                 |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |                |                                 |                |                                                                                                                                                                            |      |                                                                                                                                                                                 |      |                       |      |                                   |      |                                  |      |                                       |      |          |      |      |      |       |      |      |      |        |      |      |      |        |      |      |      |        |      |       |      |        |
| 000            | PWM operation                                                                                                                                                                   |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |                |                                 |                |                                                                                                                                                                            |      |                                                                                                                                                                                 |      |                       |      |                                   |      |                                  |      |                                       |      |          |      |      |      |       |      |      |      |        |      |      |      |        |      |      |      |        |      |       |      |        |
| 001            | Force GPO assertion                                                                                                                                                             |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |                |                                 |                |                                                                                                                                                                            |      |                                                                                                                                                                                 |      |                       |      |                                   |      |                                  |      |                                       |      |          |      |      |      |       |      |      |      |        |      |      |      |        |      |      |      |        |      |       |      |        |
| 010            | Force GPO deassertion                                                                                                                                                           |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |                |                                 |                |                                                                                                                                                                            |      |                                                                                                                                                                                 |      |                       |      |                                   |      |                                  |      |                                       |      |          |      |      |      |       |      |      |      |        |      |      |      |        |      |      |      |        |      |       |      |        |
| 011            | PG/GPI operation (use bits 31:16)                                                                                                                                               |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |                |                                 |                |                                                                                                                                                                            |      |                                                                                                                                                                                 |      |                       |      |                                   |      |                                  |      |                                       |      |          |      |      |      |       |      |      |      |        |      |      |      |        |      |      |      |        |      |       |      |        |
| 100            | Alarm operation (use bits 31:16)                                                                                                                                                |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |                |                                 |                |                                                                                                                                                                            |      |                                                                                                                                                                                 |      |                       |      |                                   |      |                                  |      |                                       |      |          |      |      |      |       |      |      |      |        |      |      |      |        |      |      |      |        |      |       |      |        |
| 101            | FAULT1 special function (only PAGE 7)                                                                                                                                           |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |                |                                 |                |                                                                                                                                                                            |      |                                                                                                                                                                                 |      |                       |      |                                   |      |                                  |      |                                       |      |          |      |      |      |       |      |      |      |        |      |      |      |        |      |      |      |        |      |       |      |        |
| 11x            | Reserved                                                                                                                                                                        |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |                |                                 |                |                                                                                                                                                                            |      |                                                                                                                                                                                 |      |                       |      |                                   |      |                                  |      |                                       |      |          |      |      |      |       |      |      |      |        |      |      |      |        |      |      |      |        |      |       |      |        |

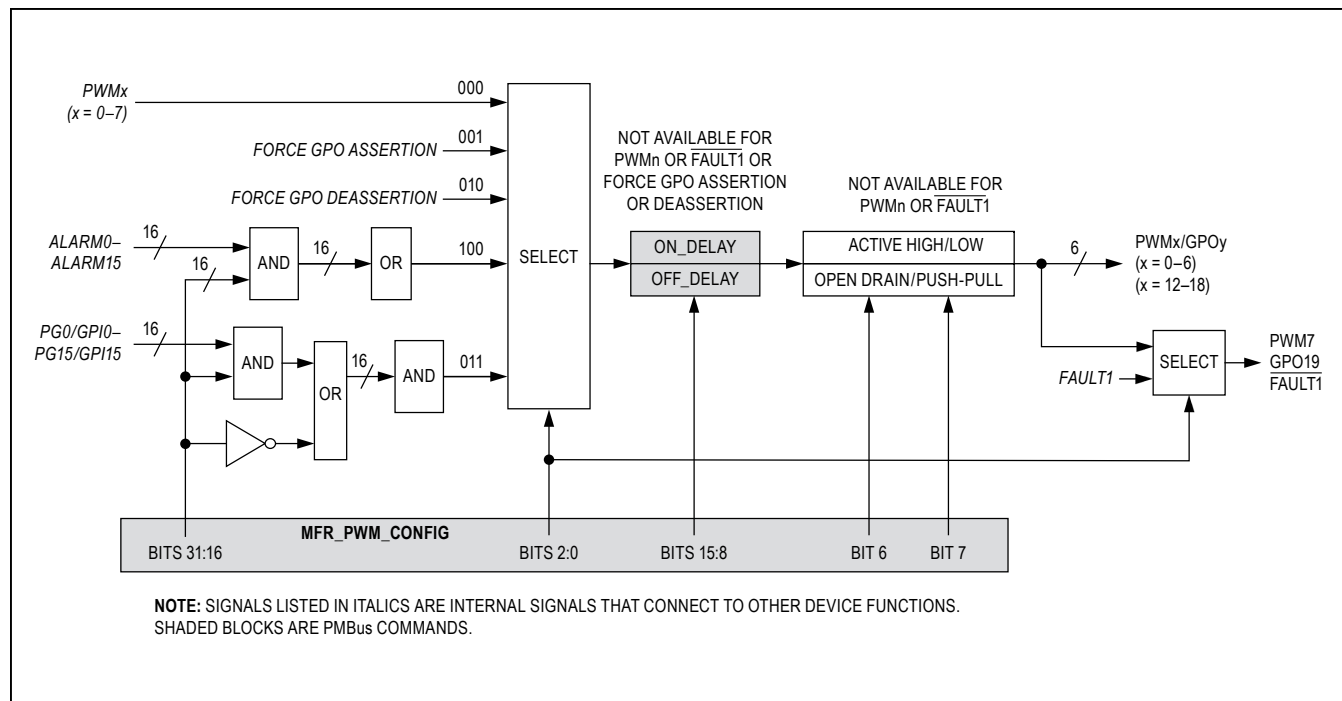


Figure 13. MFR\_PWM\_CONFIG Functional Logic

## Delay Function

If a delay is configured either on or off, the input must be continuously static through the delay time before the output changes state (see [Figure 9](#)).

## MFR\_SEQ\_CONFIG (E8h)

The MFR\_SEQ\_CONFIG command is used to configure the sequencing channels (PAGES 0–11). This command should not be changed while the power supplies are operating. The MFR\_SEQ\_CONFIG command is described in [Table 38](#) and shown in [Figure 2](#).

Each channel can be independently configured to initiate power-on sequencing, using the SELECT[1:0] bits, to one of the following conditions:

- Wait for either SEQUENCE0 or SEQUENCE1 from ON\_OFF\_CONFIG decode (SELECT[1:0] = 00)
- Wait for all enabled channel power-good (PG) or GPI to be asserted (SELECT[1:0] = 01)
- Wait for a match on the  $\overline{\text{SEQ}}$  pin (SELECT[2:0] = 10)

If SELECT[1:0] = 00, then the channel waits for either the SEQUENCE0 or SEQUENCE1 signal to assert before powering on. The sequence signal to use is selected with the SEQ\_SELECT bit. The SEQUENCE0 and SEQUENCE1 signals are generated by decoding

the OPERATION command and CONTROLn pins using the ON\_OFF\_CONFIG command. See the ON\_OFF\_CONFIG command description for details. This selection would be used if the channel is being controlled by time-based sequencing.

If SELECT[1:0] = 01, then sequencing for the channel is initiated when some combination of power-goods (PGs) and general-purpose inputs (GPIs) are asserted. The channels that should be used in this combination are selected using the PG\_GPI\_SELECT bits 31:16. If the PG\_GPI\_SELECT bit is cleared, then the associated channel is not used in the logical combination to assert the GPOn output. If the PG\_GPI\_SELECT bit is set, then the power good or GPI from the channel is used in the logical combination to initiate the power-on sequencing. This selection would be used if the channel is being controlled by event-based sequencing.

If SELECT[1:0] = 10, then sequencing is initiated when the channel matches the selected signature on the  $\overline{\text{SEQ}}$  pin. The signature to match on is selected with the SEQ\_MATCH bits. The  $\overline{\text{SEQ}}$  signal is used to facilitate event-based sequencing in multiple-device systems. This selection would be used if the channel is being controlled by event-based sequencing.

Table 38. MFR\_SEQ\_CONFIG (E8h)

| BIT                | NAME                                          | MEANING                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |                   |          |      |                    |                                  |                        |      |                                    |            |             |                                           |              |      |                                               |             |              |          |             |      |              |      |             |      |              |      |             |      |              |      |             |      |              |
|--------------------|-----------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------------|----------|------|--------------------|----------------------------------|------------------------|------|------------------------------------|------------|-------------|-------------------------------------------|--------------|------|-----------------------------------------------|-------------|--------------|----------|-------------|------|--------------|------|-------------|------|--------------|------|-------------|------|--------------|------|-------------|------|--------------|
| 31:16              | PG_GPI_SELECT                                 | These bits are only used if SELECT[1:0] = 01; each bit corresponds to one channel (device channel N + 16 = bit number):<br>When these bits are cleared, the power good (PG) or GPI from channel N is not used in the logical AND to initiate power-on sequencing. When these bits are set, the PG or GPI is used.                                                                                                                                                                                                                                                                                                                                                                                                                                                        |                   |          |      |                    |                                  |                        |      |                                    |            |             |                                           |              |      |                                               |             |              |          |             |      |              |      |             |      |              |      |             |      |              |      |             |      |              |
| 15:12              | 0                                             | These bits always return a 0.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |                   |          |      |                    |                                  |                        |      |                                    |            |             |                                           |              |      |                                               |             |              |          |             |      |              |      |             |      |              |      |             |      |              |      |             |      |              |
| 11:8               | SEQ_MATCH                                     | These bits determine which $\overline{\text{SEQ}}$ signature the channel must match before initiating power on sequencing:<br><table><tr><td>0000</td><td>Disabled</td><td>1000</td><td>Signature 8</td></tr><tr><td>0001</td><td>Signature 1</td><td>1001</td><td>Signature 9</td></tr><tr><td>0010</td><td>Signature 2</td><td>1010</td><td>Signature 10</td></tr><tr><td>0011</td><td>Signature 3</td><td>1011</td><td>Signature 11</td></tr><tr><td>0100</td><td>Signature 4</td><td>1100</td><td>Signature 12</td></tr><tr><td>0101</td><td>Signature 5</td><td>1101</td><td>Signature 13</td></tr><tr><td>0110</td><td>Signature 6</td><td>1110</td><td>Signature 14</td></tr><tr><td>0111</td><td>Signature 7</td><td>1111</td><td>Signature 15</td></tr></table> | 0000              | Disabled | 1000 | Signature 8        | 0001                             | Signature 1            | 1001 | Signature 9                        | 0010       | Signature 2 | 1010                                      | Signature 10 | 0011 | Signature 3                                   | 1011        | Signature 11 | 0100     | Signature 4 | 1100 | Signature 12 | 0101 | Signature 5 | 1101 | Signature 13 | 0110 | Signature 6 | 1110 | Signature 14 | 0111 | Signature 7 | 1111 | Signature 15 |
| 0000               | Disabled                                      | 1000                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     | Signature 8       |          |      |                    |                                  |                        |      |                                    |            |             |                                           |              |      |                                               |             |              |          |             |      |              |      |             |      |              |      |             |      |              |      |             |      |              |
| 0001               | Signature 1                                   | 1001                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     | Signature 9       |          |      |                    |                                  |                        |      |                                    |            |             |                                           |              |      |                                               |             |              |          |             |      |              |      |             |      |              |      |             |      |              |      |             |      |              |
| 0010               | Signature 2                                   | 1010                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     | Signature 10      |          |      |                    |                                  |                        |      |                                    |            |             |                                           |              |      |                                               |             |              |          |             |      |              |      |             |      |              |      |             |      |              |      |             |      |              |
| 0011               | Signature 3                                   | 1011                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     | Signature 11      |          |      |                    |                                  |                        |      |                                    |            |             |                                           |              |      |                                               |             |              |          |             |      |              |      |             |      |              |      |             |      |              |      |             |      |              |
| 0100               | Signature 4                                   | 1100                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     | Signature 12      |          |      |                    |                                  |                        |      |                                    |            |             |                                           |              |      |                                               |             |              |          |             |      |              |      |             |      |              |      |             |      |              |      |             |      |              |
| 0101               | Signature 5                                   | 1101                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     | Signature 13      |          |      |                    |                                  |                        |      |                                    |            |             |                                           |              |      |                                               |             |              |          |             |      |              |      |             |      |              |      |             |      |              |      |             |      |              |
| 0110               | Signature 6                                   | 1110                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     | Signature 14      |          |      |                    |                                  |                        |      |                                    |            |             |                                           |              |      |                                               |             |              |          |             |      |              |      |             |      |              |      |             |      |              |      |             |      |              |
| 0111               | Signature 7                                   | 1111                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     | Signature 15      |          |      |                    |                                  |                        |      |                                    |            |             |                                           |              |      |                                               |             |              |          |             |      |              |      |             |      |              |      |             |      |              |      |             |      |              |
| 7:6                | 0                                             | These bits always return a 0.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |                   |          |      |                    |                                  |                        |      |                                    |            |             |                                           |              |      |                                               |             |              |          |             |      |              |      |             |      |              |      |             |      |              |      |             |      |              |
| 5:4                | SELECT[1:0]                                   | These bits determine the signal that initiates power-on sequencing:<br><table><tr><th colspan="3">SELECTED POWER-ON</th></tr><tr><th><u>SELECT[1:0]</u></th><th><u>SEQUENCING CONTROL SIGNAL</u></th><th><u>SEQUENCING TYPE</u></th></tr><tr><td>00</td><td>SEQUENCE0 or SEQUENCE1 (use bit 0)</td><td>Time based</td></tr><tr><td>01</td><td>PG/GPI logic combination (use bits 31:16)</td><td>Event based</td></tr><tr><td>10</td><td><math>\overline{\text{SEQ}}</math> Match (use bits 11:8)</td><td>Event based</td></tr><tr><td>11</td><td>Reserved</td><td></td></tr></table>                                                                                                                                                                                     | SELECTED POWER-ON |          |      | <u>SELECT[1:0]</u> | <u>SEQUENCING CONTROL SIGNAL</u> | <u>SEQUENCING TYPE</u> | 00   | SEQUENCE0 or SEQUENCE1 (use bit 0) | Time based | 01          | PG/GPI logic combination (use bits 31:16) | Event based  | 10   | $\overline{\text{SEQ}}$ Match (use bits 11:8) | Event based | 11           | Reserved |             |      |              |      |             |      |              |      |             |      |              |      |             |      |              |
| SELECTED POWER-ON  |                                               |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |                   |          |      |                    |                                  |                        |      |                                    |            |             |                                           |              |      |                                               |             |              |          |             |      |              |      |             |      |              |      |             |      |              |      |             |      |              |
| <u>SELECT[1:0]</u> | <u>SEQUENCING CONTROL SIGNAL</u>              | <u>SEQUENCING TYPE</u>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |                   |          |      |                    |                                  |                        |      |                                    |            |             |                                           |              |      |                                               |             |              |          |             |      |              |      |             |      |              |      |             |      |              |      |             |      |              |
| 00                 | SEQUENCE0 or SEQUENCE1 (use bit 0)            | Time based                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |                   |          |      |                    |                                  |                        |      |                                    |            |             |                                           |              |      |                                               |             |              |          |             |      |              |      |             |      |              |      |             |      |              |      |             |      |              |
| 01                 | PG/GPI logic combination (use bits 31:16)     | Event based                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |                   |          |      |                    |                                  |                        |      |                                    |            |             |                                           |              |      |                                               |             |              |          |             |      |              |      |             |      |              |      |             |      |              |      |             |      |              |
| 10                 | $\overline{\text{SEQ}}$ Match (use bits 11:8) | Event based                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |                   |          |      |                    |                                  |                        |      |                                    |            |             |                                           |              |      |                                               |             |              |          |             |      |              |      |             |      |              |      |             |      |              |      |             |      |              |
| 11                 | Reserved                                      |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |                   |          |      |                    |                                  |                        |      |                                    |            |             |                                           |              |      |                                               |             |              |          |             |      |              |      |             |      |              |      |             |      |              |      |             |      |              |
| 3:1                | 0                                             | These bits always return a 0.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |                   |          |      |                    |                                  |                        |      |                                    |            |             |                                           |              |      |                                               |             |              |          |             |      |              |      |             |      |              |      |             |      |              |      |             |      |              |
| 0                  | SEQ_SELECT                                    | 0 = SEQUENCE0<br>1 = SEQUENCE1                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |                   |          |      |                    |                                  |                        |      |                                    |            |             |                                           |              |      |                                               |             |              |          |             |      |              |      |             |      |              |      |             |      |              |      |             |      |              |

**MFR\_MARGIN\_CONFIG (DFh)**

The MFR\_MARGIN\_CONFIG command configures both the digital PWMn outputs (PWM0–PWM7) and the external DS4424 current DAC (if present) to margin the associated power supplies. If the PWMn/GPOn pin is configured with MFR\_PWM\_CONFIG for any function besides PWM operation, this selection overrides the margining functionality. The MFR\_MARGIN\_CONFIG command is described in [Table 39](#).

**Power-Supply Margining Operation**

For the power supplies connected to PSEN0–PSEN7 (PAGES 0–7), power-supply margining is implemented using the PWM0–PWM7 outputs, respectively. The PWM frequency is 312.5kHz. For power supplies connected to PSEN8–PSEN11 (PAGES 8–11), power-supply margining is implemented using the external DS4424 DAC outputs according [Table 40](#). The device close-loop controls the PWM duty cycle or DAC output current setting to margin the power supply. When margining is not active, the PWMn and DAC outputs are high impedance.

**Table 39. MFR\_MARGIN\_CONFIG (DFh)**

| BIT  | NAME      | MEANING                                                                                                                                                                                                                                                                                                                |
|------|-----------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15   | SLOPE     | DAC and PWM setting to resulting voltage relationship:<br>0 = Negative slope<br>DAC source current results in a lower voltage<br>Increasing PWM duty cycle results in a lower voltage<br>1 = Positive slope<br>DAC source current results in a higher voltage<br>Decreasing PWM duty cycle results in a higher voltage |
| 14   | OPEN_LOOP | 0 = Normal closed-loop margining<br>1 = PWM duty cycle or DAC value set constantly to the DC_DAC value when margining invoked                                                                                                                                                                                          |
| 13:8 | 0         | These bits always return a 0.                                                                                                                                                                                                                                                                                          |
| 7:0  | DC_DAC    | This 8-bit value has two purposes:<br>1) With PWM margining, it is used as the initial PWM duty cycle when the device begins to margin a power supply either up or down.<br>2) When bit 14 is set, this value is used to set the PWM duty cycle or the external current DAC level.                                     |

**Table 40. Power-Supply DAC Outputs**

| PAGE | POWER SUPPLY | DS4424 OUTPUT |
|------|--------------|---------------|
| 8    | PSEN8        | OUT0          |
| 9    | PSEN9        | OUT1          |
| 10   | PSEN10       | OUT2          |
| 11   | PSEN11       | OUT3          |

The device margins the power supplies when OPERATION is set to one of the margin states. Margining of the supplies does not begin until **ALL** power supplies have exceeded their programmed POWER\_GOOD\_ON levels. When this happens, the PWM or DAC output is enabled and margining is initiated. The device then averages four samples of  $V_{OUT}$  for a total time of 20ms. If the measured  $V_{OUT}$  and the target (set by either VOUT\_MARGIN\_HIGH or VOUT\_MARGIN\_LOW) differ by more than 1%, the PWM duty cycle or the DAC setting is adjusted by one step. The direction of the duty-cycle adjustment is determined by the SLOPE bit in MFR\_MARGIN\_CONFIG. All changes to the DAC setting are made after averaging four samples of  $V_{OUT}$  over a 20ms period.

When the OPERATION command deactivates margining, and the margining has been running with the “Ignore All Faults” condition, the device does not begin monitoring for faults for 100ms after the “Margin Off” input is received to allow time for the power supplies to return to a normal condition.

### Margining Faults

The device detects two possible margining faults. First, if the initial PWM duty cycle or DAC step causes  $V_{OUT}$

to exceed the target value (either high or low, depending on whether the device has been instructed to margin high or low, respectively), this creates a fault. Second, if the target value cannot be reached when the PWM duty cycle or DAC reaches zero or full scale, this also creates a fault. If either margining fault occurs, the device continues attempting to margin the power supply and does the following:

- 1) Sets the MARGIN bit in STATUS\_WORD.
- 2) Sets the MARGIN\_FAULT bit in STATUS\_MFR\_SPECIFIC (PAGES 0–11).
- 3) Notifies the host through  $\overline{\text{ALERT}}$  assertion (if enabled in MFR\_MODE).

If a communication error occurs between the MAX34451 and the external DS4424, a fault occurs when the MAX34451 attempts to set the DAC to full scale and the target margin value is not reached.

### DC\_DAC Value

The DC\_DAC value for the channels controlled by the PWMn outputs can be determined by the following formula. The DC\_DAC value for the channels controlled by the external current DAC is automatically configured by the device and set to 0x00h.

$$\text{PWM DC\_DAC value} = 256 \times (V_{FB}/V_{DD})$$

where  $V_{FB}$  is the power-supply feedback node voltage and  $V_{DD}$  is the supply voltage.

Example:

$$V_{FB} = 0.8\text{V}, V_{DD} = 3.3\text{V}$$

$$\text{PWM DC\_DAC value} = 256 \times (0.8/3.3) = 62\text{d} = 0\text{x}3\text{Eh}$$



**PWM/DAC Margining Component Selection**

The external components needed to realize the margining circuitry for both the PWM outputs and the current DAC outputs are shown in [Figure 14](#) and described in the formulas below:

PWM "R" =  $(V_{FB} - 0.3)/(I_{FB} \times \text{margining range} \times 120\%)$   
 where  $V_{FB}$  is the feedback node voltage and  $I_{FB}$  is the feedback node current.

Example:

$$V_{FB} = 0.8V, I_{FB} = 10\mu A, \text{margining range} = \pm 12\%$$

$$\text{PWM "R" Value} = (0.8 - 0.3)/(10\mu A \times 12\% \times 120\%) = 417k\Omega$$

DAC "R<sub>FS</sub>" =  $(7.75)/(I_{FB} \times \text{Margining range} \times 120\%)$

where  $I_{FB}$  is the feedback node current.

Example:

$$I_{FB} = 500\mu A, \text{margining range} = \pm 15\%$$

$$\text{DAC "RFS" value} = (7.75)/(500\mu A \times 15\% \times 120\%) = 86k\Omega$$

**Note:**  $40k\Omega < R_{FS} < 160k\Omega$

**Temperature Sensor Operation**

The device can monitor up to five different temperature sensors, four external sensors, plus its own internal temperature sensor. The external temperature sensors are all connected in parallel to the master I<sup>2</sup>C port (MSDA and MSCL pins). The device can support up to four DS75LV devices.

Each of the enabled temperature sensors are measured once per second. The internal temperature sensor is averaged four times to reduce the effect of noise. Each time the device attempts to read a temperature sensor, it checks for faults. For the internal temperature sensor, a fault is defined as reading greater than +130°C or less than -60°C. For the I<sup>2</sup>C temperature sensors, a fault is defined as a communication access failure. Temperature-sensor faults are reported by setting the temperature reading to 7FFFh. A temperature-sensor fault results in the setting of the TEMPERATURE bit in STATUS\_WORD and  $\overline{\text{ALERT}}$  is asserted (if enabled in MFR\_MODE). No bits are set in STATUS\_TEMPERATURE. On reset of the device, if the device cannot initialize the external DS75LV device, the TEMPERATURE bit in STATUS\_WORD is set and  $\overline{\text{ALERT}}$  is asserted (if enabled in MFR\_MODE), but the device does not attempt to reinitialize the DS75LV until 8000h is written to MFR\_TEMP\_SENSOR\_CONFIG. Reading disabled temperature sensors returns a fixed value of 0000h.

Up to four DS75LV digital temperature sensors can be controlled by the MAX34451. The A0–A2 pins on the DS75LV should be configured as shown in [Table 41](#). The thermostat function on the DS75LV is not used and hence the O.S. output should be left open circuit.

**MFR\_TEMP\_SENSOR\_CONFIG (F0h)**

The MFR\_TEMP\_SENSOR\_CONFIG command is used to configure the temperature sensors. The MFR\_TEMP\_SENSOR\_CONFIG command is described in [Table 42](#).

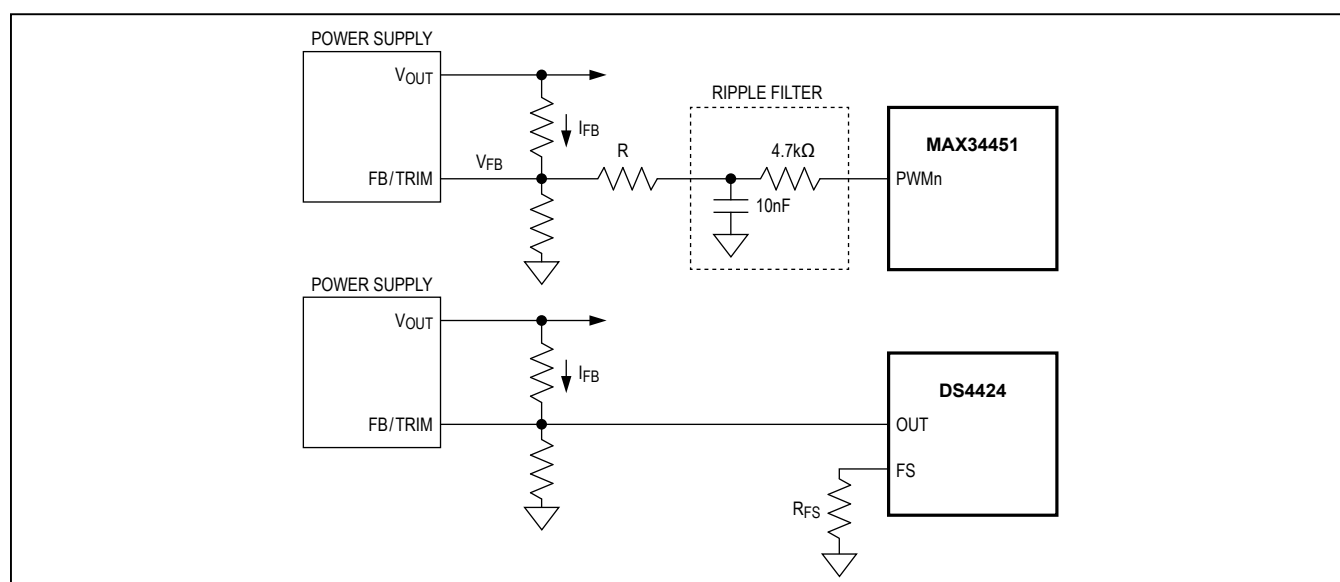


Figure 14. Margining Hardware Configurations



**Table 41. DS75LV Address Pin Configuration**

| PAGE | MAX34451 TEMP SENSOR | DS75LV ADDRESS PIN CONFIGURATION |    |    |
|------|----------------------|----------------------------------|----|----|
|      |                      | A2                               | A1 | A0 |
| 16   | MAX34451 internal    | —                                | —  | —  |
| 17   | DS75LV (address 90h) | 0                                | 0  | 0  |
| 18   | DS75LV (address 92h) | 0                                | 0  | 1  |
| 19   | DS75LV (address 94h) | 0                                | 1  | 0  |
| 20   | DS75LV (address 96h) | 0                                | 1  | 1  |

**Table 42. MFR\_TEMP\_SENSOR\_CONFIG (F0h)**

| BIT  | NAME   | MEANING                                                           |
|------|--------|-------------------------------------------------------------------|
| 15   | ENABLE | 0 = Temperature sensor disabled<br>1 = Temperature sensor enabled |
| 14:0 | 0      | These bits always return a 0.                                     |

## Applications Information

### V<sub>DD</sub>, V<sub>DDA</sub>, and REG18 Decoupling

To achieve the best results when using the device, decouple V<sub>DD</sub> and V<sub>DDA</sub> power inputs each with a 0.1μF capacitor. If possible, use a high-quality, ceramic, surface-mount capacitor. Surface-mount components minimize lead inductance, which improves performance, and ceramic capacitors tend to have adequate high-frequency response for decoupling applications. Decouple the REG18 regulator output using 1μF and 10nF capacitors with a maximum ESR of 500mΩ.

### Open-Drain Pins

MSDA, MSCL, SCL, SDA,  $\overline{\text{FAULTn}}$ ,  $\overline{\text{SEQ}}$ , and  $\overline{\text{ALERT}}$  are open-drain pins and require external pullup resistors connected to V<sub>DD</sub> to realize high logic levels.

PSEN0–PSEN11 can be user-configured as either CMOS push-pull or open-drain outputs. When configured as open drain (see MFR\_PSEN\_CONFIG), external pullup resistors connected to V<sub>DD</sub> are required to realize high logic levels.

### Keep-Alive Circuit

In systems where the power to the device may not always be present, a keep-alive circuit consisting of a Schottky diode and a bulk capacitor can be added to allow the device time to orderly shut down the power supplies it is controlling before power is lost.

### Configuration Port

Some applications require the ability to configure the device when the device has been mounted on a PCB. In such applications, a 3- or 4-wire header can be added to allow access to the slave I<sup>2</sup>C pins.

### Resistor-Dividers and Source Impedance for R<sub>Sn</sub> Inputs

The maximum full-scale voltage on the ADC inputs is 2.048V (nominal). A resistor-divider must be used to measure voltages greater than 1.8V. The maximum source impedance to the R<sub>Sn</sub> inputs is determined by the ADC\_TIME bits in MFR\_MODE. See the *Recommended Operating Conditions* section for more details.

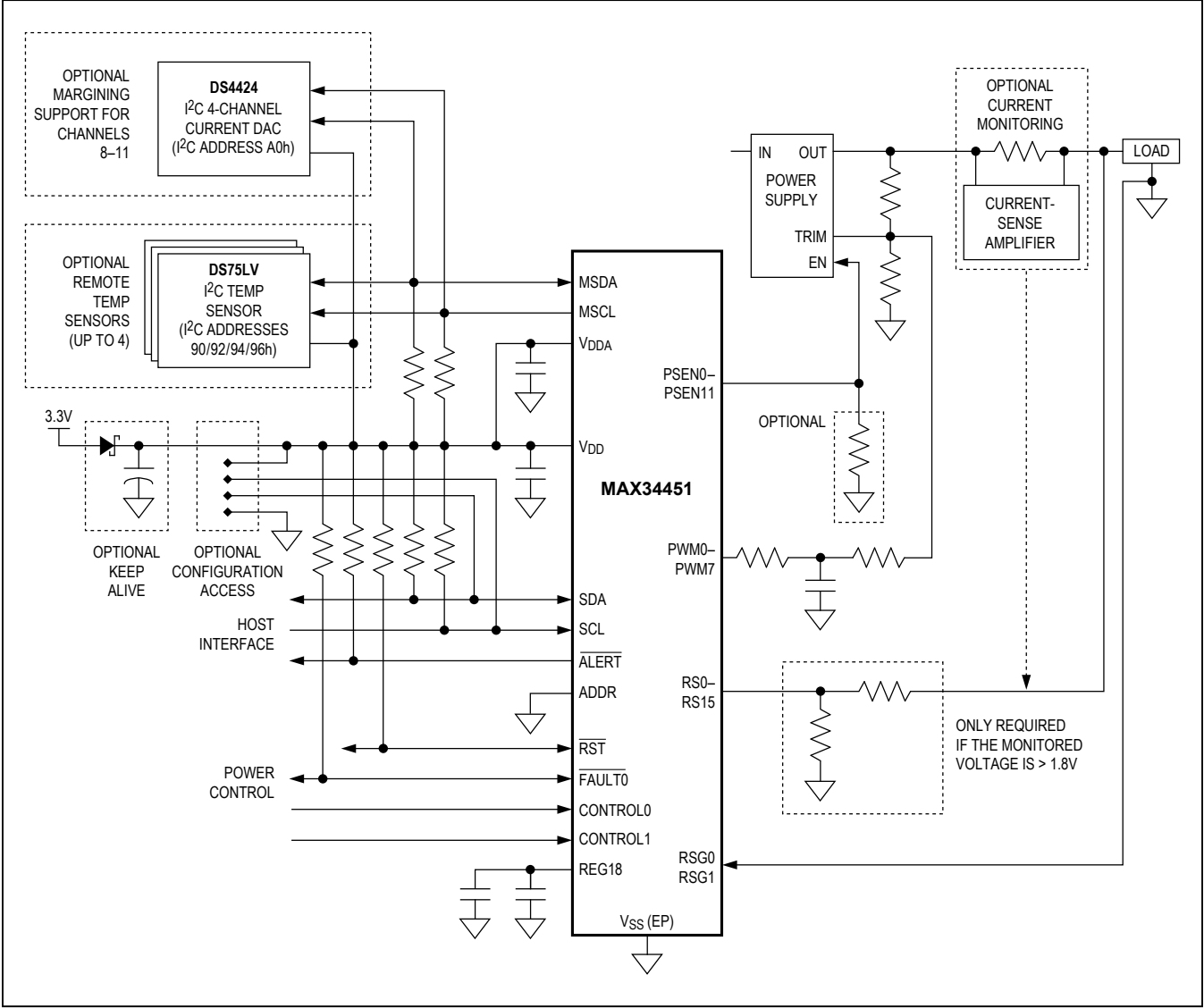
### Protecting Input Pins

In applications where voltages can be applied to the R<sub>Sn</sub> or CONTROL<sub>n</sub> signals, when V<sub>DD</sub> or V<sub>DDA</sub> is grounded, a series 100Ω resistor is recommended to protect the device by limiting power dissipation.

### Exposed Pad Grounding

The device uses the exposed pad of the TQFN package as the common ground (V<sub>SS</sub>) for the entire device. The exposed pad must be connected to the local ground plane.

Typical Operating Circuit



Package Information

For the latest package outline information and land patterns (footprints), go to [www.maximintegrated.com/packages](http://www.maximintegrated.com/packages). Note that a “+”, “#”, or “-” in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

| PACKAGE TYPE | PACKAGE CODE | OUTLINE NO. | LAND PATTERN NO. |
|--------------|--------------|-------------|------------------|
| 56 TQFN-EP   | T5677+2      | 21-0144     | 90-0043          |

## Revision History

| REVISION<br>NUMBER | REVISION<br>DATE | DESCRIPTION                                                                                                                                           | PAGES<br>CHANGED |
|--------------------|------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------|------------------|
| 0                  | 3/13             | Initial release                                                                                                                                       | —                |
| 1                  | 8/13             | Added $V_{DD}$ rise time and $V_{DD}$ source impedance to <i>Recommended Operating Conditions</i> table, updated the 7-bit slave addresses in Table 4 | 2, 17            |
| 2                  | 5/15             | Updated <i>Benefits and Features</i> section and moved <i>Ordering Information</i> to page 1                                                          | 1, 66            |

For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim Integrated's website at [www.maximintegrated.com](http://www.maximintegrated.com).

Maxim Integrated cannot assume responsibility for use of any circuitry other than circuitry entirely embodied in a Maxim Integrated product. No circuit patent licenses are implied. Maxim Integrated reserves the right to change the circuitry and specifications without notice at any time. The parametric values (min and max limits) shown in the *Electrical Characteristics* table are guaranteed. Other parametric values quoted in this data sheet are provided for guidance.

## Данный компонент на территории Российской Федерации

**Вы можете приобрести в компании MosChip.**

Для оперативного оформления запроса Вам необходимо перейти по данной ссылке:

<http://moschip.ru/get-element>

Вы можете разместить у нас заказ для любого Вашего проекта, будь то серийное производство или разработка единичного прибора.

В нашем ассортименте представлены ведущие мировые производители активных и пассивных электронных компонентов.

Нашей специализацией является поставка электронной компонентной базы двойного назначения, продукции таких производителей как XILINX, Intel (ex.ALTERA), Vicor, Microchip, Texas Instruments, Analog Devices, Mini-Circuits, Amphenol, Glenair.

Сотрудничество с глобальными дистрибьюторами электронных компонентов, предоставляет возможность заказывать и получать с международных складов практически любой перечень компонентов в оптимальные для Вас сроки.

На всех этапах разработки и производства наши партнеры могут получить квалифицированную поддержку опытных инженеров.

Система менеджмента качества компании отвечает требованиям в соответствии с ГОСТ Р ИСО 9001, ГОСТ РВ 0015-002 и ЭС РД 009

### Офис по работе с юридическими лицами:

105318, г.Москва, ул.Щербаковская д.3, офис 1107, 1118, ДЦ «Щербаковский»

Телефон: +7 495 668-12-70 (многоканальный)

Факс: +7 495 668-12-70 (доб.304)

E-mail: [info@moschip.ru](mailto:info@moschip.ru)

Skype отдела продаж:

moschip.ru

moschip.ru\_4

moschip.ru\_6

moschip.ru\_9