

32-Channel Serial-to-Parallel Converter With Open Drain Outputs

Features

- 100 mA Minimum Sink Current
- 8 MHz Shift Register Speed
- Polarity and Blanking Inputs
- CMOS-compatible Inputs
- Forward and Reverse Shifting Options
- Diode to V_{PP} allows Efficient Power Recovery

Applications

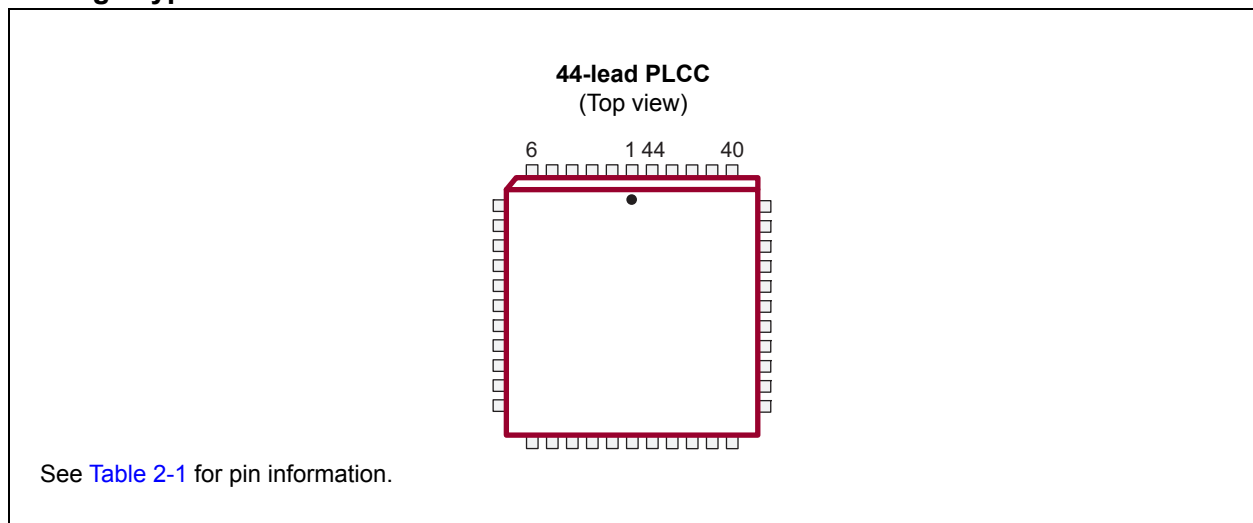
- Display Driver
- Inkjet Driver
- Print Head Driver
- Microelectromechanical Systems Applications

General Description

The HV5630 is a low-voltage to high-voltage serial-to-parallel converter with open drain outputs. This device has been designed for use as a driver for AC-electroluminescent displays. It can also be used in any application requiring multiple-output high-voltage current-sinking capabilities, such as driving inkjet and electrostatic print heads, plasma panels, vacuum fluorescent and large matrix LCD displays.

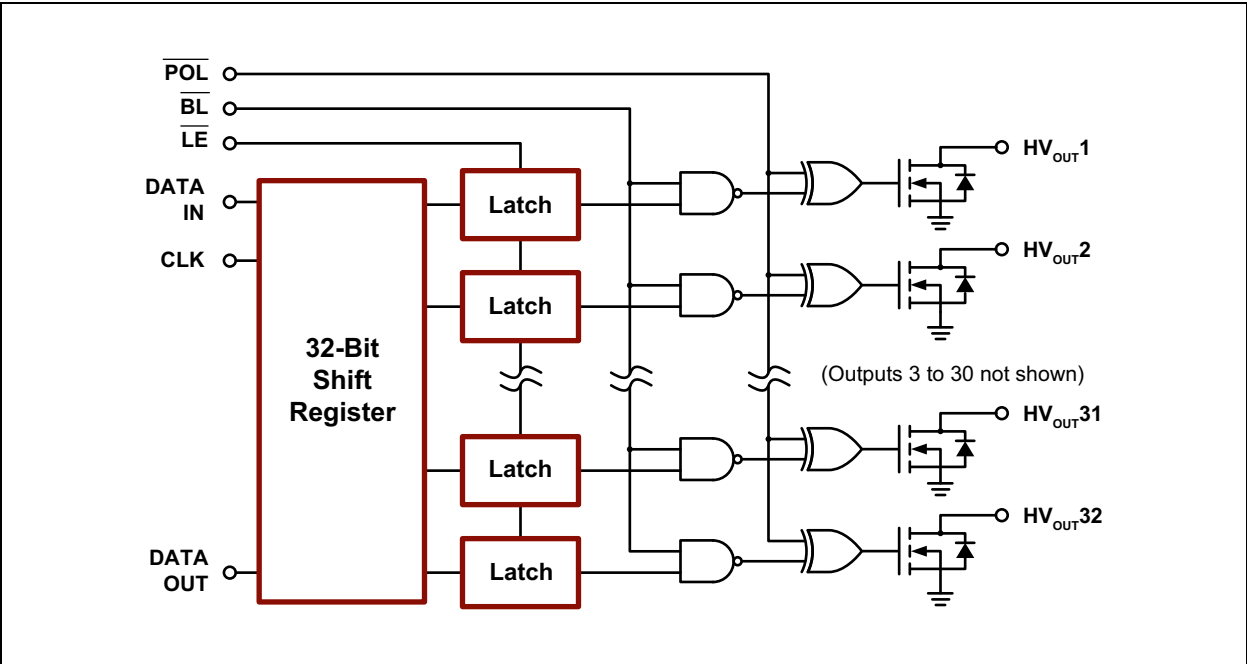
The device consists of a 32-bit Shift register, 32 latches and control logic to perform the polarity select and blanking of the outputs. Data is shifted through the Shift register on the high-to-low transition of the clock. The HV5630 shifts in a clockwise direction when viewed from the top of the package. A data output buffer is provided for cascading devices. This output reflects the current status of the last bit of the Shift register. The operation of the Shift register is not affected by the latch enable (\overline{LE}), blanking (\overline{BL}) and polarity (\overline{POL}) inputs. The transfer of data from the Shift register to the latch occurs when the \overline{LE} input is high. The data in the latch is stored when \overline{LE} is low.

Package Type

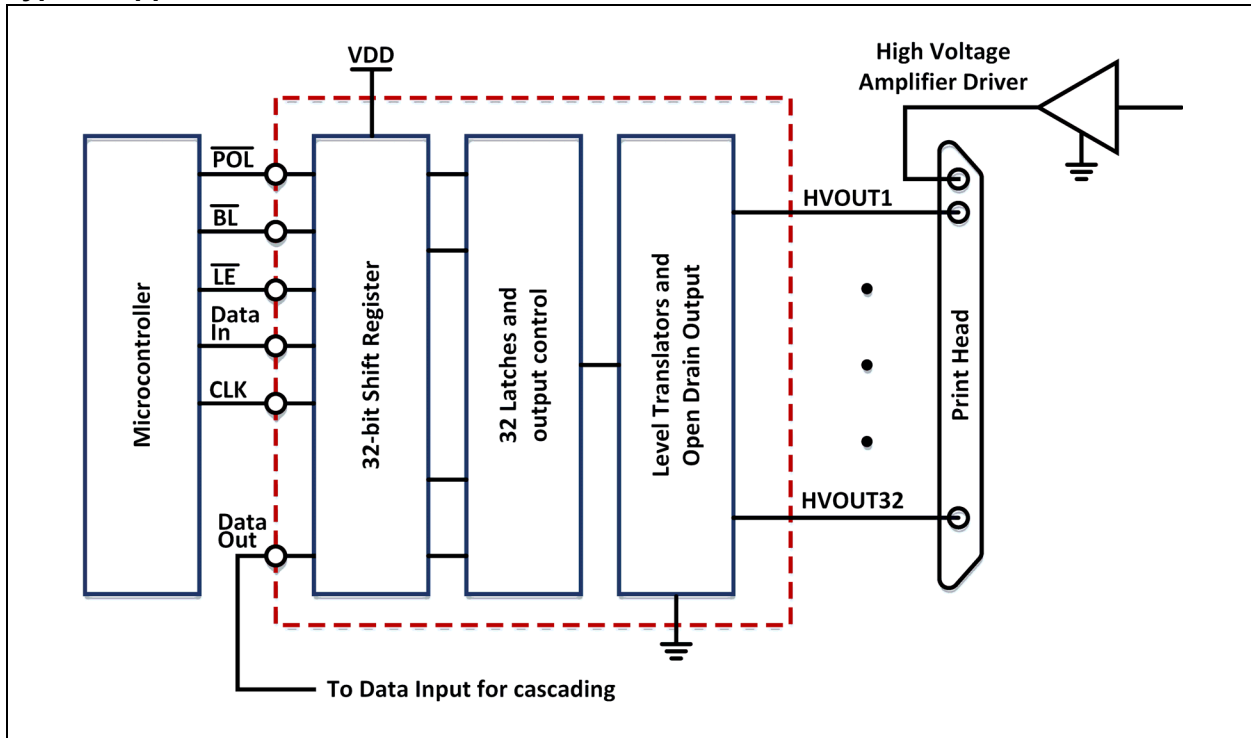


HV5630

Functional Block Diagram



Typical Application Circuit



HV5630

1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings†

Supply Voltage, V_{DD} (Note 1)	–0.5V to +15V
High-voltage Output Voltage, HV_{OUT} (Note 1)	–0.5V to +315V
Logic Input Levels (Note 1)	–0.5V to $V_{DD}+0.5V$
Ground Current (Note 2)	1.5A
Maximum Junction Temperature, $T_{J(MAX)}$	+125°C
Storage Temperature, T_S	–65°C to +150°C
Continuous Total Power Dissipation:	
44-lead PLCC (Note 3)	1200 mW

† **Notice:** Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

- Note 1:** All voltages are referenced to V_{SS} .
Note 2: Duty cycle is limited by the total power dissipated in the package.
Note 3: For operations above 25°C ambient, derate linearly to the maximum operating temperature at 20 mW/°C.

RECOMMENDED OPERATING CONDITIONS

Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
Logic Supply Voltage	V_{DD}	10.8	—	13.2	V	
High-voltage Output Voltage	HV_{OUT}	–0.3	—	+300	V	
High-level Input Voltage	V_{IH}	$V_{DD}-2$	—	V_{DD}	V	
Low-level Input Voltage	V_{IL}	0	—	2	V	
Clock Frequency	f_{CLK}	—	—	8	MHz	
Operating Ambient Temperature	T_A	–40	—	+85	°C	

DC ELECTRICAL CHARACTERISTICS

Electrical Specifications: Over recommended operating conditions unless otherwise stated							
Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions	
V _{DD} Supply Current	I _{DD}	—	—	15	mA	f _{CLK} = 8 MHz, f _{DATA} = 4 MHz	
Quiescent V _{DD} Supply Current	I _{DDQ}	—	—	100	μA	V _{IN} = 0V	
Off State Output Current	I _{O(OFF)}	—	—	10	μA	All outputs high, all SWS parallel	
High-level Logic Input Current	I _{IH}	—	—	1	μA	V _{IH} = V _{DD}	
Low-level Logic Input Current	I _{IL}	—	—	-1	μA	V _{IL} = 0V	
High-level Output Data Out	V _{OH}	V _{DD} -1V	—	—	V	I _{DOUT} = -100 μA	
Low-level Output Voltage	HV _{OUT}	V _{OL}	—	—	15	V	I _{HVOUT} = 100 mA
	Data Out				1	V	I _{DOUT} = 100 μA
HV _{OUT} Clamp Voltage	V _{OC}	—	—	-1.5	V	I _{OL} = -100 mA	

AC ELECTRICAL CHARACTERISTICS

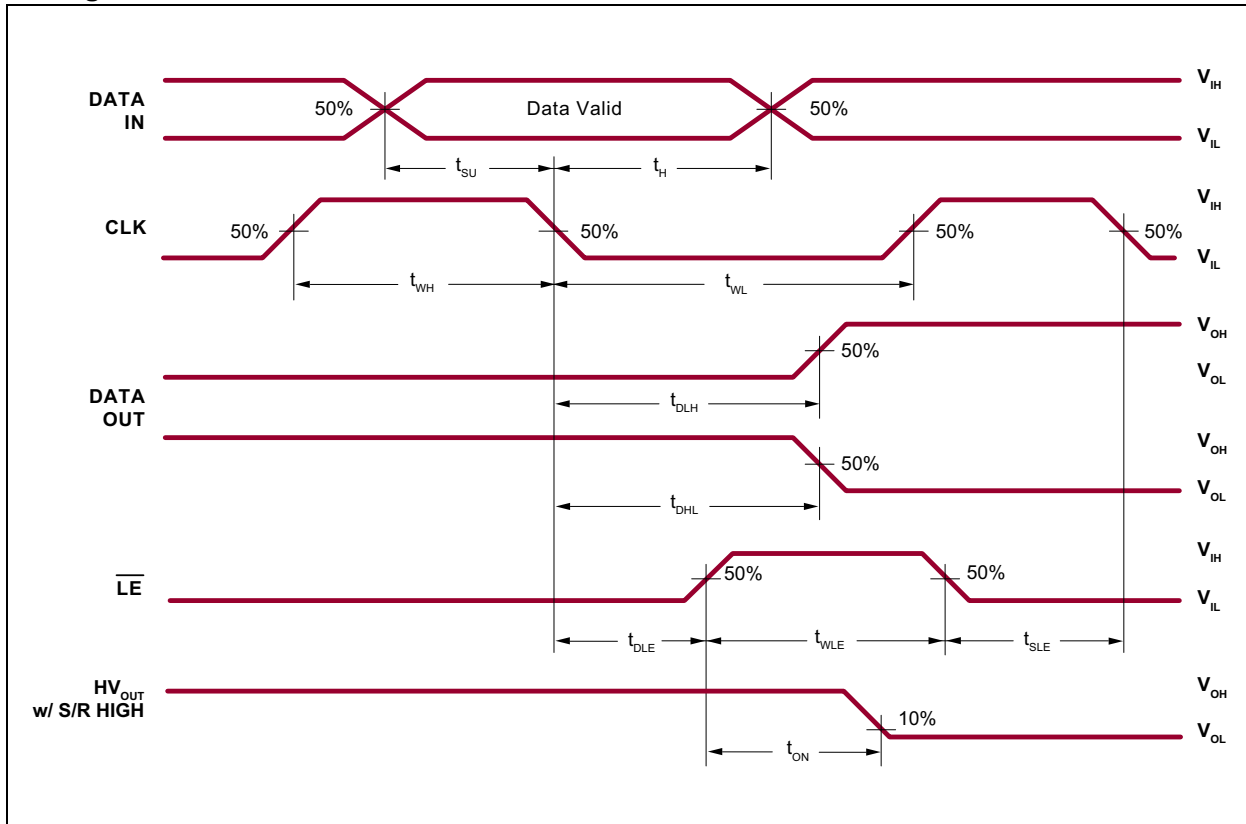
Electrical Specifications: For V _{DD} = 12V and T _A = 25°C						
Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
Clock Frequency	f _{CLK}	—	—	8	MHz	
Clock Width High or Low	t _{WL} , t _{WH}	62	—	—	ns	
Data Set-up Time before Clock Falls	t _{SU}	25	—	—	ns	
Data Hold Time after Clock Falls	t _H	10	—	—	ns	
Turn-on Time, HV _{OUT} from Enable	t _{ON}	—	—	500	ns	R _L = 2 kΩ to V _{PP} maximum
Latch Enable Pulse Width	t _{WLE}	50	—	—	ns	
Delay Time Clock to Latch Enable Low to High	t _{DLE}	50	—	—	ns	
Latch Enable Set-up Time before Clock Falls	t _{SLE}	50	—	—	ns	
Delay Time Clock to Data Low to High	t _{DLH}	—	—	100	ns	C _L = 15 pF
Delay Time Clock to Data High to Low	t _{DHL}	—	—	100	ns	C _L = 15 pF

TEMPERATURE SPECIFICATIONS

Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
TEMPERATURE RANGE						
Operating Ambient Temperature	T _A	-40	—	+85	°C	
Maximum Junction Temperature	T _{J(MAX)}	—	—	+125	°C	
Storage Temperature	T _S	-65	—	+150	°C	
PACKAGE THERMAL RESISTANCE						
44-lead PLCC	θ _{JA}	—	37	—	°C/W	

HV5630

Timing Waveforms



2.0 PIN DESCRIPTION

The details on the pins of HV5630 are in [Table 2-1](#).

Refer to [Package Type](#) for the location of pins.

TABLE 2-1: PIN FUNCTION TABLE

Pin Number	Pin Name	Description
1	HVOUT17	High-voltage output
2	HVOUT16	High-voltage output
3	HVOUT15	High-voltage output
4	HVOUT14	High-voltage output
5	HVOUT13	High-voltage output
6	HVOUT12	High-voltage output
7	HVOUT11	High-voltage output
8	HVOUT10	High-voltage output
9	HVOUT9	High-voltage output
10	HVOUT8	High-voltage output
11	HVOUT7	High-voltage output
12	HVOUT6	High-voltage output
13	HVOUT5	High-voltage output
14	HVOUT4	High-voltage output
15	HVOUT3	High-voltage output
16	HVOUT2	High-voltage output
17	HVOUT1	High-voltage output
18	DATA OUT	Data output pin
19	NC	No connection
20	NC	No connection
21	NC	No connection
22	$\overline{\text{POL}}$	Inverts the polarity of the HVOUT pins
23	CLK	Clock pin. Shift registers shift data on the falling edge of the input clock.
24	VSS	Reference voltage (usually ground)
25	VDD	Logic supply voltage
26	$\overline{\text{LE}}$	Latch enable pin. Data is shifted from the Shift register to the latches on logic input high.
27	DATA IN	Data input pin
28	$\overline{\text{BL}}$	This blanking pin sets all HVOUT pins low or high depending upon the state of polarity. See Table 3-2 .
29	NC	No connection
30	HVOUT32	High-voltage output
31	HVOUT31	High-voltage output
32	HVOUT30	High-voltage output
33	HVOUT29	High-voltage output
34	HVOUT28	High-voltage output
35	HVOUT27	High-voltage output

HV5630

TABLE 2-1: PIN FUNCTION TABLE (CONTINUED)

Pin Number	Pin Name	Description
36	HVOUT26	High-voltage output
37	HVOUT25	High-voltage output
38	HVOUT24	High-voltage output
39	HVOUT23	High-voltage output
40	HVOUT22	High-voltage output
41	HVOUT21	High-voltage output
42	HVOUT20	High-voltage output
43	HVOUT19	High-voltage output
44	HVOUT18	High-voltage output

3.0 FUNCTIONAL DESCRIPTION

Follow the steps in [Table 3-1](#) to power up and power down the HV5630.

TABLE 3-1: POWER-UP AND POWER-DOWN SEQUENCE

Power-up		Power-down	
Step	Description	Step	Description
1	Connect ground.	1	Remove all inputs.
2	Apply V_{DD} .	2	Remove V_{DD} .
3	Set all inputs to a known state.	3	Disconnect ground.

TABLE 3-2: TRUTH FUNCTION TABLE

Function	Inputs					Outputs				
	Data	CLK	\overline{LE}	\overline{BL}	\overline{POL}	Shift Register		High-voltage Output		Data Out
						1	2...32	1	2...32	*
All On	X	X	X	L	L	*	*...*	On	On...On	*
All Off	X	X	X	L	H	*	*...*	Off	Off...Off	*
Invert Mode	X	X	L	H	L	*	*...*	$\overline{*}$	$\overline{*...*}$	*
Load S/R	H or L	↓	L	H	H	H or L	*...*	*	*...*	*
Load Latches	X	H or L	↑	H	H	*	*...*	*	*...*	*
	X	H or L	↑	H	L	*	*...*	$\overline{*}$	$\overline{*...*}$	*
Transparent Latch Mode	L	↓	H	H	H	L	*...*	Off	*...*	*
	H	↓	H	H	H	H	*...*	On	*...*	*

Note: H = High-logic level
 L = Low-logic level
 X = Irrelevant
 ↓ = High-to-low transition
 ↑ = Low-to-high transition
 * = Dependent on the previous stage's state before the last CLK ↓ or last \overline{LE} high

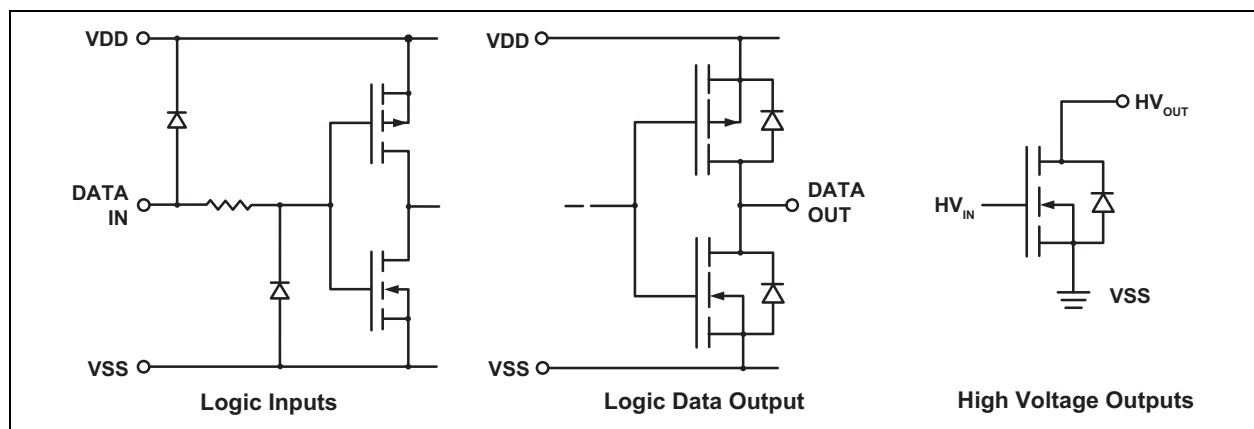
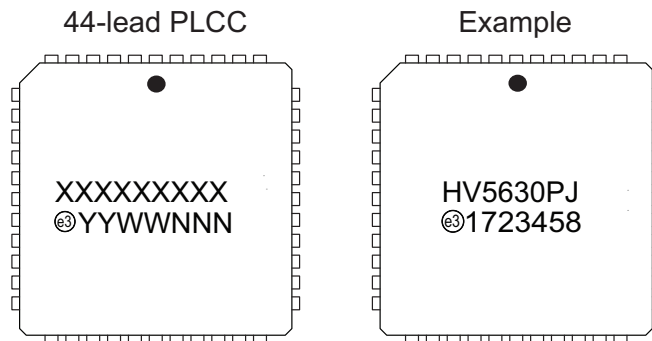


FIGURE 3-1: Input and Output Equivalent Circuits.

HV5630

4.0 PACKAGE MARKING INFORMATION

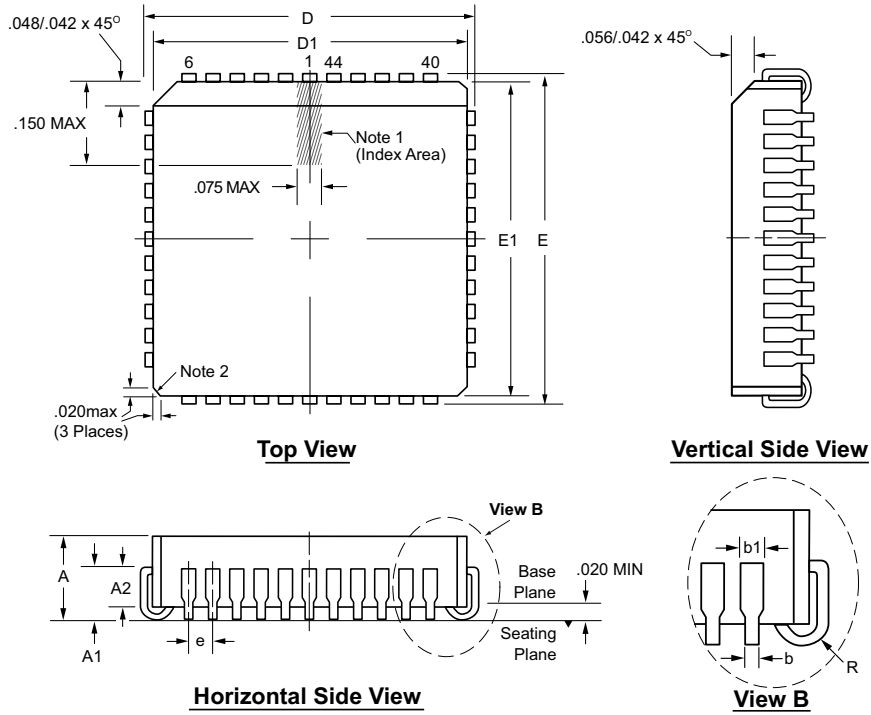
4.1 Packaging Information



Legend:	XX...X	Product Code or Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code
	ⓔ3	Pb-free JEDEC [®] designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator (ⓔ3) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for product code or customer-specific information. Package may or not include the corporate logo.

44-Lead PLCC Package Outline (PJ) .653x.653in body, .180in height (max), .050in pitch



Note: For the most current package drawings, see the Microchip Packaging Specification at www.microchip.com/packaging.

Notes:

1. A Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.
2. Actual shape of this feature may vary.

Symbol	A	A1	A2	b	b1	D	D1	E	E1	e	R	
Dimension (inches)	MIN	.165	.090	.062	.013	.026	.685	.650	.685	.650	.050 BSC	.025
	NOM	.172	.105	-	-	-	.690	.653	.690	.653		.035
	MAX	.180	.120	.083	.021	.036†	.695	.656	.695	.656		.045

JEDEC Registration MS-018, Variation AC, Issue A, June, 1993.

† This dimension differs from the JEDEC drawing.

Drawings not to scale.

HV5630

NOTES:

APPENDIX A: REVISION HISTORY

Revision A (October 2017)

- Converted Supertex Doc # DSFP-HV5630 to Microchip DS20005855A
- Removed “Processed with HVCMOS® Technology” in the Features section
- Changed the package marking format
- Removed the 44-lead PLCC PJ M903 media type
- Made minor changes throughout the document

HV5630

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

<u>PART NO.</u>	<u>XX</u>	-	<u>X</u>	-	<u>X</u>
Device	Package Options		Environmental		Media Type
Device:	HV5630	=	32-Channel Serial-to-Parallel Converter with Open Drain Outputs		
Package:	PJ	=	44-lead PLCC		
Environmental:	G	=	Lead (Pb)-free/RoHS-compliant Package		
Media Type:	(blank)	=	27/Tube for a PJ Package		

Example:

a) HV5630PJ-G: 32-Channel Serial-to-Parallel Converter with Open Drain Outputs, 44-lead PLCC, 27/Tube

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На всех этапах разработки и производства наши партнеры могут получить квалифицированную поддержку опытных инженеров.

Система менеджмента качества компании отвечает требованиям в соответствии с ГОСТ Р ИСО 9001, ГОСТ РВ 0015-002 и ЭС РД 009

Офис по работе с юридическими лицами:

105318, г.Москва, ул.Щербаковская д.3, офис 1107, 1118, ДЦ «Щербаковский»

Телефон: +7 495 668-12-70 (многоканальный)

Факс: +7 495 668-12-70 (доб.304)

E-mail: info@moschip.ru

Skype отдела продаж:

moschip.ru

moschip.ru_4

moschip.ru_6

moschip.ru_9