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## DS8500

## HART Modem

### General Description

The DS8500 is a single-chip modem with Highway Addressable Remote Transducer (HART) capabilities. It has been fully tested and verified and has received a HART® Certificate of Registration. The device integrates the modulation and demodulation of the 1200Hz/2200Hz FSK signal, has very low power consumption, and needs only a few external components due to the integrated digital signal processing. The input signal is sampled by an analog-to-digital converter (ADC), followed by a digital filter/demodulator. This architecture ensures reliable signal detection in noisy environments. The output digital-to-analog converter (DAC) generates a sine wave and provides a clean signal with phase-continuous switching between 1200Hz and 2200Hz. Low power is achieved by disabling the receive circuits during transmit and vice versa. The DS8500 is ideal for low-power process control transmitters.

### Applications

- 4mA–20mA Loop-Powered Transmitters for Temperature, Pressure, Flow, and Level Measurement
- HART Multiplexers
- HART Modem Interface Connectivity

*HART is a registered trademark of the HART Communication Foundation. Membership in the HART Communication Foundation does not guarantee a product has been verified or received a HART Registration Certificate.*

### Benefits and Features

- Single-Chip, Half-Duplex Modem Overlays 1200bps FSK Digital Communication on Top of Installed 4mA–20mA Current Loop Infrastructure
- Digital Signal Processing Provides Reliable Input Signal Detection in Noisy Conditions
- Standard Component 3.6864MHz Crystal Reduces System Cost
- Fully Tested and Verified as a HART-Registered Modem IC
- Integrated Solution Requires Minimal Power and Space
  - 2.7V to 3.6V Operating Voltage
  - 285µA (max) Current Consumption
  - Space-Saving, 5mm x 5mm x 0.8mm, 20-Pin TQFN Package
  - Few External Components Required

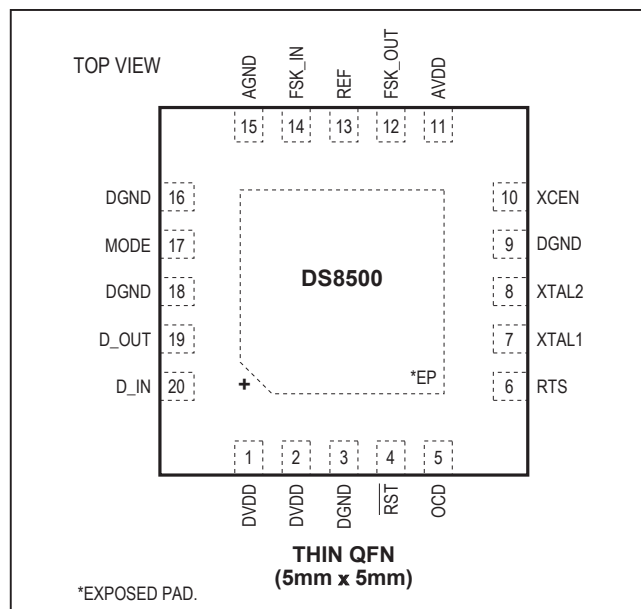
### Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
DS8500-JND+	-40°C to +85°C	20 TQFN-EP*

+Denotes a lead(Pb)-free/RoHS-compliant package.

\*EP = Exposed pad.

### Pin Configuration



## Absolute Maximum Ratings

Voltage Range on All Pins (including AVDD, DVDD) Relative to Ground .....-0.5V to +3.6V  
 Voltage Range on Any Pin Relative to Ground Except AVDD, DVDD.....-0.5V to ( $V_{DVDD} + 0.5V$ )

Operating Temperature Range..... -40°C to +85°C  
 Storage Temperature Range ..... -65°C to +150°C  
 Soldering Temperature .....Refer to the IPC/JEDEC J-STD-020 Specification.

*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

## Recommended DC Operating Conditions

( $V_{DVDD} = V_{AVDD} = 2.7V$  to  $3.6V$ ,  $T_A = -40^\circ C$  to  $+85^\circ C$ .) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Digital Supply Voltage	$V_{DVDD}$		2.7		3.6	V
Analog Supply Voltage	$V_{AVDD}$	$V_{AVDD} = V_{DVDD}$	2.7		3.6	V
Ground	GND	AGND = DGND	0		0	V
Digital Power-Fail Reset Voltage	$V_{RST}$	Monitors $V_{DVDD}$	2.59	2.64	2.69	V
Active Current	$I_{DD}$	$V_{AVDD} = V_{DVDD} = 2.7V$ (Note 2)			285	$\mu A$
Input Low Voltage	$V_{IL}$		DGND		$0.30 \times V_{DVDD}$	V
Input High Voltage	$V_{IH}$		$0.75 \times V_{DVDD}$		$V_{DVDD}$	V
Output Low Voltage	$V_{OL}$	$I_{OL} = 4mA$	DGND		0.4	V
Output High Voltage	$V_{OH}$	$I_{OH} = -4mA$	$0.8 \times V_{DVDD}$			V
I/O Pin Capacitance	$C_{IO}$	Guaranteed by design (Note 3)			15	pF
$\overline{RST}$ Pullup Resistance	$R_{RST}$		19		45	k $\Omega$
Input Leakage Current XTAL, $\overline{RST}$	$I_{ILRX}$		-30		+30	$\mu A$
Input Leakage Current All Other Pins	$I_{IL}$		-2		+2	$\mu A$
Input Low Current for $\overline{RST}$	$I_{IL1}$	$V_{IN} = 0.4V$			170	$\mu A$
<b>CLOCK SOURCE</b>						
External Clock Frequency	$f_{HFIN}$		-1%	3.6864	+1%	MHz
<b>VOLTAGE REFERENCE</b>						
Internal Reference Voltage	$V_{REF}$	(Note 5)		1.23		V
<b>FSK INPUT</b>						
Input Voltage Range at FSK_IN			0		$V_{REF}$	V
<b>FSK OUTPUT</b>						
Output Voltage at FSK_OUT	$V_{OUT}$	AC-coupled max 30k $\Omega$ load	400	500	600	mV <sub>P-P</sub>
Frequency of FSK_OUT (Note 4)		For a mark	-1%	1200	+1%	Hz
		For a space	-1%	2200	+1%	

**Note 1:** Specifications to  $-40^\circ C$  are guaranteed by design and are not production tested.

**Note 2:** Active currents are measured when the device is driven by an external clock XCEN = 1 condition.

**Note 3:** Guaranteed by design and not production tested.

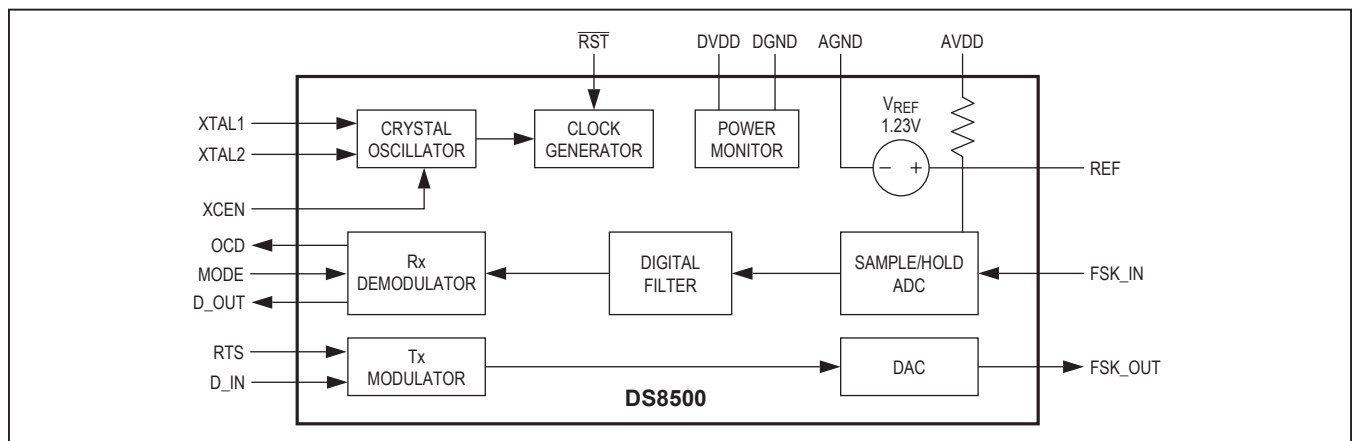
**Note 4:** Accuracy is guaranteed based on the external crystal or clock provided.

**Note 5:**  $V_{REF}$  voltage is output only in demodulator mode.

Pin Description

PIN	NAME	FUNCTION
1, 2	DVDD	Digital Supply Voltage
3, 9, 16, 18	DGND	Digital Ground
4	RST	Active-Low Reset, Digital Input/Output. This pin includes an internal pullup resistor and is driven low as an output when an internal reset condition occurs.
5	OCD	Carrier Detect, Digital Output. A logic-high indicates a valid carrier detection on FSK_IN. OCD = 1 when FSK_IN amplitude is greater than 120mV <sub>P-P</sub> . OCD = 0 when FSK_IN amplitude is less than 80mV <sub>P-P</sub> .
6	RTS	Request to Send, Digital Input. When set high, the device is put into the demodulator mode. A logic-low puts the device into modulator mode.
7	XTAL1	Crystal Pin or Input for External Clock at 3.6864MHz
8	XTAL2	Crystal Pin or Output of the Crystal Amplifier
10	XCEN	External Clock Enable, Digital Input. When set high, this pin allows the user to drive an external clock signal through XTAL1. When in this mode, XTAL2 should be left unconnected. An external crystal must be connected between XTAL1 and XTAL2 when set low.
11	AVDD	Analog Supply Voltage
12	FSK_OUT	FSK Out, Analog Output. Output of the modulator. Provides a phase-continuous, FSK-modulated output signal (1200Hz and 2200Hz output frequencies) to the 4–20mA current loop interface circuit.
13	REF	Reference, Analog Output. The internal voltage reference is provided as an output when in demodulator mode. This pin must be connected to a 0.1µF capacitor.
14	FSK_IN	FSK In, Analog Input. Input for the FSK-modulated HART receive signal from the 4–20mA current loop interface circuit.
15	AGND	Analog Ground
17	MODE	This pin should be tied high for HART applications. This pin can also be tied low for support of legacy designs.
19	D_OUT	Digital Data Out, Digital Output. Output from the demodulator.
20	D_IN	Digital Data In, Digital Input. Input to the modulator.
—	EP	Exposed Pad. Should be connected to ground (DGND, AGND).

Block Diagram



## Introduction to HART

HART is a backward-compatible enhancement to existing 4–20mA instrumentation networks that allows two-way, half-duplex, digital communication with a microcontroller-based field device. The digital signal is encoded on top of the existing instrumentation signal. Communication is accomplished through a series of commands and responses dependent on the specific protocol and network topology. The DS8500 does not implement any portion of the communication protocol; it only handles the modulation and demodulation of the encoded information. Digital data is encoded using frequency-shift keying (FSK), which is illustrated in [Figure 1](#). A “1” is identified as a mark symbol and is represented with a center frequency of 1.2kHz. A “0” is identified as a space symbol and is represented with a center frequency of 2.2kHz. This allows a throughput of 1.2kbps, with each symbol occupying an 833 $\mu$ s slot.

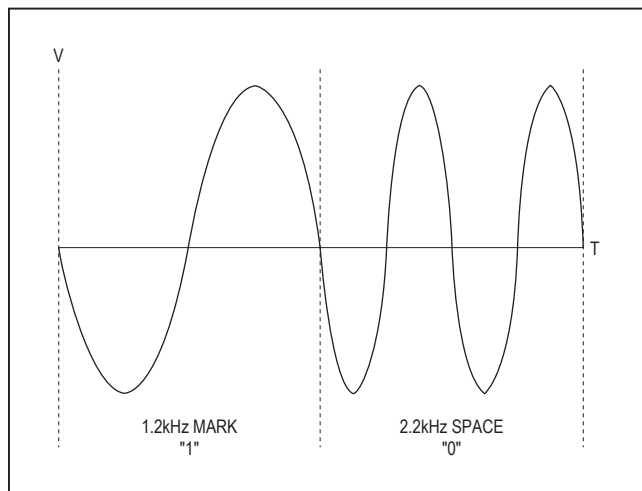


Figure 1. HART FSK Signal

## Functional Description

The DS8500 modem chip consists of a demodulator, carrier detect, digital filter, ADC for input signal conversion, a modulator and DAC for output signal generation, and receive and transmit state machine blocks to perform the HART communication. The [Block Diagram](#) illustrates the interface between various blocks of circuitry. The input HART signal's noise interference is attenuated by a one-pole highpass filter that is external to the chip; the attenuated signal is digitized by the ADC and filtered by the receive state machine. The transmit state machine modulates the input to the HART-compliant signal with the help of the modulator and the DAC.

## Modulator

The modulator performs the FSK modulation of the digital data at the D\_IN input. The FSK-modulated sinusoidal signal is present at the FSK\_OUT output as illustrated in [Figure 1](#). The modulator is enabled by RTS being a logic-low. The modulation is done between 1200Hz (mark) or 2200Hz (space) depending on the logic level of the input signal. The modulator preserves a continuous phase when switching between frequencies to minimize the bandwidth of the transmitted signal.

[Figure 2](#) illustrates an example waveform of the DS8500 in modulate mode. The data to be modulated is presented in a UART format (start, 8 data bits, parity, stop bit) at D\_IN. FSK\_OUT shows the modulated output.

## Demodulator

The demodulator accepts an FSK signal at the FSK\_IN input and reproduces the original modulating signal at the D\_OUT output. The HART signal should be presented as an 11-bit UART character with a start, data, parity, and stop bits for proper operation of the demodulator block. The nominal bit rate of the D\_OUT signal is 1200 bits per second. A simple RC filter is sufficient for anti-aliasing. [Figure 3](#) illustrates an example waveform of the DS8500 in demodulate mode.

## Applications Information

[Figure 4](#) shows the typical application circuit. As the DS8500 integrates a digital filter, only a simple passive RC filter is required in front of the ADC. R3 and C3 implement a lowpass filter with a 10kHz cutoff frequency; C2 and R2/R1 implement a highpass filter with a 480Hz cutoff frequency. The resistor-divider formed by R1 and R2 provides an input bias voltage of  $V_{REF}/2$  to the ADC input ( $R1 = R2$ ) when in demodulator mode.  $V_{REF}$  is powered down in modulator mode in order to save power.

The output DAC provides a sine-wave signal, and C4 provides the AC-coupled signal output from the DS8500. The typical value of C4 can be anything greater than 20nF based on the application.

## HART Registration

This IC has been tested and has received a Modem IC Registration Certificate from the HART Communication Foundation. The use of this HART-registered IC reduces the customer cost and effort associated with achieving HART registration of the end product.

A copy of the DS8500 Registration Certificate (L2-06-1000-346) is available from the HART Communication Foundation at [www.hartcomm.org](http://www.hartcomm.org).

## Technical Support

For technical support, go to <http://support.maximintegrated.com/micro>.

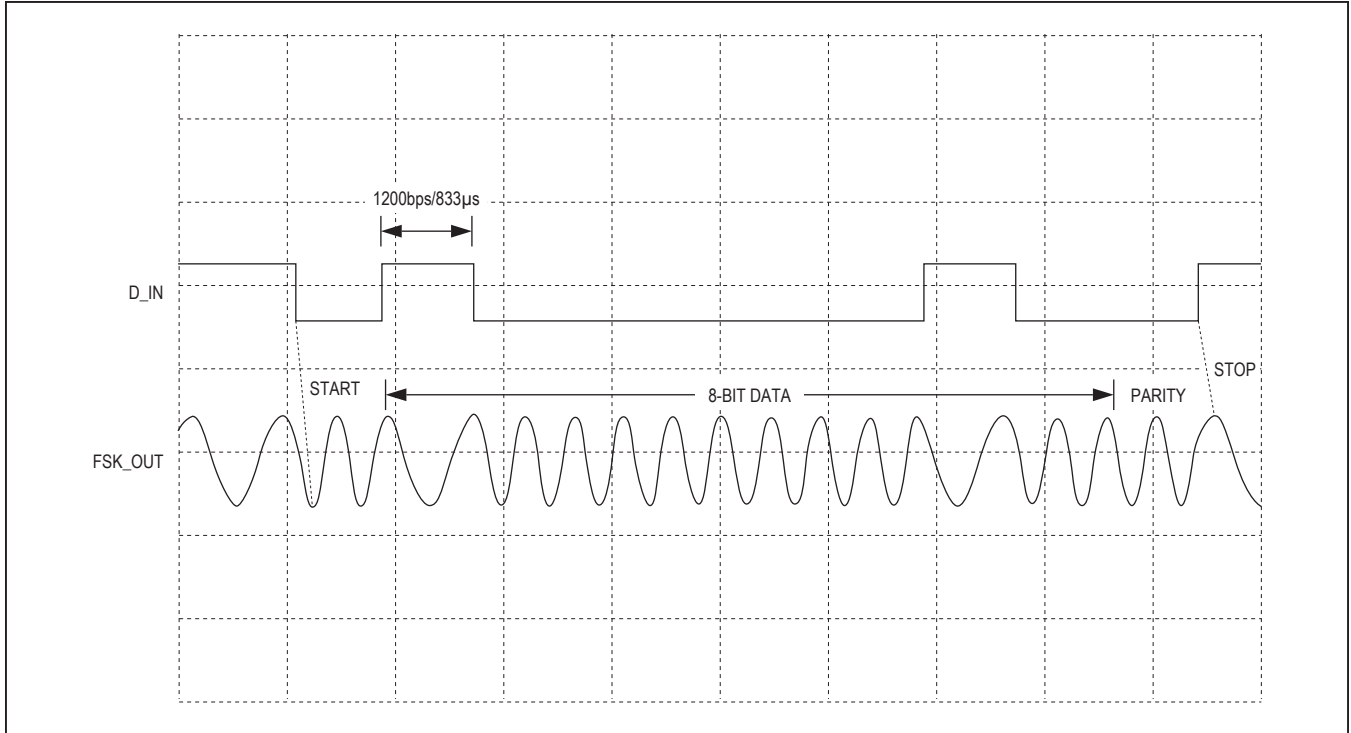


Figure 2. Actual DS8500 Modulator Waveform

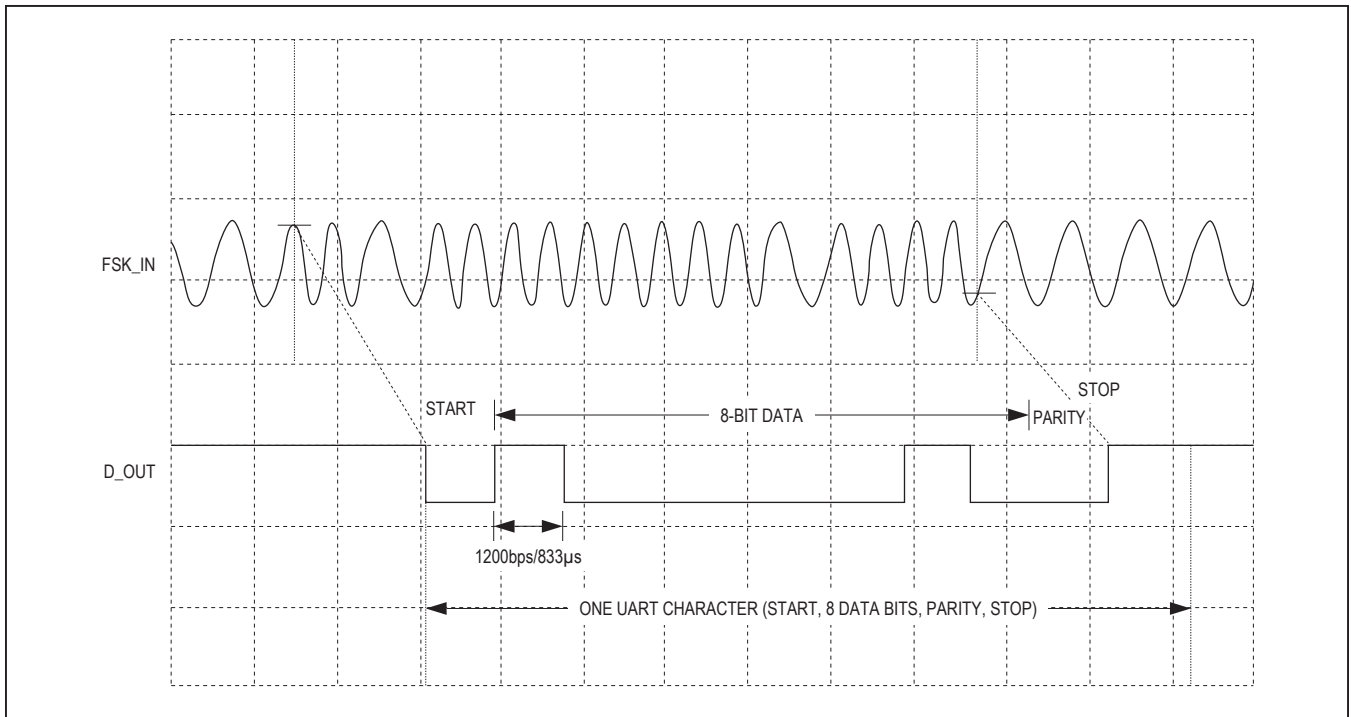


Figure 3. Actual DS8500 Demodulator Waveform

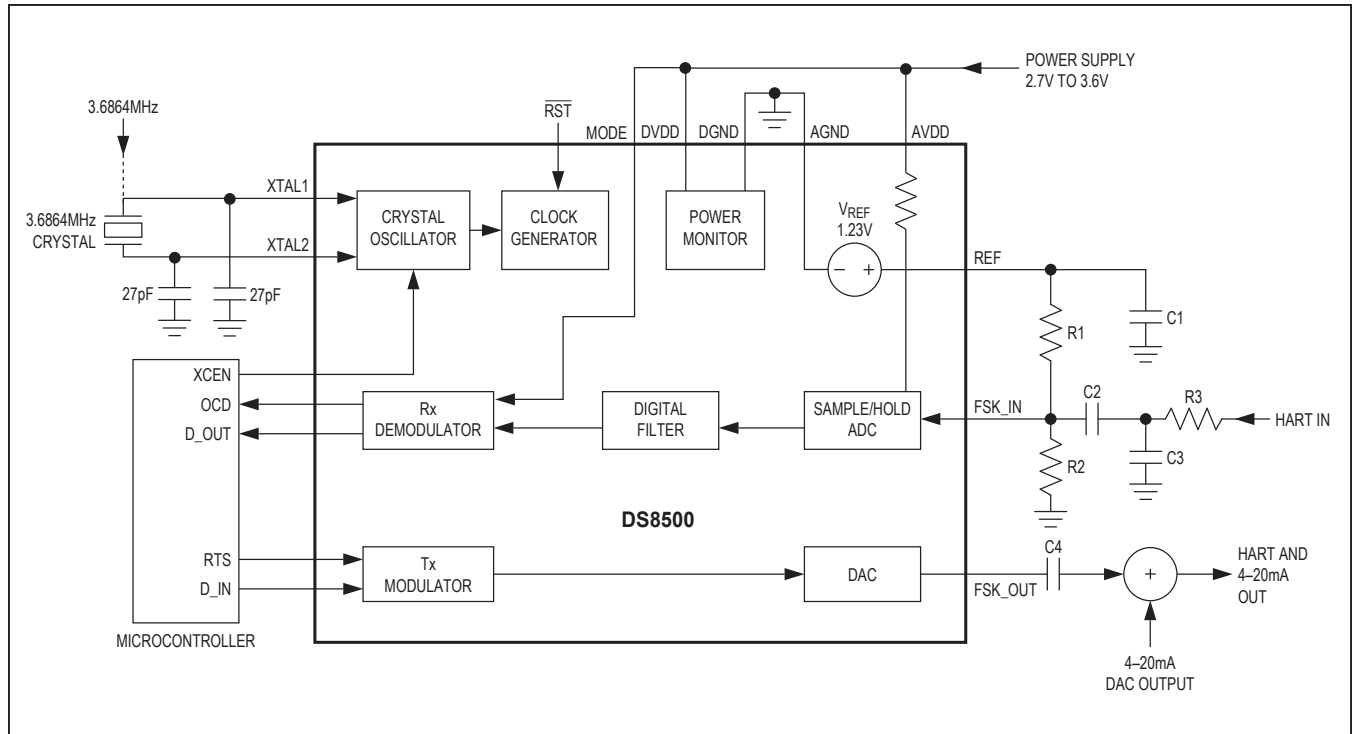


Figure 4. Typical Application Circuit

### Package Information

For the latest package outline information and land patterns (footprints), go to [www.maximintegrated.com/packages](http://www.maximintegrated.com/packages). Note that a “+”, “#”, or “-” in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
20 TQFN	T2055+3	<a href="#">21-0140</a>	<a href="#">90-0008</a>

## Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	10/08	Initial release.	—
1	2/09	In the <i>Electrical Characteristics</i> table, changed the Frequency of FSK_OUT parameter units from kHz to Hz.	2
		Added the EP description to the <i>Pin Description</i> table.	3
2	4/15	Updated <i>Benefits and Features</i> section, added HART registration information, clarified alternate function of pin 17	1, 3, 4, 6
3	2/20	Updated <i>Recommended DC Operating Conditions</i> , added Note 5, <i>Pin Description</i> , and <i>Application Information</i> section	2–4

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