FAIRCHILD SEMICONDUCTOR®

August 2006

# FDS8670

## 30V N-Channel PowerTrench® MOSFET

### General Description

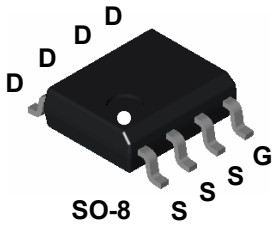
This device has been designed specifically to improve the efficiency of DC-DC converters. Using new techniques in MOSFET construction, the various components of gate charge and capacitance have been optimized to reduce switching losses. Low gate resistance and very low Miller charge enable excellent performance with both adaptive and fixed dead time gate drive circuits. Very low Rds(on) has been maintained to provide an extremely versatile device.

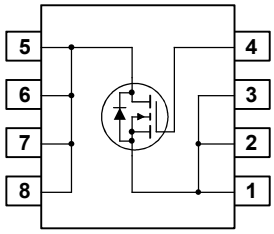
### Applications

- High Efficiency DC-DC Converters:
  - Notebook Vcore Power Supply
  - Telecom Brick Synchronous Rectifier
  - Multi purpose Point Of Load

### Features

- 21 A, 30 V  Max $R_{DS(ON)}$ = 3.7 mΩ @ $V_{GS}$ = 10 V
  Max $R_{DS(ON)}$ = 5.0 mΩ @ $V_{GS}$ = 4.5 V
- High performance trench technology for extremely low $R_{DS(ON)}$ and gate charge
- Minimal Qgd (5.5 nC typical)
- 100% $R_G$ tested (0.9 Ω typical)
- RoHS Compliant




## Absolute Maximum Ratings

$T_A$=25°C unless otherwise noted

| Symbol | Parameter | | Ratings | Units |
|---|---|---|---|---|
| $V_{DSS}$ | Drain-Source Voltage | | 30 | V |
| $V_{GSS}$ | Gate-Source Voltage | | ±20 | V |
| $I_D$ | Drain Current – Continuous | (Note 1a) | 21 | A |
| | – Pulsed | | 105 | |
| $P_D$ | Power Dissipation | (Note 1a) | 2.5 | W |
| | | (Note 1b) | 1.2 | |
| | | (Note 1c) | 1 | |
| $T_J$, $T_{STG}$ | Operating and Storage Junction Temperature Range | | –55 to +150 | °C |

## Thermal Characteristics

| | | | | |
|---|---|---|---|---|
| $R_{\theta JA}$ | Thermal Resistance, Junction-to-Ambient | (Note 1a) | 50 | °C/W |
| $R_{\theta JC}$ | Thermal Resistance, Junction-to-Case | (Note 1) | 25 | |

## Package Marking and Ordering Information

| Device Marking | Device | Reel Size | Tape width | Quantity |
|---|---|---|---|---|
| FDS8670 | FDS8670 | 13” | 12mm | 2500 units |

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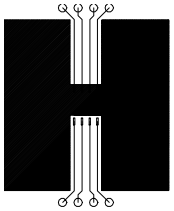
## Electrical Characteristics

$T_A$ = 25°C unless otherwise noted

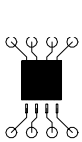
| Symbol | Parameter | Test Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **Off Characteristics** | | | | | | |
| $BV_{DSS}$ | Drain–Source Breakdown Voltage | $V_{GS}$ = 0 V, $I_D$ = 250 µA | 30 | | | V |
| $\frac{\Delta BV_{DSS}}{\Delta T_J}$ | Breakdown Voltage Temperature Coefficient | $I_D$ = 250 µA, Referenced to 25°C | | 39 | | mV/°C |
| $I_{DSS}$ | Zero Gate Voltage Drain Current | $V_{DS}$ = 24 V, $V_{GS}$ = 0 V | | | 1 | µA |
| $I_{GSS}$ | Gate–Body Leakage | $V_{GS}$ = ±20 V, $V_{DS}$ = 0 V | | | ±100 | nA |
| **On Characteristics** (Note 2) | | | | | | |
| $V_{GS(th)}$ | Gate Threshold Voltage | $V_{DS}$ = $V_{GS}$, $I_D$ = 250 µA | 1 | 1.4 | 3 | V |
| $\frac{\Delta V_{GS(th)}}{\Delta T_J}$ | Gate Threshold Voltage Temperature Coefficient | $I_D$ = 250 µA, Referenced to 25°C | | –5 | | mV/°C |
| $R_{DS(on)}$ | Static Drain–Source On–Resistance | $V_{GS}$ = 10 V, $I_D$ = 21 A<br>$V_{GS}$ = 4.5 V, $I_D$ = 18 A<br>$V_{GS}$=10 V, $I_D$ =21 A, $T_J$=125°C | | 3.3<br>4.2<br>4.4 | 3.7<br>5.0<br>5.5 | mΩ |
| $g_{FS}$ | Forward Transconductance | $V_{DS}$ = 10 V, $I_D$ = 21 A | | 118 | | S |
| **Dynamic Characteristics** | | | | | | |
| $C_{iss}$ | Input Capacitance | $V_{DS}$ = 15 V, $V_{GS}$ = 0 V, f = 1.0 MHz | | 4040 | | pF |
| $C_{oss}$ | Output Capacitance | | | 1730 | | pF |
| $C_{rss}$ | Reverse Transfer Capacitance | | | 160 | | pF |
| $R_G$ | Gate Resistance | f = 1.0 MHz | 0.2 | 0.9 | 1.5 | Ω |
| **Switching Characteristics** (Note 2) | | | | | | |
| $t_{d(on)}$ | Turn–On Delay Time | $V_{DD}$ = 15 V, $I_D$ = 1 A, $V_{GS}$ = 10 V, $R_{GEN}$ = 6 Ω | | 12 | 21 | ns |
| $t_r$ | Turn–On Rise Time | | | 11 | 20 | ns |
| $t_{d(off)}$ | Turn–Off Delay Time | | | 56 | 90 | ns |
| $t_f$ | Turn–Off Fall Time | | | 68 | 108 | ns |
| $Q_{g(TOT)}$ | Total Gate Charge at $V_{GS}$ = 10V | $V_{DD}$ = 15 V, $I_D$ = 21 A | | 58.5 | 82 | nC |
| $Q_{g(TOT)}$ | Total Gate Charge at $V_{GS}$ = 5V | | | 30 | 42 | nC |
| $Q_{gs}$ | Gate–Source Charge | | | 9.5 | | nC |
| $Q_{gd}$ | Gate–Drain Charge | | | 5.5 | | nC |
| **Drain–Source Diode Characteristics and Maximum Ratings** | | | | | | |
| $V_{SD}$ | Drain–Source Diode Forward Voltage | $V_{GS}$ = 0 V, $I_S$ = 2.1 A (Note 2) | | 0.7 | 1.2 | V |
| $t_{rr}$ | Diode Reverse Recovery Time | $I_F$ = 21 A, $dI_F/dt$ = 100 A/µs | | 51 | | ns |
| $I_{RM}$ | Diode Reverse Recovery Current | | | 1.5 | | A |
| $Q_{rr}$ | Diode Reverse Recovery Charge | | | 37 | | nC |

**Notes:**

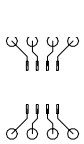
**1.** $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a) 50°/W when mounted on a 1 $in^2$ pad of 2 oz copper



b) 105°/W when mounted on a .04 $in^2$ pad of 2 oz copper



c) 125°/W when mounted on a minimum pad.

Scale 1 : 1 on letter size paper

**2.** Pulse Test: Pulse Width < 300µs, Duty Cycle < 2.0%

## Typical Characteristics

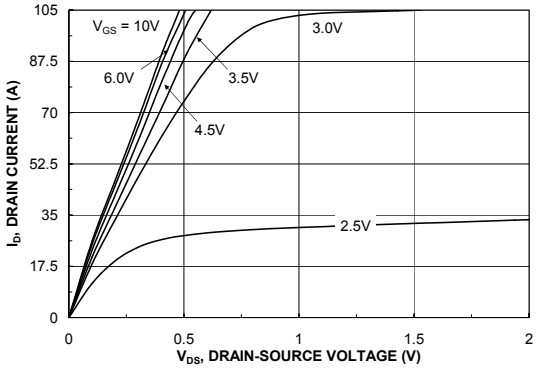



**Figure 1. On-Region Characteristics.**

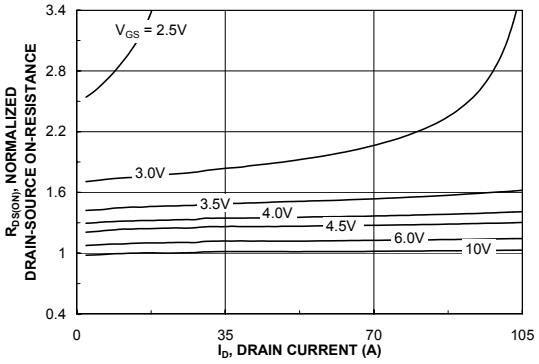



**Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.**

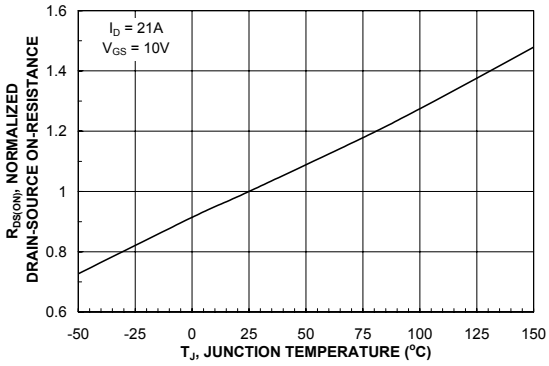



**Figure 3. On-Resistance Variation with Temperature.**

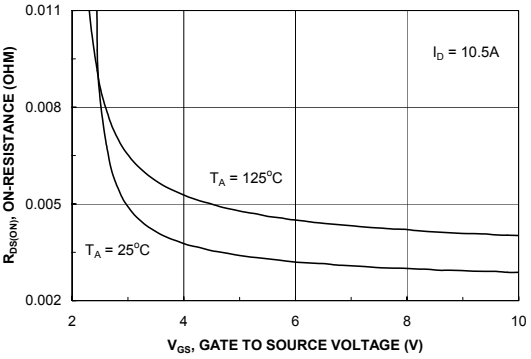



**Figure 4. On-Resistance Variation with Gate-to-Source Voltage.**

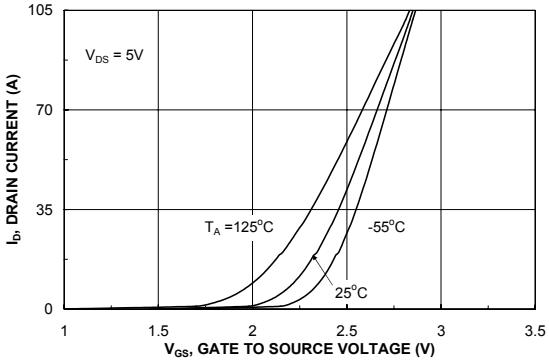



**Figure 5. Transfer Characteristics.**

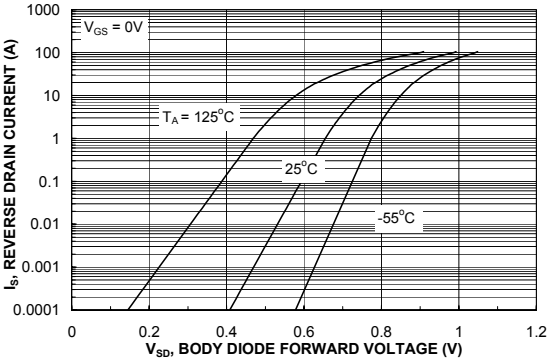



**Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.**

## Typical Characteristics (continued)

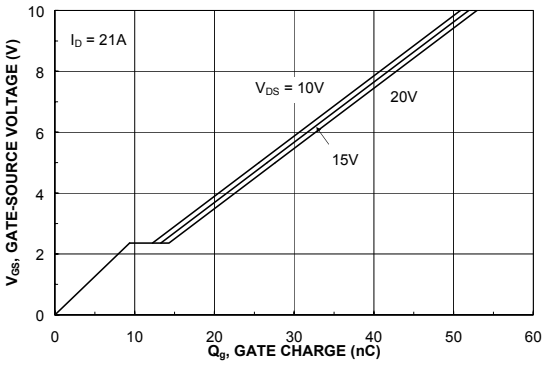



**Figure 7. Gate Charge Characteristics.**

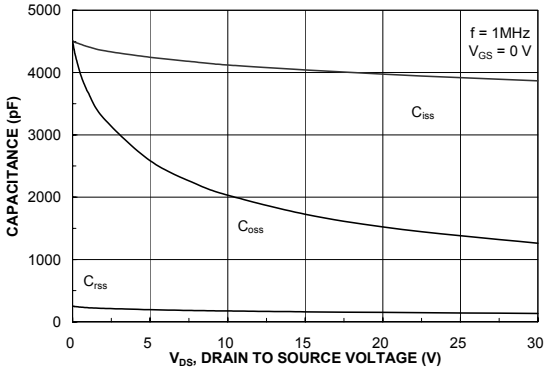



**Figure 8. Capacitance Characteristics.**

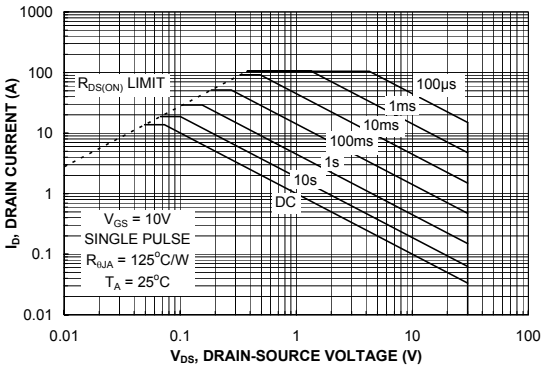



**Figure 9. Maximum Safe Operating Area.**

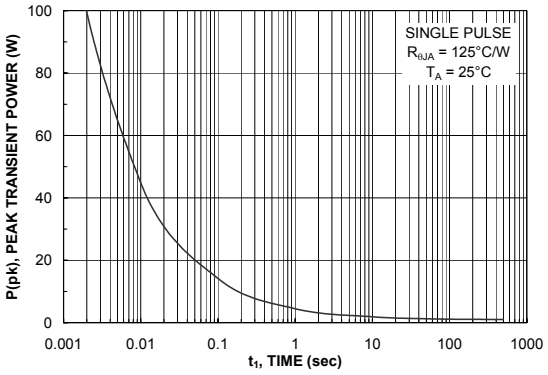



**Figure 10. Single Pulse Maximum Power Dissipation.**

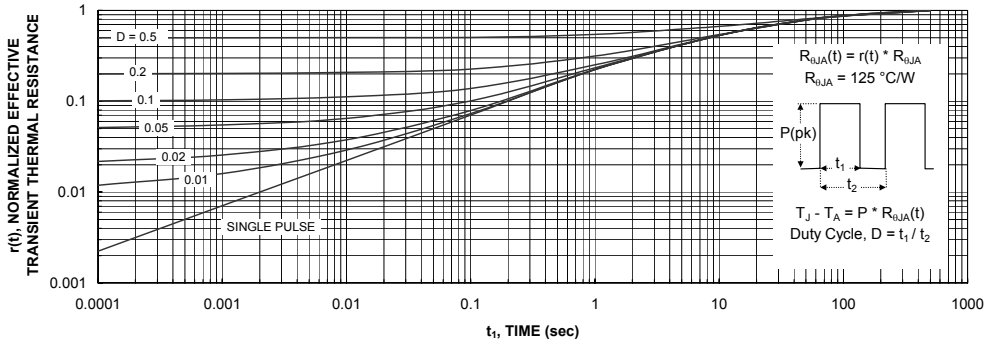



**Figure 11. Transient Thermal Response Curve.**

**Thermal characterization performed using the conditions described in Note 1c.**
**Transient thermal response will change depending on the circuit board design.**

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