



Preliminary 1.0

AS7C316096B

2048K X 8 BIT HIGH SPEED CMOS SRAM

REVISION HISTORY

<u>Revision</u>	<u>Description</u>	<u>Issue Date</u>
Rev. 1.0	Initial Issue	June.2014
Rev. 2.0	Typo error on page 1 - should be 44-pin 400 mil TSOP-II	Jan. 2017

AS7C316096B

2048K X 8 BIT HIGH SPEED CMOS SRAM

FEATURES

- Fast access time : 10ns
- **Low power consumption:**
Operating current : 70mA (TYP.)
Standby current : 4mA(TYP.)
- Single 3.3V power supply
- All inputs and outputs TTL compatible
- Fully static operation
- Tri-state output
- Data retention voltage : 1.5V (MIN.)
- **All parts are ROHS Compliant**
- Package : 44-pin 400 mil TSOP-II
48-ball 6mm x 8mm TFBGA

GENERAL DESCRIPTION

The AS7C316096B is a 16M-bit high speed CMOS static random access memory organized as 2048K words by 8 bits. It is fabricated using very high performance, high reliability CMOS technology. Its standby current is stable within the range of operating temperature.

The AS7C316096B operates from a single power supply of 3.3V and all inputs and outputs are fully TTL compatible

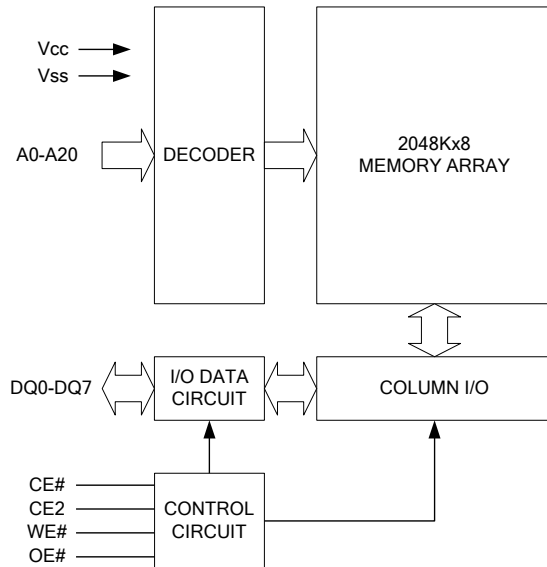
Table 1. Speed Grade Information

Product Family	V _{CC} Range	Speed	Power Dissipation	
			Standby(I _{SB1} , TYP.)	Operating(I _{CC} , TYP.)
AS7C316096B	2.7 ~ 3.6V	10ns	4mA	70mA

Table 2. Ordering Information

Product part No	Org	Temperature	Package
AS7C316096B-10TIN	2048K x 8	Industrial -40°C to 85°C	44-pin 400mil TSOP-II
AS7C316096B-10BIN	2048K x 8	Industrial -40°C to 85°C	48-ball 6mm x 8mm TFBGA

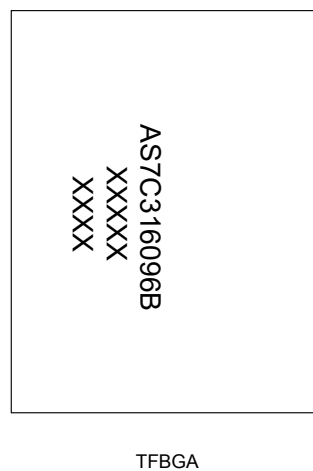
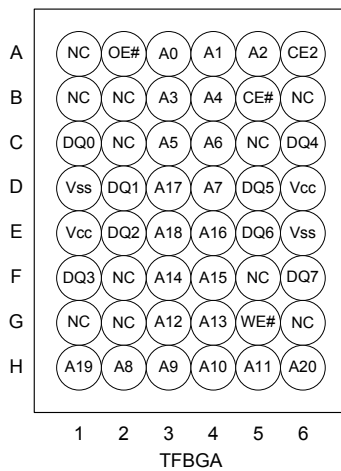
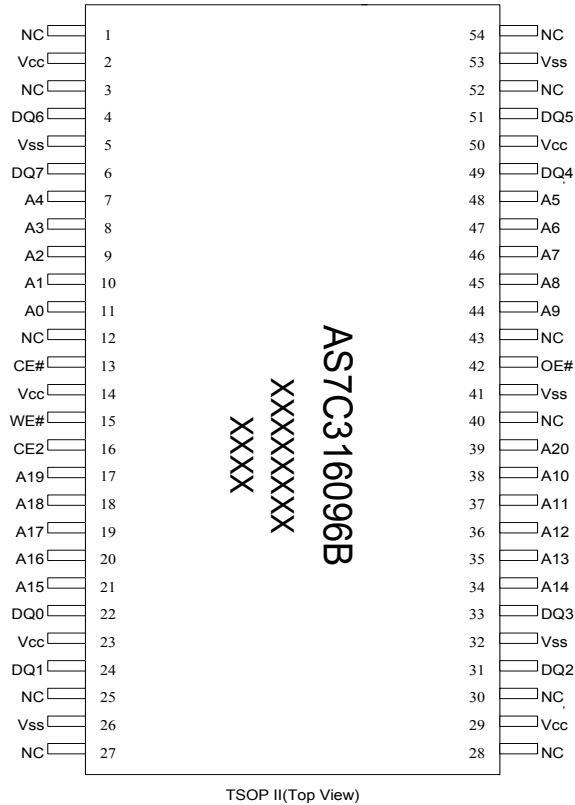
FUNCTIONAL BLOCK DIAGRAM



PIN DESCRIPTION

SYMBOL	DESCRIPTION
A0 – A20	Address Inputs
DQ0 – DQ7	Data Inputs/Outputs
CE#, CE2	Chip Enable Inputs
WE#	Write Enable Input
OE#	Output Enable Input
Vcc	Power Supply
Vss	Ground
NC	No Connection

PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS*

PARAMETER	SYMBOL	RATING	UNIT
Voltage on V_{CC} relative to V_{SS}	V_{T1}	-0.5 to 4.6	V
Voltage on any other pin relative to V_{SS}	V_{T2}	-0.5 to $V_{CC}+0.5$	V
Operating Temperature	T_A	-40 to 85(I grade)	°C
Storage Temperature	T_{STG}	-65 to 150	°C
Power Dissipation	P_D	1	W
DC Output Current	I_{OUT}	50	mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to the absolute maximum rating conditions for extended period may affect device reliability.

TRUTH TABLE

MODE	CE#	CE2	OE#	WE#	I/O OPERATION	SUPPLY CURRENT
Standby	H	X	X	X	High-Z	I_{SB1}
	X	L	X	X	High-Z	I_{SB1}
Output Disable	L	H	H	H	High-Z	I_{CC}
Read	L	H	L	H	D_{OUT}	I_{CC}
Write	L	H	X	L	D_{IN}	I_{CC}

Note: H = V_{IH} , L = V_{IL} , X = don't care.

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYM.	TEST CONDITION	MIN.	TYP. ⁴	MAX.	UNIT	
Supply Voltage	V _{CC}		2.7	3.3	3.6	V	
Input High Voltage	V _{IH} ¹		2.2	-	V _{CC} +0.3	V	
Input Low Voltage	V _{IL} ²		- 0.3	-	0.8	V	
Input Leakage Current	I _{LI}	V _{CC} ≥ V _{IN} ≥ V _{SS}	- 1	-	1	μA	
Output Leakage Current	I _{LO}	V _{CC} ≥ V _{OUT} ≥ V _{SS} , Output Disabled	- 1	-	1	μA	
Output High Voltage	V _{OH}	I _{OH} = -4mA	2.4	-	-	V	
Output Low Voltage	V _{OL}	I _{OL} = 8mA	-	-	0.4	V	
Average Operating Power supply Current	I _{CC}	CE# ≤0.2V and CE2≥ V _{CC} -0.2V, other pins at 0.2V or V _{CC} -0.2V, I _{I/O} = 0mA; f=max.	-10	-	70	120	mA
Standby Power Supply Current	I _{SB1}	CE# ≥ V _{CC} - 0.2V; Other pins at 0.2V or V _{CC} -0.2V.	-	4	40	mA	

Notes:

1. $V_{IH(MAX)} = V_{CC} + 2.0V$ for pulse width less than 6ns.

2. $V_{IL(MIN)} = V_{SS} - 2.0V$ for pulse width less than 6ns.

3. Over/Undershoot specifications are characterized on engineering evaluation stage, not for mass production test.

4. Typical values are included for reference only and are not guaranteed or tested.

Typical values are measured at $V_{CC} = V_{CC(TYP)}$ and $T_A = 25^\circ C$

CAPACITANCE ($T_A = 25^\circ\text{C}$, $f = 1.0\text{MHz}$)

PARAMETER	SYMBOL	MIN.	MAX	UNIT
Input Capacitance	C_{IN}	-	8	pF
Input/Output Capacitance	$C_{I/O}$	-	10	pF

Note : These parameters are guaranteed by device characterization, but not production tested.

AC TEST CONDITIONS

speed	10ns
Input Pulse Levels	0.2V to $V_{CC}-0.2V$
Input Rise and Fall Times	3ns
Input and Output Timing Reference Levels	$V_{CC}/2$
Output Load	$C_L = 30\text{pF} + 1\text{TTL}$, $I_{OH}/I_{OL} = -8\text{mA}/4\text{mA}$

AC ELECTRICAL CHARACTERISTICS

(1) READ CYCLE

PARAMETER	SYM.	AS7C316096B-10		UNIT
		MIN.	MAX.	
Read Cycle Time	t_{RC}	10	-	ns
Address Access Time	t_{AA}	-	10	ns
Chip Enable Access Time	t_{ACE}	-	10	ns
Output Enable Access Time	t_{OE}	-	4.5	ns
Chip Enable to Output in Low-Z	t_{CLZ}^*	2	-	ns
Output Enable to Output in Low-Z	t_{OLZ}^*	0	-	ns
Chip Disable to Output in High-Z	t_{CHZ}^*	-	4	ns
Output Disable to Output in High-Z	t_{OHZ}^*	-	4	ns
Output Hold from Address Change	t_{OH}	2	-	ns

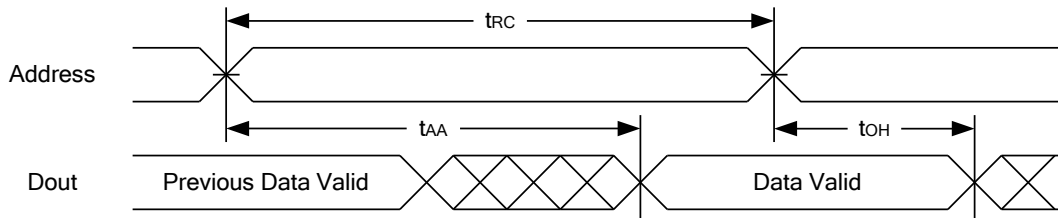
(2) WRITE CYCLE

PARAMETER	SYM.	AS7C316096B-10		UNIT
		MIN.	MAX.	
Write Cycle Time	t_{WC}	10	-	ns
Address Valid to End of Write	t_{AW}	8	-	ns
Chip Enable to End of Write	t_{CW}	8	-	ns
Address Set-up Time	t_{AS}	0	-	ns
Write Pulse Width	t_{WP}	8	-	ns
Write Recovery Time	t_{WR}	0	-	ns
Data to Write Time Overlap	t_{DW}	6	-	ns
Data Hold from End of Write Time	t_{DH}	0	-	ns
Output Active from End of Write	t_{OW}^*	2	-	ns
Write to Output in High-Z	t_{WHZ}^*	-	4	ns

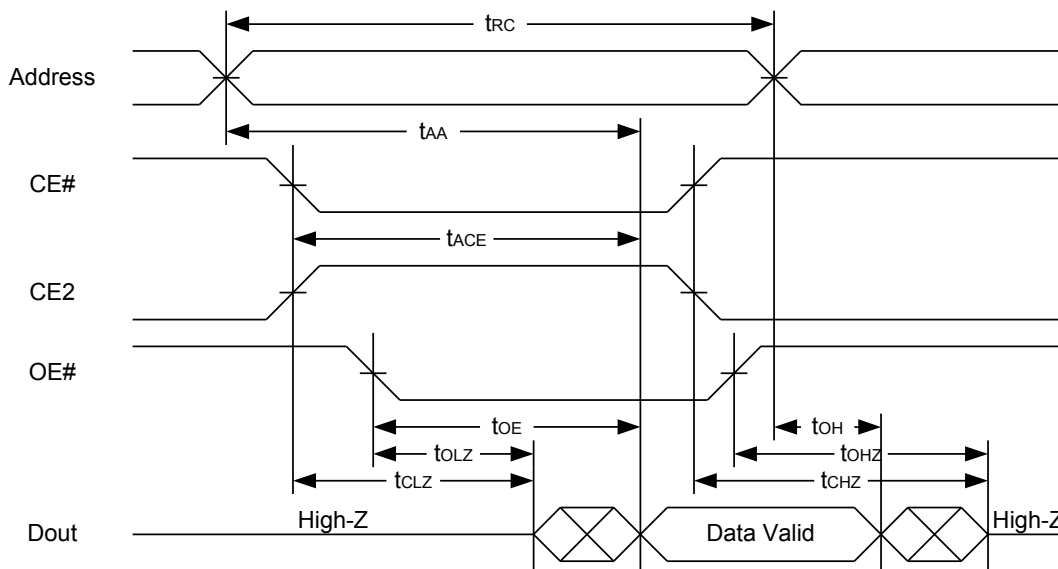
*These parameters are guaranteed by device characterization, but not production tested.

TIMING WAVEFORMS

READ CYCLE 1 (Address Controlled) (1,2)



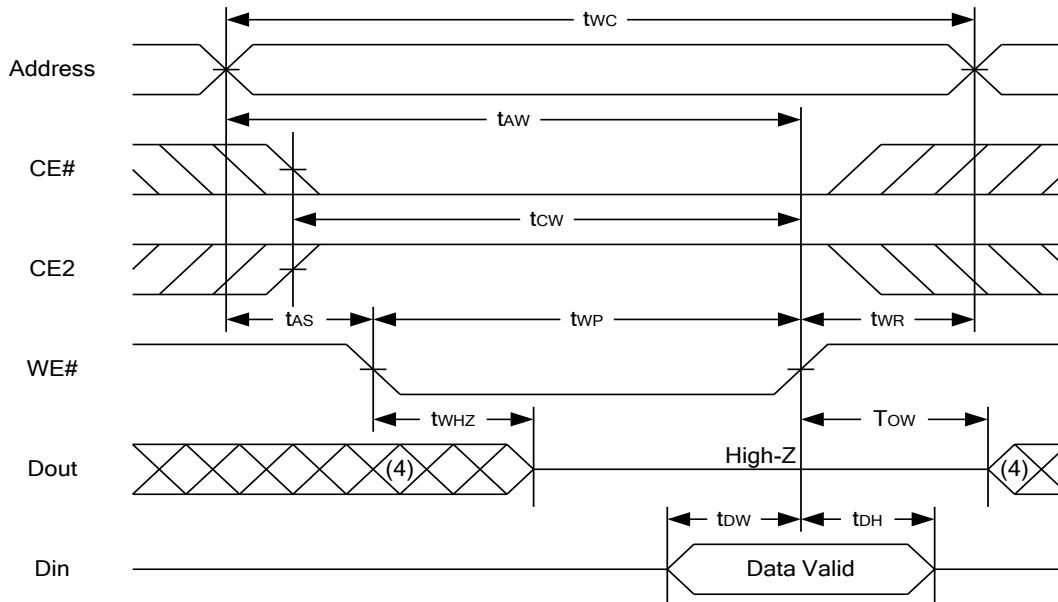
READ CYCLE 2 (CE# and CE2 and OE# Controlled) (1,3,4,5)



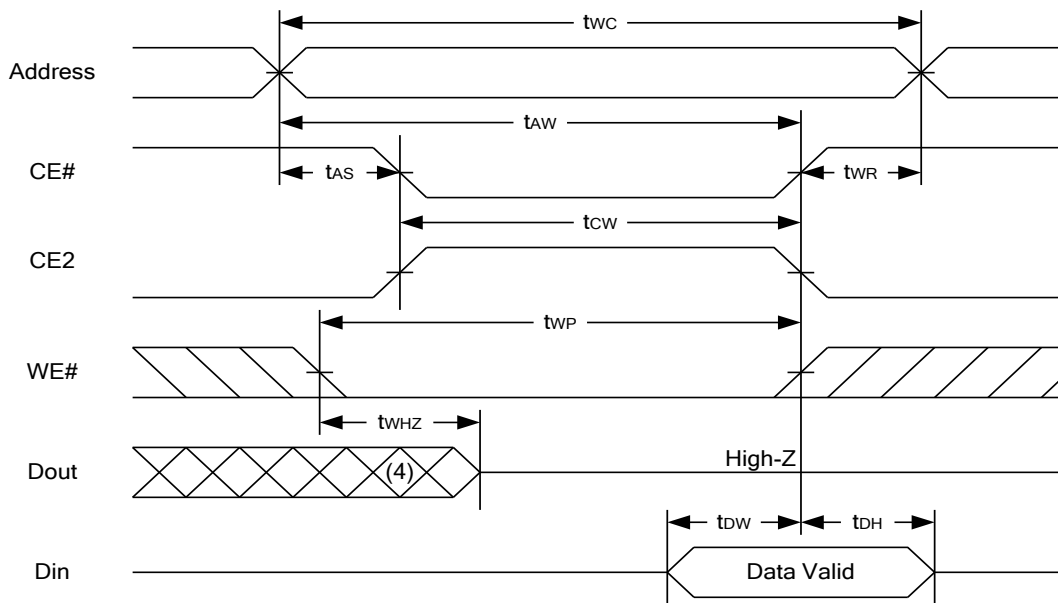
Notes :

1. WE# is high for read cycle.
2. Device is continuously selected OE# = low, CE# = low, CE2 = high.
3. Address must be valid prior to or coincident with CE# = low, CE2 = high; otherwise t_{AA} is the limiting parameter.
4. t_{CLZ} , t_{OLZ} , t_{CHZ} and t_{OHZ} are specified with $C_L = 5pF$. Transition is measured $\pm 500mV$ from steady state.
5. At any given temperature and voltage condition, t_{CHZ} is less than t_{CLZ} , t_{OHZ} is less than t_{OLZ} .

WRITE CYCLE 1 (WE# Controlled) (1,2,3,5,6)



WRITE CYCLE 2 (CE# and CE2 Controlled) (1,2,5,6)



Notes :

1. WE#, CE# must be high or CE2 must be low during all address transitions.
2. A write occurs during the overlap of a low CE#, high CE2, low WE#.
3. During a WE#-controlled write cycle with OE# low, t_{WP} must be greater than $t_{WHZ} + t_{DW}$ to allow the drivers to turn off and data to be placed on the bus.
4. During this period, I/O pins are in the output state, and input signals must not be applied.
5. If the CE# low transition and CE2 high transition occurs simultaneously with or after WE# low transition, the outputs remain in a high impedance state.
6. t_{OW} and t_{WHZ} are specified with $C_L = 5pF$. Transition is measured $\pm 500mV$ from steady state.

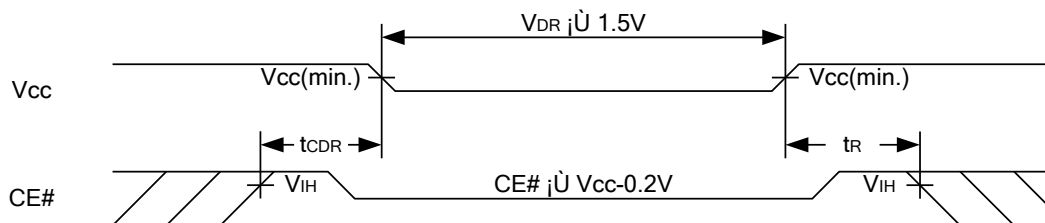
DATA RETENTION CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
V _{CC} for Data Retention	V _{DR}	CE# $\geq$ V _{CC} - 0.2V or CE2 $\leq$ 0.2V	1.5	-	3.6	V
Data Retention Current	I _{DR}	V _{CC} = 1.5V CE# $\geq$ V _{CC} - 0.2V or CE2 $\leq$ 0.2V Other pins at 0.2V or V _{CC} -0.2V	-	4	40	mA
Chip Disable to Data Retention Time	t _{CDR}	See Data Retention Waveforms (below)	0	-	-	ns
Recovery Time	t _R		t _{RC} *	-	-	ns

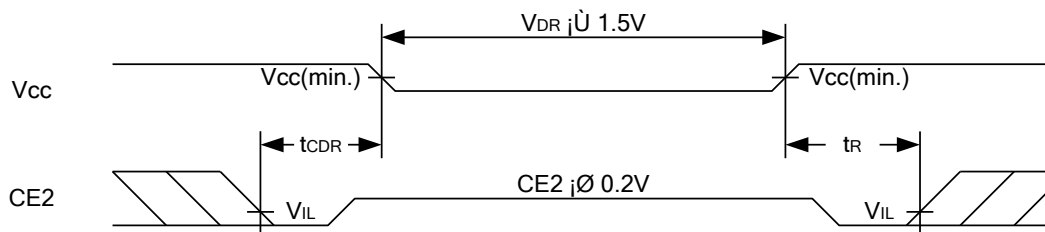
t_{RC}* = Read Cycle Time

DATA RETENTION WAVEFORM

Low V_{CC} Data Retention Waveform (1) (CE# controlled)

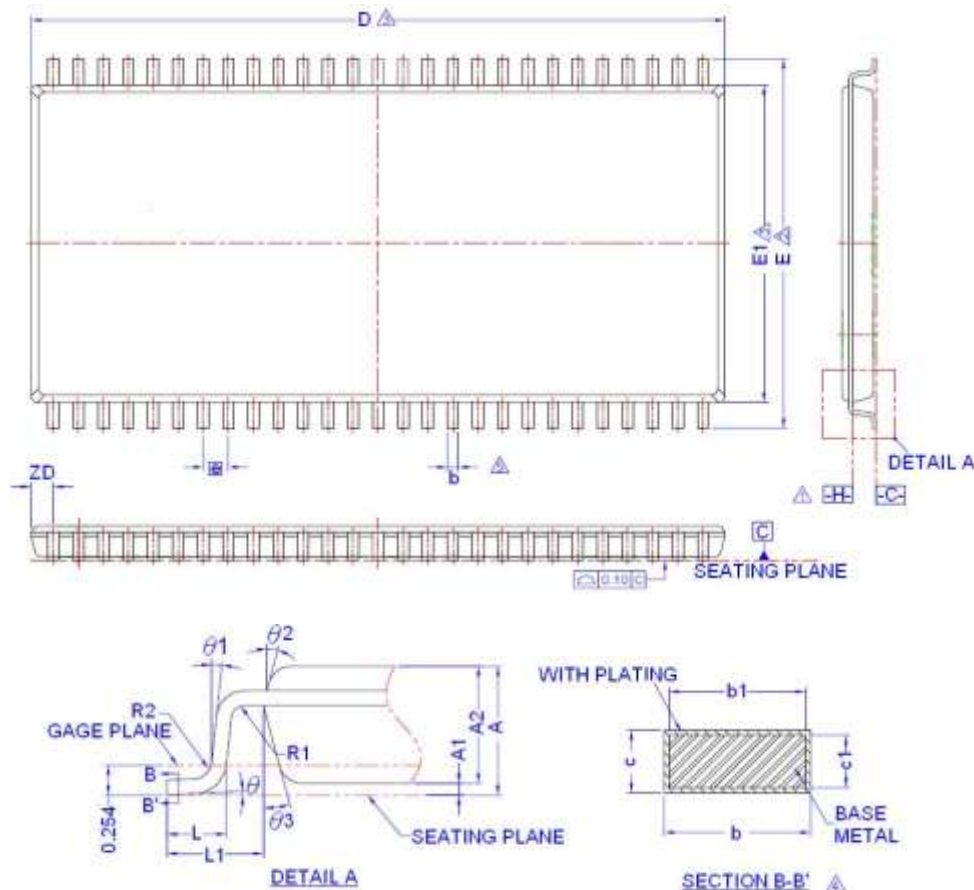


Low V_{CC} Data Retention Waveform (2) (CE2 controlled)



PACKAGE OUTLINE DIMENSION

54-pin 400 mil TSOP-II Package Outline Dimension

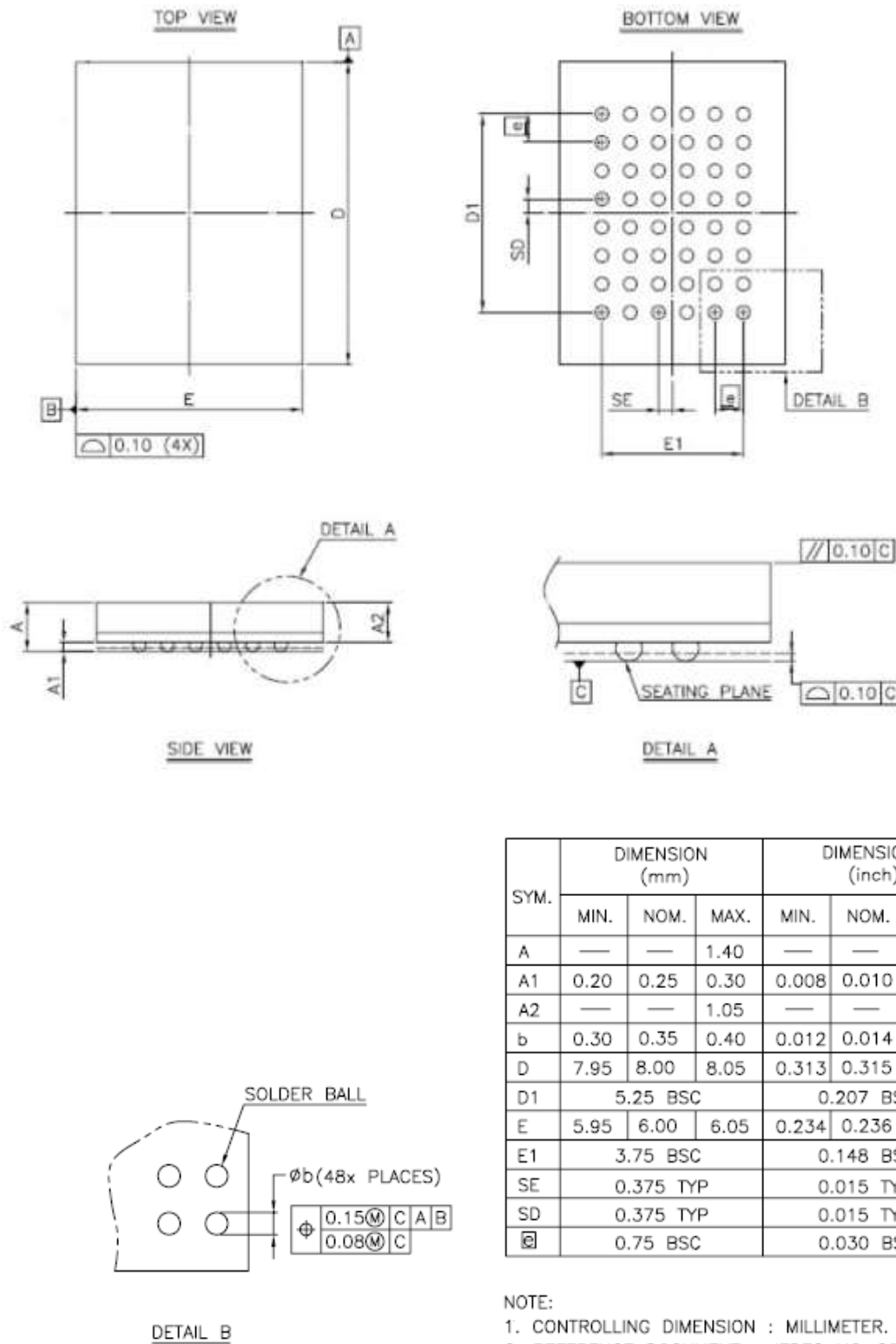


SYM.	DIMENSION (MM)			DIMENSION (INCH)		
	MIN	NOM	MAX	MIN	NOM	MAX
A	—	—	1.20	—	—	0.047
A1	0.05	0.10	0.15	0.002	0.004	0.006
A2	0.95	1.00	1.05	0.037	0.039	0.041
b	0.30	—	0.45	0.012	—	0.018
b1	0.30	0.35	0.40	0.012	0.014	0.016
c	0.12	—	0.21	0.005	—	0.008
c1	0.10	0.127	0.16	0.004	0.005	0.006
D	22.22 BSC			0.875 BSC		
ZD	0.71 REF			0.028 REF		
E	11.76 BSC			0.463 BSC		
E1	10.16 BSC			0.400 BSC		
L	0.40	0.50	0.60	0.016	0.020	0.024
L1	0.80 REF			0.031 REF		
[E]	0.80 BSC			0.031 BSC		
R1	0.12	—	—	0.005	—	—
R2	0.12	—	0.25	0.005	—	0.010
θ	0°	—	8°	0°	—	8°
θ1	0°	—	—	0°	—	—
θ2	10°	15°	20°	10°	15°	20°
θ3	10°	15°	20°	10°	15°	20°

NOTE:

1. DATUM PLANE [H] COINCIDENT WITH BOTTOM OF LEAD, WHERE LEAD EXITS BODY.
2. TO BE DETERMINED AT SEATING PLANE [C].
3. DIMENSION D AND E1 ARE DETERMINED AT DATUM [H].
DIMENSION D DOES NOT INCLUDE MOLD PROTRUSIONS OR GATE BURRS. MOLD PROTRUSIONS AND GATE BURRS SHALL NOT EXCEED 0.15mm PER SIDE.
DIMENSION E1 DOES NOT INCLUDE INTERLEAD MOLD PROTRUSIONS. INTERLEAD MOLD PROTRUSIONS SHALL NOT EXCEED 0.25mm PER SIDE.
4. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.
5. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION/INTRUSION.
6. CONTROLLING DIMENSION: MILLIMETER.
7. REFER TO JEDEC STD MS-024, FA.

48-ball 6mm × 8mm TFBGA Package Outline Dimension



NOTE:

1. CONTROLLING DIMENSION : MILLIMETER.
2. REFERENCE DOCUMENT : JEDEC MO-207.



Preliminary 1.0

AS7C316096B

2048K X 8 BIT HIGH SPEED CMOS SRAM

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