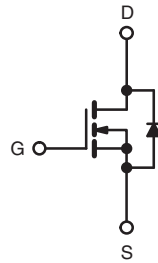
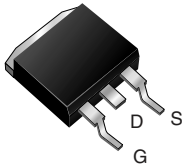


Power MOSFET

PRODUCT SUMMARY

V_{DS} (V)	250	
$R_{DS(on)}$ (Ω)	$V_{GS} = 10$ V	0.28
Q_g (Max.) (nC)	68	
Q_{gs} (nC)	11	
Q_{gd} (nC)	35	
Configuration	Single	

D²PAK (TO-263)


N-Channel MOSFET

FEATURES

- Halogen-free According to IEC 61249-2-21 Definition
- Surface Mount
- Available in Tape and Reel
- Dynamic dV/dt Rating
- Repetitive Avalanche Rated
- Fast Switching
- Ease of Paralleling
- Simple Drive Requirements
- Compliant to RoHS Directive 2002/95/EC



RoHS*
COMPLIANT
HALOGEN
FREE
Available

DESCRIPTION

Third generation Power MOSFETs from Vishay provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The D²PAK is a surface mount power package capable of accommodating die size up to HEX-4. It provides the highest power capability and the lowest possible on-resistance in any existing surface mount package. The D²PAK is suitable for high current applications because of its low internal connection resistance and can dissipate up to 2.0 W in a typical surface mount application.

ORDERING INFORMATION

Package	D ² PAK (TO-263)	D ² PAK (TO-263)	D ² PAK (TO-263)
Lead (Pb)-free and Halogen-free	SiHF644S-GE3	SiHF644STRL-GE3 ^a	SiHF644STRR-GE3 ^a
Lead (Pb)-free	IRF644SPbF	IRF644STRLPbF ^a	IRF644STRRPbF ^a
	SiHF644S-E3	SiHF644STL-E3 ^a	SiHF644STR-E3 ^a

Note

- a. See device orientation.

ABSOLUTE MAXIMUM RATINGS ($T_C = 25$ °C, unless otherwise noted)

PARAMETER	SYMBOL	LIMIT	UNIT	
Drain-Source Voltage	V_{DS}	250	V	
Gate-Source Voltage	V_{GS}	± 20		
Continuous Drain Current	V_{GS} at 10 V	$T_C = 25$ °C	14	A
		$T_C = 100$ °C	8.5	
Pulsed Drain Current ^a	I_{DM}	56	W/°C	
Linear Derating Factor		1.0		
Linear Derating Factor (PCB Mount) ^e		0.025		
Single Pulse Avalanche Energy ^b	E_{AS}	550	mJ	
Avalanche Current ^a	I_{AR}	14	A	
Repetitive Avalanche Energy ^a	E_{AR}	13	mJ	
Maximum Power Dissipation	P_D	$T_C = 25$ °C	125	W
		$T_A = 25$ °C	3.1	
Peak Diode Recovery dV/dt ^c	dV/dt	4.8	V/ns	
Operating Junction and Storage Temperature Range	T_J, T_{stg}	- 55 to + 150	°C	
Soldering Recommendations (Peak Temperature)	for 10 s	300 ^d		

Notes

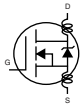

- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- $V_{DD} = 50$ V, starting $T_J = 25$ °C, $L = 4.5$ mH, $R_g = 25$ Ω , $I_{AS} = 14$ A (see fig. 12).
- $I_{SD} \leq 14$ A, $dI/dt \leq 150$ A/ μ s, $V_{DD} \leq V_{DS}$, $T_J \leq 150$ °C.
- 1.6 mm from case.
- When mounted on 1" square PCB (FR-4 or G-10 material).

* Pb containing terminations are not RoHS compliant, exemptions may apply

THERMAL RESISTANCE RATINGS				
PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient	R_{thJA}	-	62	°C/W
Maximum Junction-to-Ambient (PCB Mount) ^a	R_{thJA}	-	40	
Maximum Junction-to-Case (Drain)	R_{thJC}	-	1.0	

Note

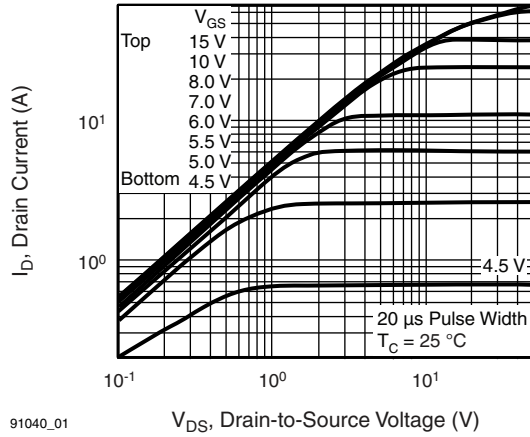
a. When mounted on 1" square PCB (FR-4 or G-10 material).

SPECIFICATIONS ($T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted)							
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0, I_D = 250\text{ }\mu\text{A}$		250	-	-	V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	Reference to $25\text{ }^\circ\text{C}$, $I_D = 1\text{ mA}$		-	0.34	-	V/°C
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$		2.0	-	4.0	V
Gate-Source Leakage	I_{GSS}	$V_{GS} = \pm 20\text{ V}$		-	-	± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 250\text{ V}, V_{GS} = 0\text{ V}$		-	-	25	μA
		$V_{DS} = 200\text{ V}, V_{GS} = 0\text{ V}, T_J = 125\text{ }^\circ\text{C}$		-	-	250	
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}$	$I_D = 8.4\text{ A}^b$	-	-	0.28	Ω
Forward Transconductance	g_{fs}	$V_{DS} = 50\text{ V}, I_D = 8.4\text{ A}^b$		6.7	-	-	S
Dynamic							
Input Capacitance	C_{iss}	$V_{GS} = 0\text{ V}, V_{DS} = 25\text{ V}, f = 1.0\text{ MHz}$, see fig. 5		-	1300	-	pF
Output Capacitance	C_{oss}			-	330	-	
Reverse Transfer Capacitance	C_{rss}			-	85	-	
Total Gate Charge	Q_g	$V_{GS} = 10\text{ V}$	$I_D = 7.9\text{ A}, V_{DS} = 200\text{ V}$, see fig. 6 and 13 ^b	-	-	68	nC
Gate-Source Charge	Q_{gs}			-	-	11	
Gate-Drain Charge	Q_{gd}			-	-	35	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 125\text{ V}, I_D = 7.9\text{ A}, R_g = 9.1\text{ }\Omega, R_D = 8.7\text{ }\Omega$, see fig. 10 ^b		-	11	-	ns
Rise Time	t_r			-	24	-	
Turn-Off Delay Time	$t_{d(off)}$			-	53	-	
Fall Time	t_f			-	49	-	
Internal Drain Inductance	L_D	Between lead, 6 mm (0.25") from package and center of die contact 		-	4.5	-	nH
Internal Source Inductance	L_S			-	7.5	-	
Drain-Source Body Diode Characteristics							
Continuous Source-Drain Diode Current	I_S	MOSFET symbol showing the integral reverse p - n junction diode 		-	-	14	A
Pulsed Diode Forward Current ^a	I_{SM}			-	-	56	
Body Diode Voltage	V_{SD}	$T_J = 25\text{ }^\circ\text{C}, I_S = 14\text{ A}, V_{GS} = 0\text{ V}^b$		-	-	1.8	V
Body Diode Reverse Recovery Time	t_{rr}	$T_J = 25\text{ }^\circ\text{C}, I_F = 7.9\text{ A}, dI/dt = 100\text{ A}/\mu\text{s}^b$		-	250	500	ns
Body Diode Reverse Recovery Charge	Q_{rr}			-	2.3	4.6	μC
Forward Turn-On Time	t_{on}	Intrinsic turn-on time is negligible (turn-on is dominated by L_S and L_D)					

Notes

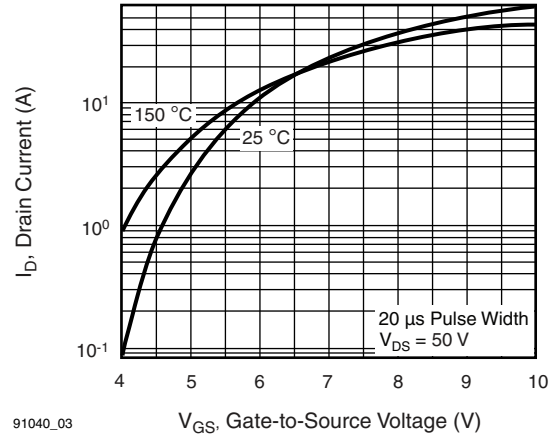
- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- Pulse width $\leq 300\text{ }\mu\text{s}$; duty cycle $\leq 2\%$.

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



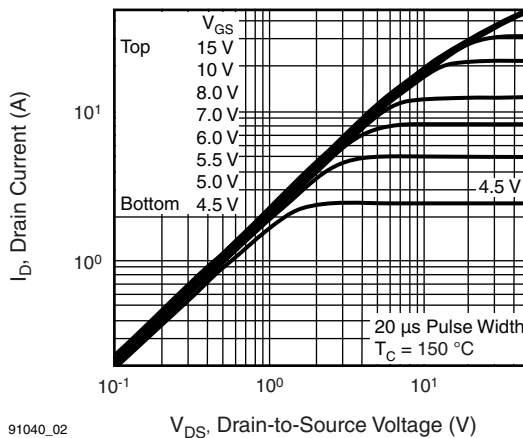
91040_01

Fig. 1 - Typical Output Characteristics, $T_C = 25\text{ }^\circ\text{C}$



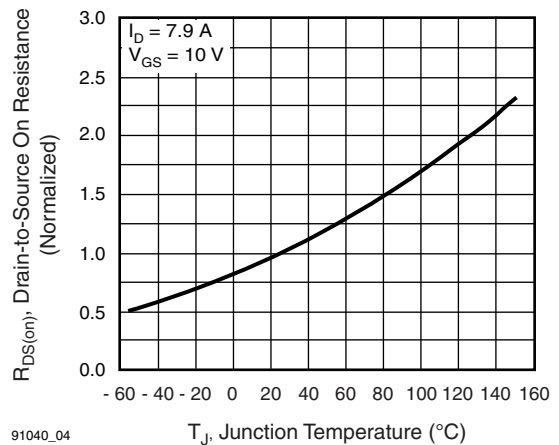
91040_03

Fig. 3 - Typical Transfer Characteristics



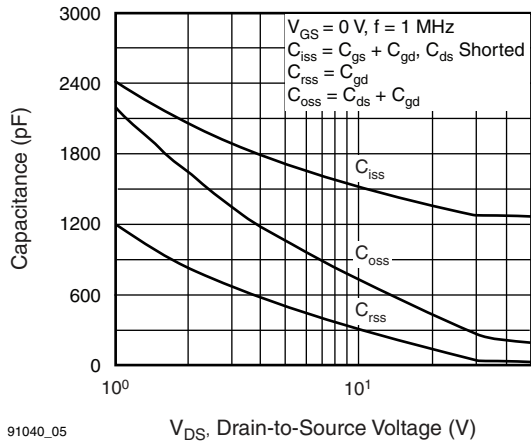
91040_02

Fig. 2 - Typical Output Characteristics, $T_C = 150\text{ }^\circ\text{C}$



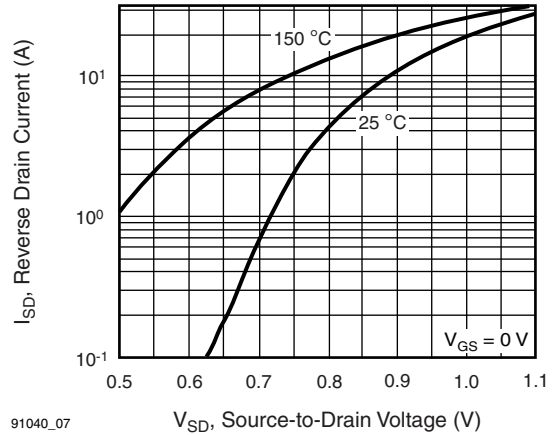
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Fig. 4 - Normalized On-Resistance vs. Temperature



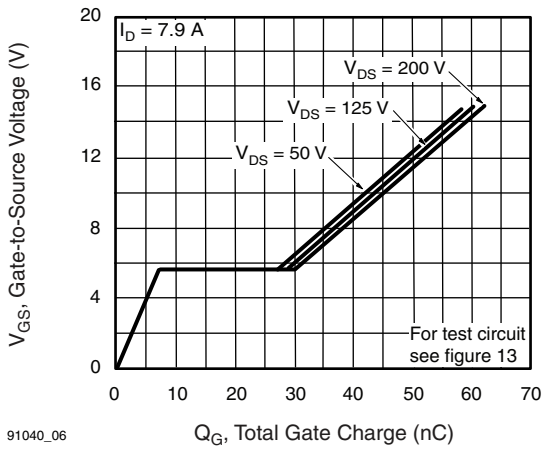
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Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage



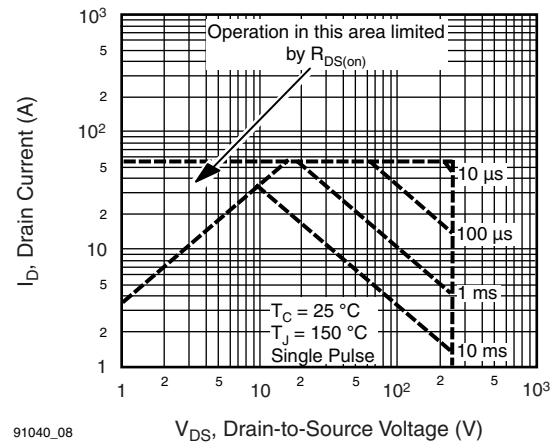
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Fig. 7 - Typical Source-Drain Diode Forward Voltage



91040_06

Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage



91040_08

Fig. 8 - Maximum Safe Operating Area

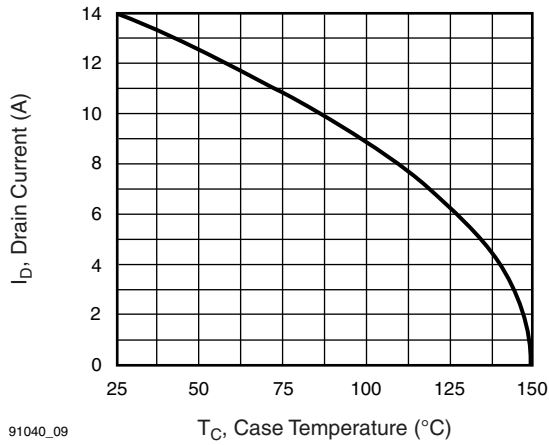


Fig. 9 - Maximum Drain Current vs. Case Temperature

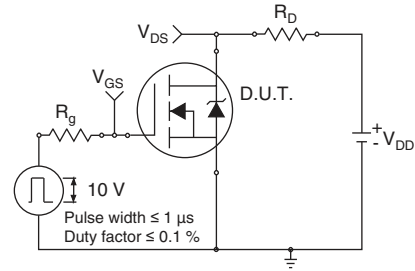


Fig. 10a - Switching Time Test Circuit

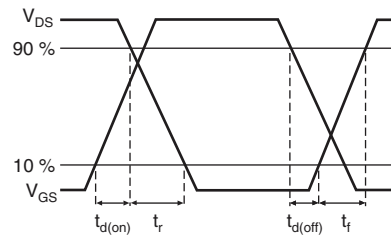


Fig. 10b - Switching Time Waveforms

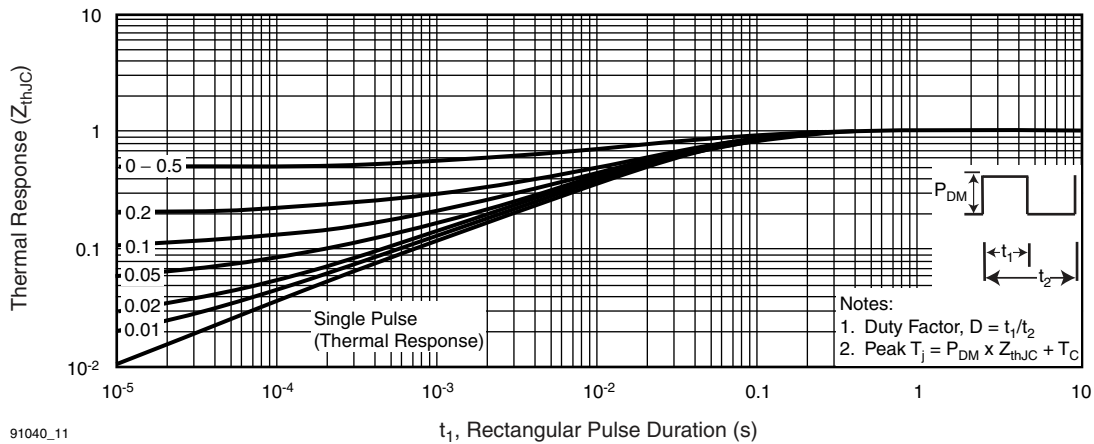


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

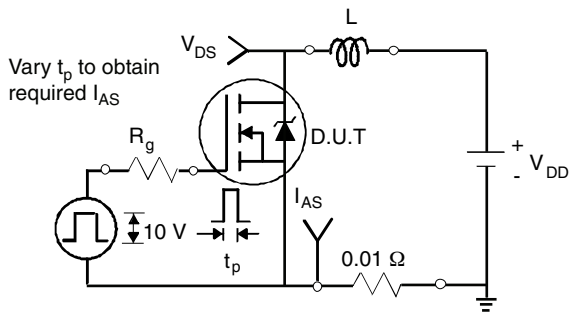


Fig. 12a - Unclamped Inductive Test Circuit

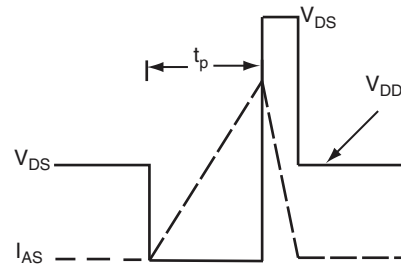
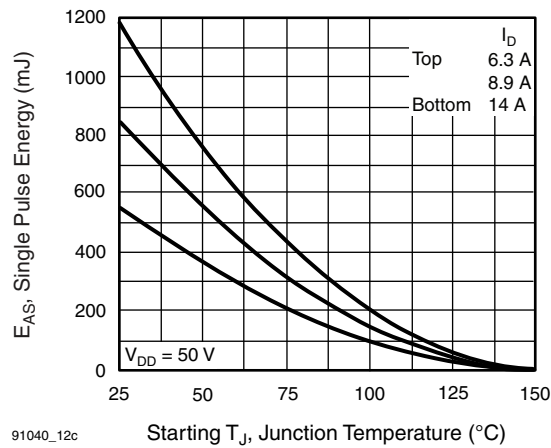


Fig. 12b - Unclamped Inductive Waveforms



91040_12c

Fig. 13 - Maximum Avalanche Energy vs. Drain Current

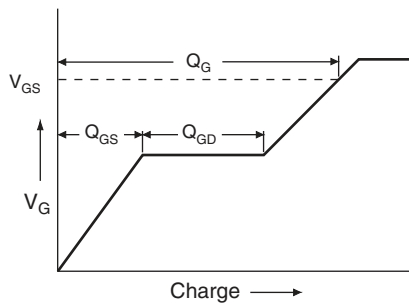


Fig. 13a - Basic Gate Charge Waveform

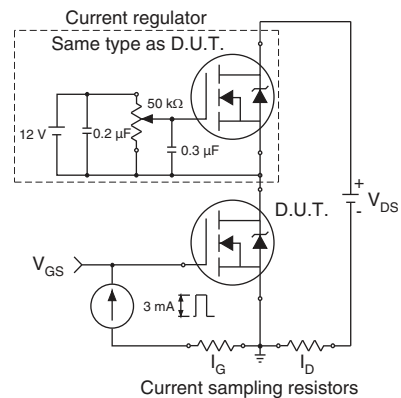
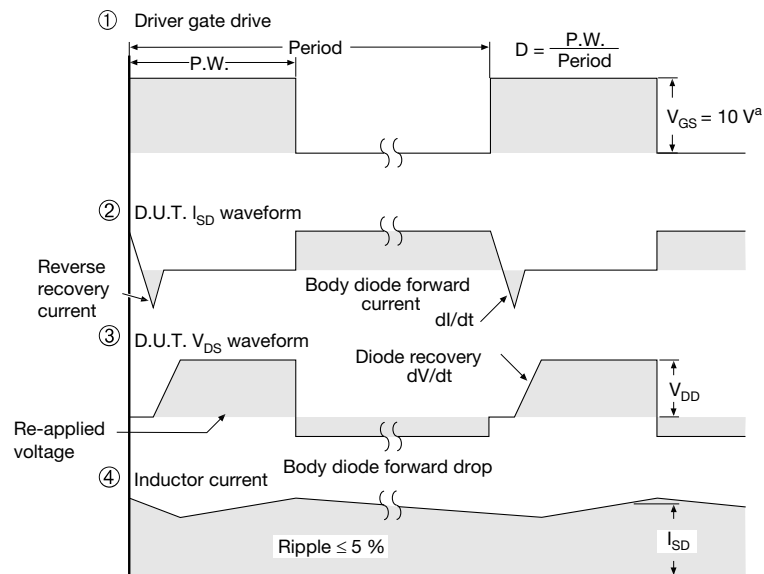
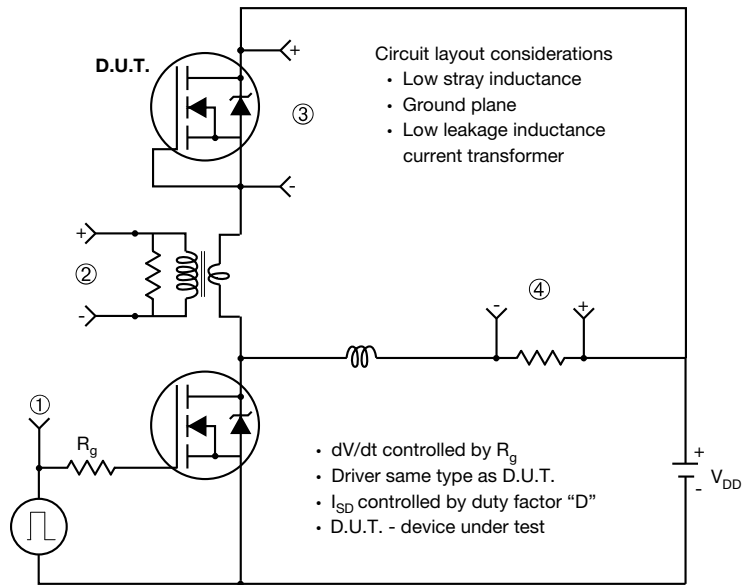


Fig. 13b - Gate Charge Test Circuit

Peak Diode Recovery dV/dt Test Circuit



Note
a. $V_{GS} = 5\text{ V}$ for logic level devices

Fig. 14 - For N-Channel

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?91040.

TO-263AB (HIGH VOLTAGE)



DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	4.06	4.83	0.160	0.190
A1	0.00	0.25	0.000	0.010
b	0.51	0.99	0.020	0.039
b1	0.51	0.89	0.020	0.035
b2	1.14	1.78	0.045	0.070
b3	1.14	1.73	0.045	0.068
c	0.38	0.74	0.015	0.029
c1	0.38	0.58	0.015	0.023
c2	1.14	1.65	0.045	0.065
D	8.38	9.65	0.330	0.380

DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
D1	6.86	-	0.270	-
E	9.65	10.67	0.380	0.420
E1	6.22	-	0.245	-
e	2.54 BSC		0.100 BSC	
H	14.61	15.88	0.575	0.625
L	1.78	2.79	0.070	0.110
L1	-	1.65	-	0.066
L2	-	1.78	-	0.070
L3	0.25 BSC		0.010 BSC	
L4	4.78	5.28	0.188	0.208

ECN: S-82110-Rev. A, 15-Sep-08
DWG: 5970

Notes

1. Dimensioning and tolerancing per ASME Y14.5M-1994.
2. Dimensions are shown in millimeters (inches).
3. Dimension D and E do not include mold flash. Mold flash shall not exceed 0.127 mm (0.005") per side. These dimensions are measured at the outmost extremes of the plastic body at datum A.
4. Thermal PAD contour optional within dimension E, L1, D1 and E1.
5. Dimension b1 and c1 apply to base metal only.
6. Datum A and B to be determined at datum plane H.
7. Outline conforms to JEDEC outline to TO-263AB.

RECOMMENDED MINIMUM PADS FOR D²PAK: 3-Lead



Recommended Minimum Pads
Dimensions in Inches/(mm)

[Return to Index](#)



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Please note that some Vishay documentation may still make reference to RoHS Directive 2002/95/EC. We confirm that all the products identified as being compliant to Directive 2002/95/EC conform to Directive 2011/65/EU.

Vishay Intertechnology, Inc. hereby certifies that all its products that are identified as Halogen-Free follow Halogen-Free requirements as per JEDEC JS709A standards. Please note that some Vishay documentation may still make reference to the IEC 61249-2-21 definition. We confirm that all the products identified as being compliant to IEC 61249-2-21 conform to JEDEC JS709A standards.

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<http://moschip.ru/get-element>

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