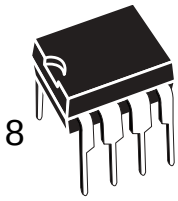
M24C16, M24C08
M24C04, M24C02, M24C01

16Kbit, 8Kbit, 4Kbit, 2Kbit and 1Kbit Serial I²C Bus EEPROM

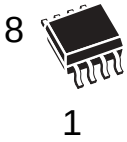
FEATURES SUMMARY

- Two Wire I²C Serial Interface
  Supports 400kHz Protocol
- Single Supply Voltage:
  - 4.5 to 5.5V for M24Cxx
  - 2.5 to 5.5V for M24Cxx-W
  - 1.8 to 5.5V for M24Cxx-R
- Write Control Input
- BYTE and PAGE WRITE (up to 16 Bytes)
- RANDOM and SEQUENTIAL READ Modes
- Self-Timed Programming Cycle
- Automatic Address Incrementing
- Enhanced ESD/Latch-Up Behavior
- More than 1 Million Erase/Write Cycles
- More than 40 Year Data Retention

Figure 1. Packages



PDIP8 (BN)



SO8 (MN)
150 mil width

TSSOP8 (DW)
169 mil width

TSSOP8 (DS)
3x3mm² body size (MSOP)

UFDFPN8 (MB)
2x3mm² (MLP)

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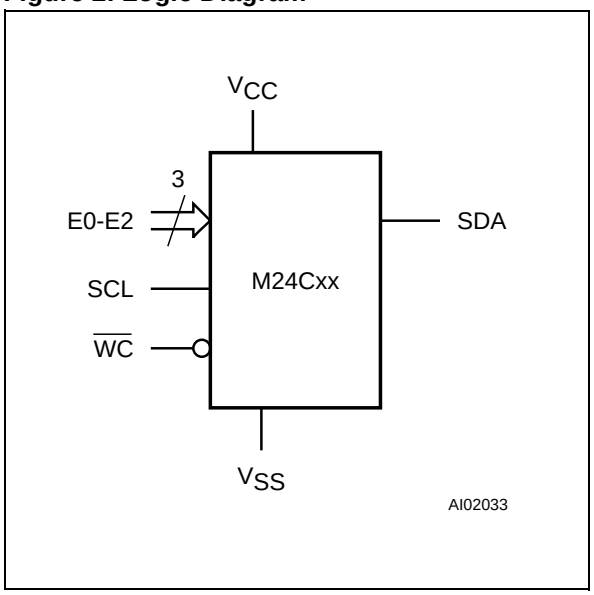
SUMMARY DESCRIPTION

These I^2C-compatible electrically erasable programmable memory (EEPROM) devices are organized as 2048/1024/512/256/128 x 8 (M24C16, M24C08, M24C04, M24C02, M24C01).

Figure 2. Logic Diagram



I^2C uses a two wire serial interface, comprising a bi-directional data line and a clock line. The devices carry a built-in 4-bit Device Type Identifier code (1010) in accordance with the I^2C bus definition.

The device behaves as a slave in the I^2C protocol, with all memory operations synchronized by the serial clock. Read and Write operations are initiated by a Start condition, generated by the bus master. The Start condition is followed by a Device Select Code and $R\overline{W}$ bit (as described in Table 2.), terminated by an acknowledge bit.

When writing data to the memory, the device inserts an acknowledge bit during the 9th bit time, following the bus master's 8-bit transmission. When data is read by the bus master, the bus master acknowledges the receipt of the data byte in the same way. Data transfers are terminated by a Stop condition after an Ack for Write, and after a NoAck for Read.

Table 1. Signal Names

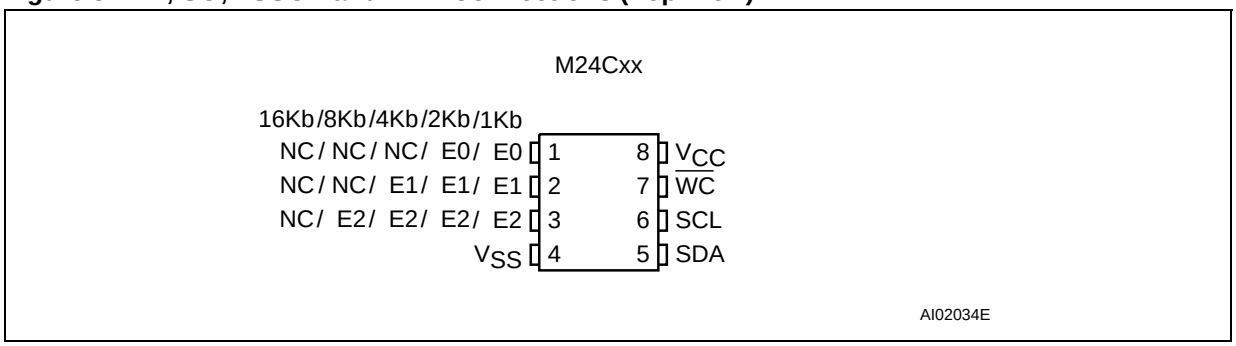
E0, E1, E2	Chip Enable
SDA	Serial Data
SCL	Serial Clock
$\overline{WC}$	Write Control
V_{CC}	Supply Voltage
V_{SS}	Ground

Power On Reset: V_{CC} Lock-Out Write Protect

In order to prevent data corruption and inadvertent Write operations during Power-up, a Power On Reset (POR) circuit is included. At Power-up, the internal reset is held active until V_{CC} has reached the POR threshold value, and all operations are disabled – the device will not respond to any command. In the same way, when V_{CC} drops from the operating voltage, below the POR threshold value, all operations are disabled and the device will not respond to any command.

A stable and valid V_{CC} (as defined in Table 6. and Table 7.) must be applied before applying any logic signal.

Figure 3. DIP, SO, TSSOP and MLP Connections (Top View)



Note: 1. NC = Not Connected
2. See PACKAGE MECHANICAL section for package dimensions, and how to identify pin-1.

SIGNAL DESCRIPTION

Serial Clock (SCL). This input signal is used to strobe all data in and out of the device. In applications where this signal is used by slave devices to synchronize the bus to a slower clock, the bus master must have an open drain output, and a pull-up resistor can be connected from Serial Clock (SCL) to V_{CC}. (Figure 4. indicates how the value of the pull-up resistor can be calculated). In most applications, though, this method of synchronization is not employed, and so the pull-up resistor is not necessary, provided that the bus master has a push-pull (rather than open drain) output.

Serial Data (SDA). This bi-directional signal is used to transfer data in or out of the device. It is an open drain output that may be wire-OR'ed with other open drain or open collector signals on the bus. A pull up resistor must be connected from Serial Data (SDA) to V_{CC}. (Figure 4. indicates how the value of the pull-up resistor can be calculated).

Chip Enable (E0, E1, E2). These input signals are used to set the value that is to be looked for on the three least significant bits (b3, b2, b1) of the 7-bit Device Select Code. These inputs must be tied to V_{CC} or V_{SS}, to establish the Device Select Code.

Write Control ($\overline{WC}$). This input signal is useful for protecting the entire contents of the memory from inadvertent write operations. Write operations are disabled to the entire memory array when Write Control ($\overline{WC}$) is driven High. When unconnected, the signal is internally read as V_{IL}, and Write operations are allowed.

When Write Control ($\overline{WC}$) is driven High, Device Select and Address bytes are acknowledged, Data bytes are not acknowledged.

Figure 4. Maximum R_L Value versus Bus Capacitance (C_{BUS}) for an I^2C Bus

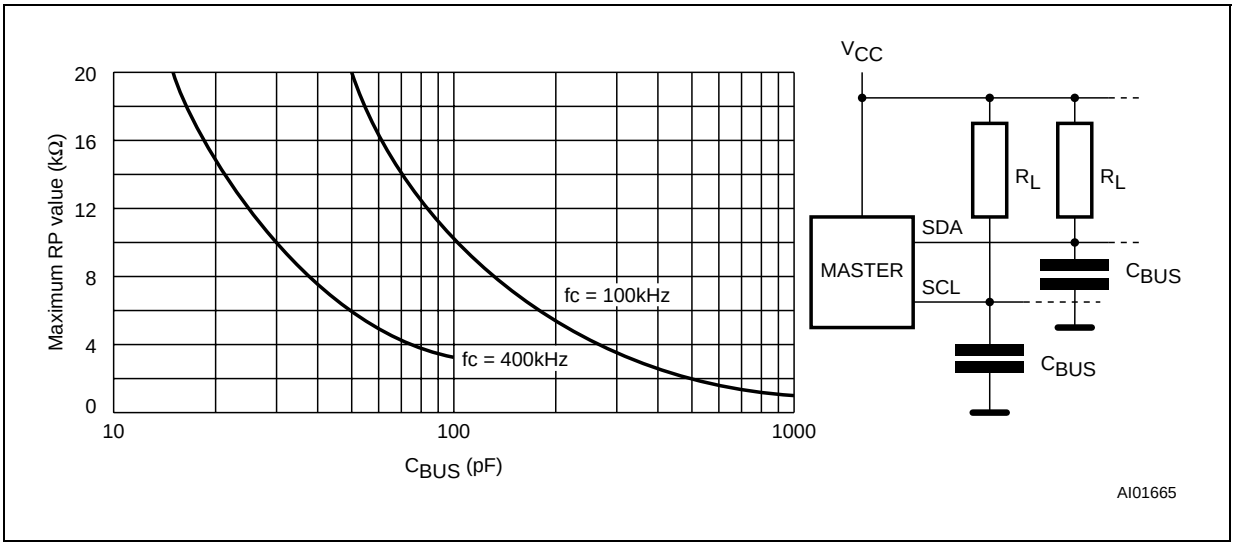


Figure 5. I²C Bus Protocol

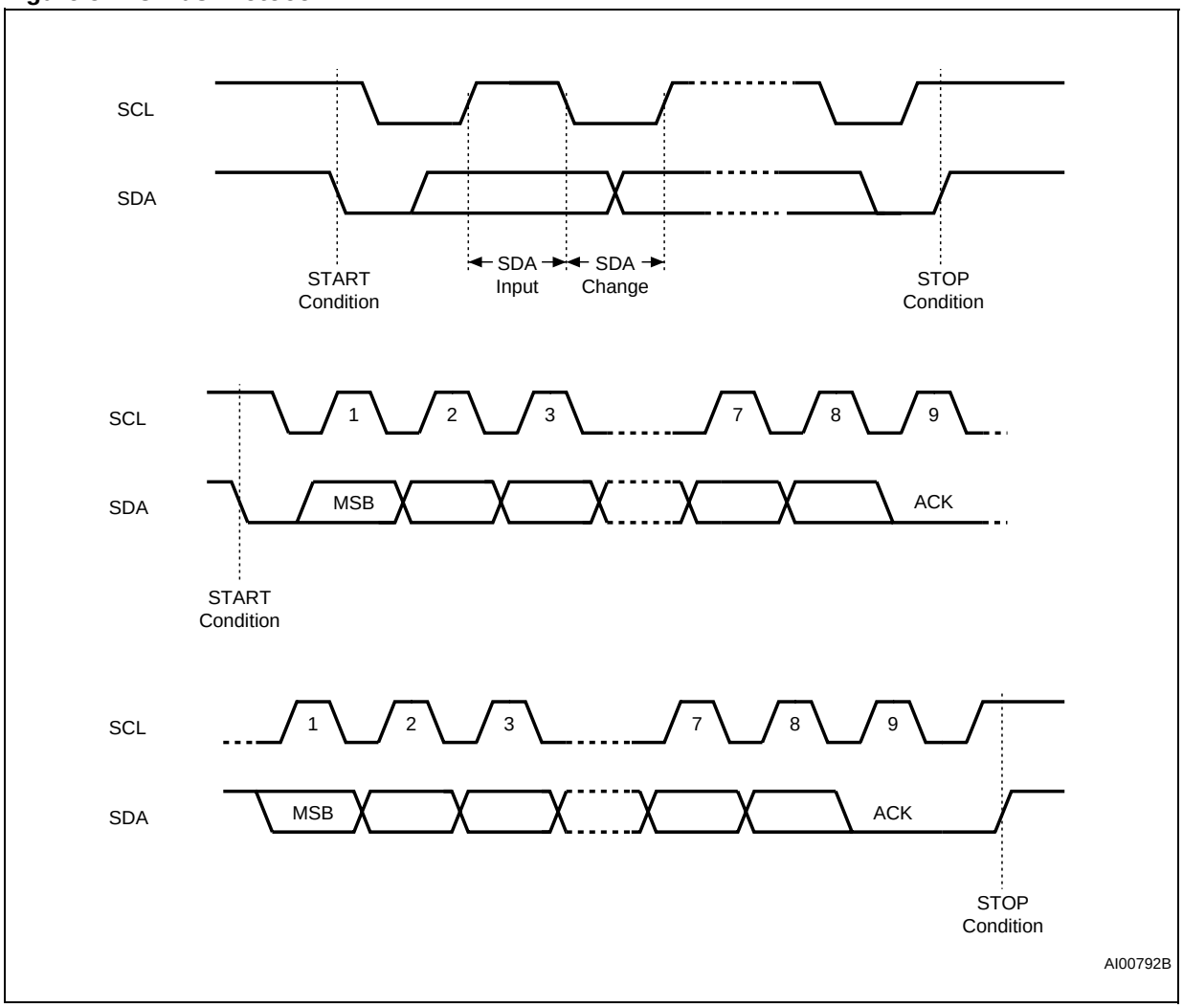


Table 2. Device Select Code

	Device Type Identifier[1]				Chip Enable[2,3]			RW
	b7	b6	b5	b4	b3	b2	b1	b0
M24C01 Select Code	1	0	1	0	E2	E1	E0	$R\overline{W}$
M24C02 Select Code	1	0	1	0	E2	E1	E0	$R\overline{W}$
M24C04 Select Code	1	0	1	0	E2	E1	A8	$R\overline{W}$
M24C08 Select Code	1	0	1	0	E2	A9	A8	$R\overline{W}$
M24C16 Select Code	1	0	1	0	A10	A9	A8	$R\overline{W}$

Note: 1. The most significant bit, b7, is sent first.
2. E0, E1 and E2 are compared against the respective external pins on the memory device.
3. A10, A9 and A8 represent most significant bits of the address.

DEVICE OPERATION

The device supports the I^2C protocol. This is summarized in Figure 5.. Any device that sends data on to the bus is defined to be a transmitter, and any device that reads the data to be a receiver. The device that controls the data transfer is known as the bus master, and the other as the slave device. A data transfer can only be initiated by the bus master, which will also provide the serial clock for synchronization. The M24Cxx device is always a slave in all communication.

Start Condition

Start is identified by a falling edge of Serial Data (SDA) while Serial Clock (SCL) is stable in the High state. A Start condition must precede any data transfer command. The device continuously monitors (except during a Write cycle) Serial Data (SDA) and Serial Clock (SCL) for a Start condition, and will not respond unless one is given.

Stop Condition

Stop is identified by a rising edge of Serial Data (SDA) while Serial Clock (SCL) is stable and driven High. A Stop condition terminates communication between the device and the bus master. A Read command that is followed by NoAck can be followed by a Stop condition to force the device into the Stand-by mode. A Stop condition at the end of a Write command triggers the internal EEPROM Write cycle.

Acknowledge Bit (ACK)

The acknowledge bit is used to indicate a successful byte transfer. The bus transmitter, whether it be bus master or slave device, releases Serial Data (SDA) after sending eight bits of data. During the 9th clock pulse period, the receiver pulls Serial Data (SDA) Low to acknowledge the receipt of the eight data bits.

Data Input

During data input, the device samples Serial Data (SDA) on the rising edge of Serial Clock (SCL). For correct device operation, Serial Data (SDA) must be stable during the rising edge of Serial Clock (SCL), and the Serial Data (SDA) signal must change *only* when Serial Clock (SCL) is driven Low.

Memory Addressing

To start communication between the bus master and the slave device, the bus master must initiate a Start condition. Following this, the bus master sends the Device Select Code, shown in Table 2. (on Serial Data (SDA), most significant bit first).

The Device Select Code consists of a 4-bit Device Type Identifier, and a 3-bit Chip Enable “Address” (E2, E1, E0). To address the memory array, the 4-bit Device Type Identifier is 1010b.

Each device is given a unique 3-bit code on the Chip Enable (E0, E1, E2) inputs. When the Device Select Code is received, the device only responds if the Chip Enable Address is the same as the value on the Chip Enable (E0, E1, E2) inputs. However, those devices with larger memory capacities (the M24C16, M24C08 and M24C04) need more address bits. E0 is not available for use on devices that need to use address line A8; E1 is not available for devices that need to use address line A9, and E2 is not available for devices that need to use address line A10 (see Figure 3. and Table 2. for details). Using the E0, E1 and E2 inputs, up to eight M24C02 (or M24C01), four M24C04, two M24C08 or one M24C16 devices can be connected to one I^2C bus. In each case, and in the hybrid cases, this gives a total memory capacity of 16 Kbits, 2 KBytes (except where M24C01 devices are used).

The 8th bit is the Read/$\overline{\text{Write}}$ bit (R$\overline{\text{W}}$). This bit is set to 1 for Read and 0 for Write operations.

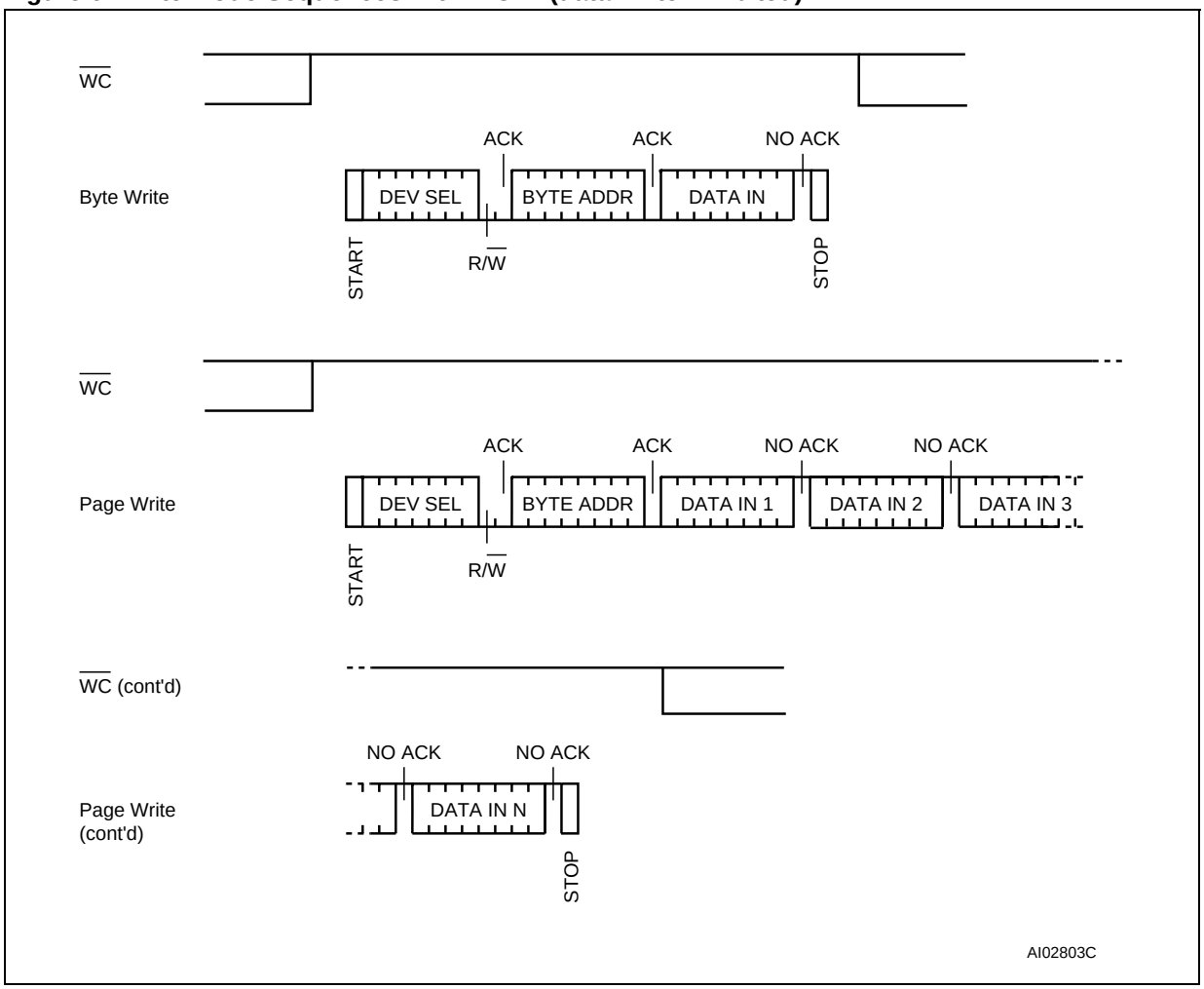
If a match occurs on the Device Select code, the corresponding device gives an acknowledgment on Serial Data (SDA) during the 9th bit time. If the device does not match the Device Select code, it deselects itself from the bus, and goes into Stand-by mode.

Table 3. Operating Modes

Mode	R$\overline{\text{W}}$ bit	$\overline{\text{WC}}$ [1]	Bytes	Initial Sequence
Current Address Read	1	X	1	START, Device Select, R$\overline{\text{W}}$ = 1
Random Address Read	0	X	1	START, Device Select, R$\overline{\text{W}}$ = 0, Address
	1	X		reSTART, Device Select, R$\overline{\text{W}}$ = 1
Sequential Read	1	X	≥ 1	Similar to Current or Random Address Read
Byte Write	0	V_{IL}	1	START, Device Select, R$\overline{\text{W}}$ = 0
Page Write	0	V_{IL}	≤ 16	START, Device Select, R$\overline{\text{W}}$ = 0

Note: 1. X = V_{IH} or V_{IL}.

Figure 6. Write Mode Sequences with $\overline{WC}$=1 (data write inhibited)



Write Operations

Following a Start condition the bus master sends a Device Select Code with the $\overline{RW}$ bit reset to 0. The device acknowledges this, as shown in Figure 7., and waits for an address byte. The device responds to the address byte with an acknowledge bit, and then waits for the data byte.

When the bus master generates a Stop condition immediately after the Ack bit (in the "10th bit" time slot), either at the end of a Byte Write or a Page Write, the internal memory Write cycle is triggered. A Stop condition at any other time slot does not trigger the internal Write cycle.

During the internal Write cycle, Serial Data (SDA) and Serial Clock (SCL) are ignored, and the device does not respond to any requests.

Byte Write

After the Device Select code and the address byte, the bus master sends one data byte. If the addressed location is Write-protected, by Write Control ($\overline{WC}$) being driven High (during the period from the Start condition until the end of the address byte), the device replies to the data byte with NoAck, as shown in Figure 6., and the location is not modified. If, instead, the addressed location is not Write-protected, the device replies with Ack. The bus master terminates the transfer by generating a Stop condition, as shown in Figure 7..

Page Write

The Page Write mode allows up to 16 bytes to be written in a single Write cycle, provided that they are all located in the same page in the memory: that is, the most significant memory address bits are the same. If more bytes are sent than will fit up to the end of the page, a condition known as 'roll-over' occurs. This should be avoided, as data starts to become overwritten in an implementation dependent way.

The bus master sends from 1 to 16 bytes of data, each of which is acknowledged by the device if Write Control ($\overline{WC}$) is Low. If the addressed location is Write-protected, by Write Control ($\overline{WC}$) being driven High (during the period from the Start

condition until the end of the address byte), the device replies to the data bytes with NoAck, as shown in Figure 6., and the locations are not modified. After each byte is transferred, the internal byte address counter (the 4 least significant address bits only) is incremented. The transfer is terminated by the bus master generating a Stop condition.

Figure 7. Write Mode Sequences with $\overline{WC}$=0 (data write enabled)

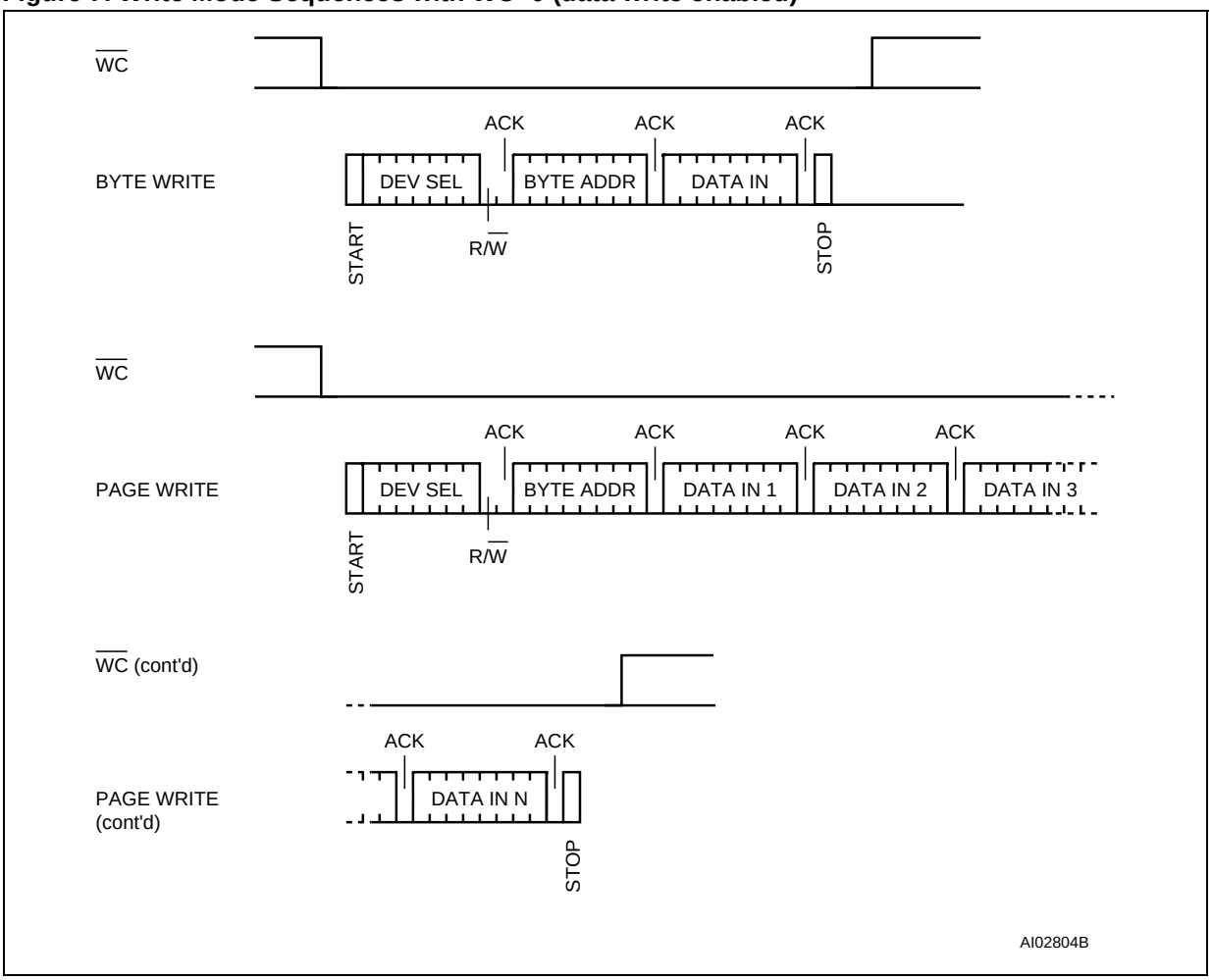
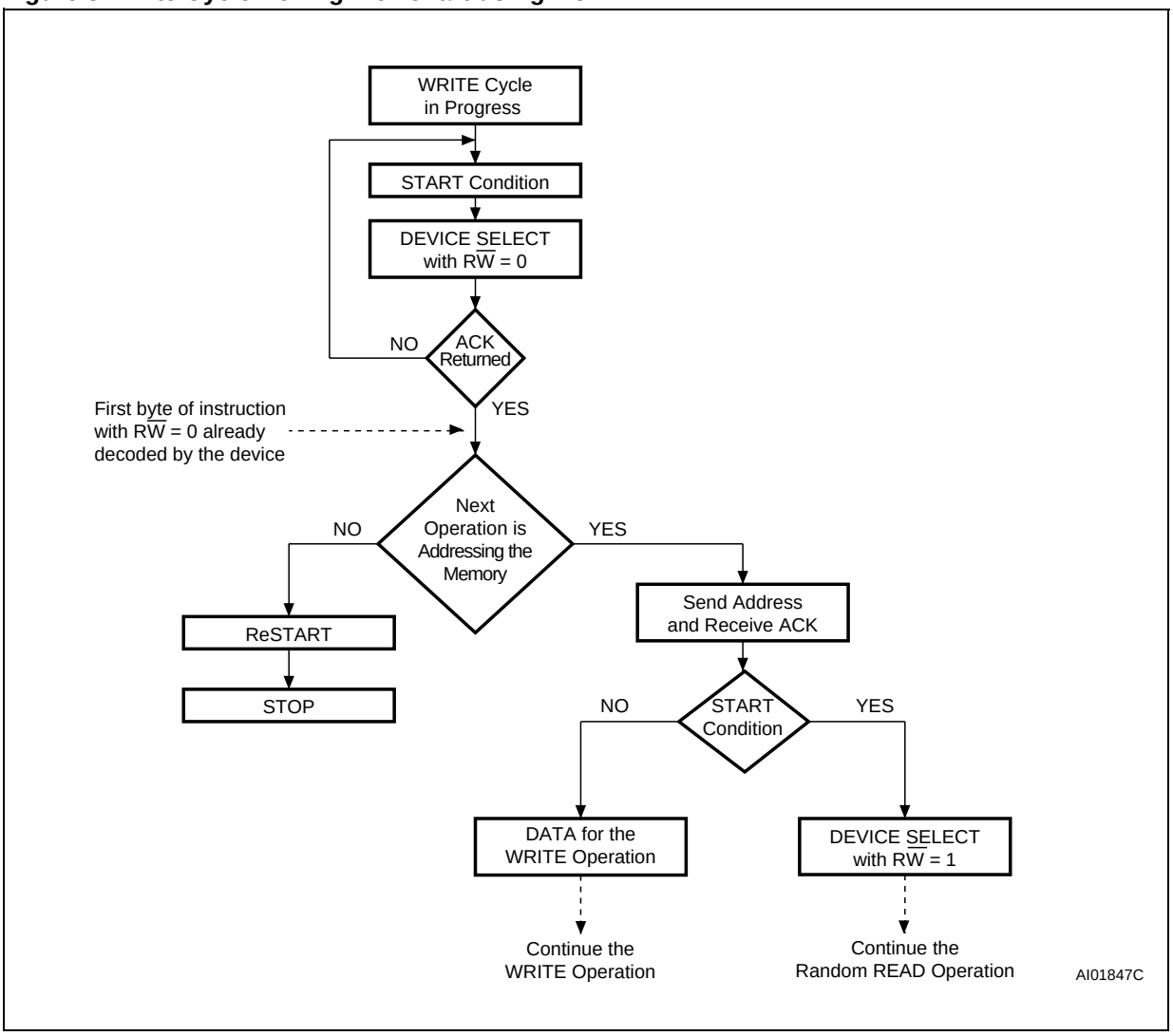


Figure 8. Write Cycle Polling Flowchart using ACK



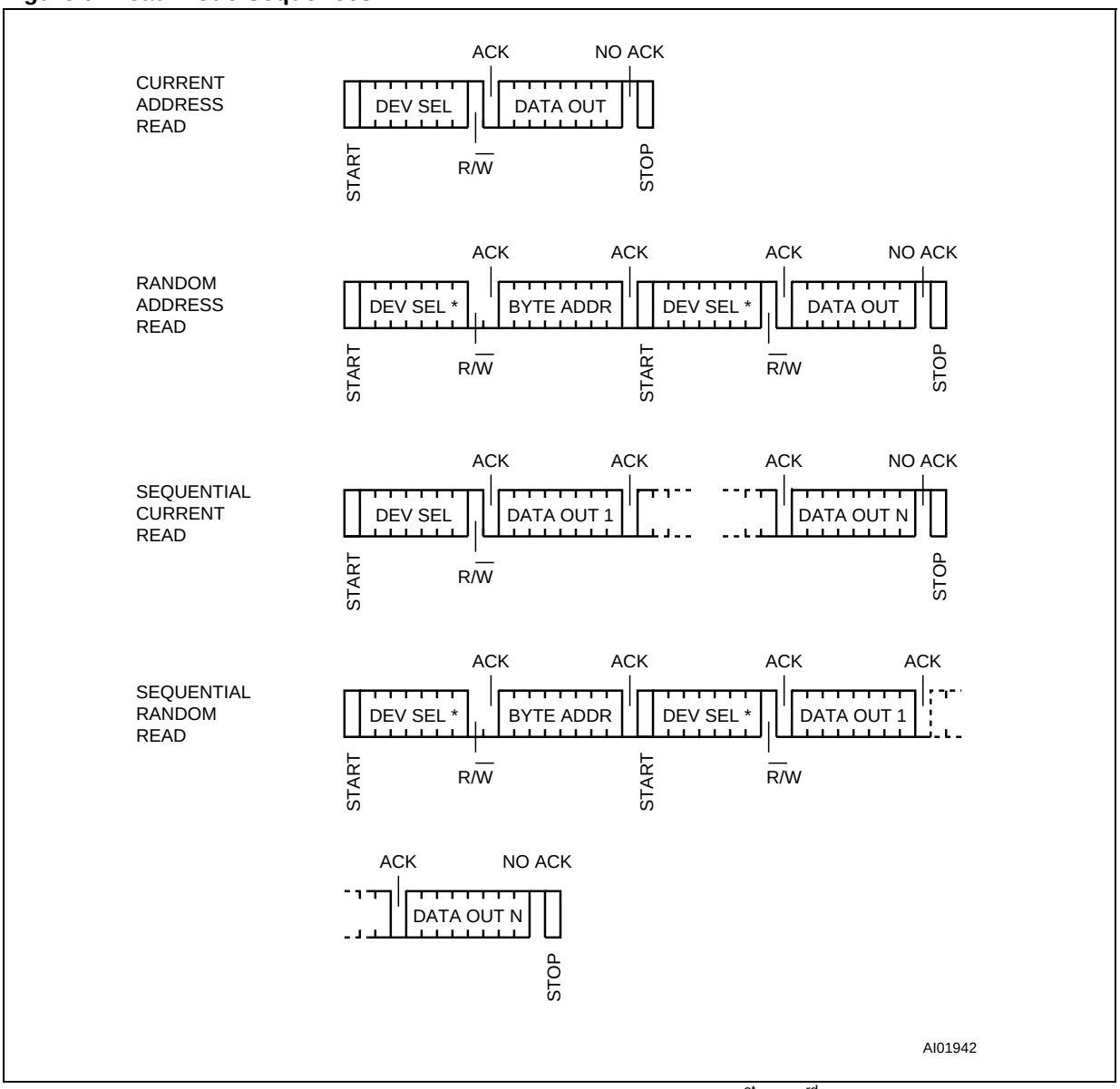
Minimizing System Delays by Polling On ACK

During the internal Write cycle, the device disconnects itself from the bus, and writes a copy of the data from its internal latches to the memory cells. The maximum Write time (t_W) is shown in Table 15. to Table 17., but the typical time is shorter. To make use of this, a polling sequence can be used by the bus master.

The sequence, as shown in Figure 8., is:

- Initial condition: a Write cycle is in progress.
- Step 1: the bus master issues a Start condition followed by a Device Select Code (the first byte of the new instruction).
- Step 2: if the device is busy with the internal Write cycle, no Ack will be returned and the bus master goes back to Step 1. If the device has terminated the internal Write cycle, it responds with an Ack, indicating that the device is ready to receive the second part of the instruction (the first byte of this instruction having been sent during Step 1).

Figure 9. Read Mode Sequences



Note: The seven most significant bits of the Device Select Code of a Random Read (in the 1st and 3rd bytes) must be identical.

Read Operations

Read operations are performed independently of the state of the Write Control ($\overline{WC}$) signal.

The device has an internal address counter which is incremented each time a byte is read.

Random Address Read

A dummy Write is first performed to load the address into this address counter (as shown in Figure 9.) but *without* sending a Stop condition. Then, the bus master sends another Start condition, and repeats the Device Select Code, with the $\overline{RW}$ bit set to 1. The device acknowledges this, and outputs the contents of the addressed byte. The bus master must *not* acknowledge the byte, and terminates the transfer with a Stop condition.

Current Address Read

For the Current Address Read operation, following a Start condition, the bus master only sends a Device Select Code with the $\overline{RW}$ bit set to 1. The device acknowledges this, and outputs the byte addressed by the internal address counter. The counter is then incremented. The bus master terminates the transfer with a Stop condition, as shown in Figure 9., *without* acknowledging the byte.

Sequential Read

This operation can be used after a Current Address Read or a Random Address Read. The bus master *does* acknowledge the data byte output, and sends additional clock pulses so that the device continues to output the next byte in sequence. To terminate the stream of bytes, the bus master must *not* acknowledge the last byte, and *must* generate a Stop condition, as shown in Figure 9..

The output data comes from consecutive addresses, with the internal address counter automatically incremented after each byte output. After the last memory address, the address counter 'rolls-over', and the device continues to output data from memory address 00h.

Acknowledge in Read Mode

For all Read commands, the device waits, after each byte read, for an acknowledgment during the 9th bit time. If the bus master does not drive Serial Data (SDA) Low during this time, the device terminates the data transfer and switches to its Standby mode.

INITIAL DELIVERY STATE

The device is delivered with the memory array erased: all bits are set to 1 (each byte contains FFh).

MAXIMUM RATING

Stressing the device above the rating listed in the Absolute Maximum Ratings" table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.

Table 4. Absolute Maximum Ratings

Symbol	Parameter	Min.	Max.	Unit
T_{STG}	Storage Temperature	–65	150	°C
T_{LEAD}	Lead Temperature during Soldering	See note [1]		°C
V_{IO}	Input or Output range	–0.50	6.5	V
V_{CC}	Supply Voltage	–0.50	6.5	V
V_{ESD}	Electrostatic Discharge Voltage (Human Body model) [2]	–4000	4000	V

Note: 1. Compliant with JEDEC Std J-STD-020B (for small body, Sn-Pb or Pb assembly), the ST ECOPACK® 7191395 specification, and the European directive on Restrictions on Hazardous Substances (RoHS) 2002/95/EU
2. JEDEC Std JESD22-A114A (C1=100 pF, R1=1500 Ω, R2=500 Ω)

DC AND AC PARAMETERS

This section summarizes the operating and measurement conditions, and the DC and AC characteristics of the device. The parameters in the DC and AC Characteristic tables that follow are derived from tests performed under the Measurement Conditions summarized in the relevant tables. Designers should check that the operating conditions in their circuit match the measurement conditions when relying on the quoted parameters.

Table 5. Operating Conditions (M24Cxx)

Symbol	Parameter	Min.	Max.	Unit
V_{CC}	Supply Voltage	4.5	5.5	V
T_A	Ambient Operating Temperature (Device Grade 6)	–40	85	°C
	Ambient Operating Temperature (Device Grade 3)	–40	125	°C

Note: 1. This range is Not for New Design, and will soon be replaced by the M24Cxx-W range.

Table 6. Operating Conditions (M24Cxx-W)

Symbol	Parameter	Min.	Max.	Unit
V_{CC}	Supply Voltage	2.5	5.5	V
T_A	Ambient Operating Temperature (Device Grade 6)	–40	85	°C
	Ambient Operating Temperature (Device Grade 3)	–40	125	°C

Table 7. Operating Conditions (M24Cxx-R)

Symbol	Parameter	Min.	Max.	Unit
V_{CC}	Supply Voltage	1.8	5.5	V
T_A	Ambient Operating Temperature	–40	85	°C

Table 8. AC Measurement Conditions

Symbol	Parameter	Min.	Max.	Unit
C_L	Load Capacitance	100		pF
	Input Rise and Fall Times		50	ns
	Input Levels	$0.2V_{CC}$ to $0.8V_{CC}$		V
	Input and Output Timing Reference Levels	$0.3V_{CC}$ to $0.7V_{CC}$		V

Figure 10. AC Measurement I/O Waveform

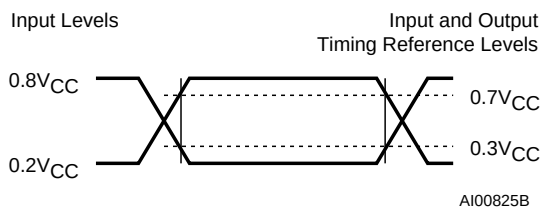


Table 9. Input Parameters

Symbol	Parameter[1,2]	Test Condition	Min.	Max.	Unit
C_{IN}	Input Capacitance (SDA)			8	pF
C_{IN}	Input Capacitance (other pins)			6	pF
Z_{WCL}	$\overline{WC}$ Input Impedance	$V_{IN} < 0.5$ V	5	70	kΩ
Z_{WCH}	$\overline{WC}$ Input Impedance	$V_{IN} > 0.7V_{CC}$	500		kΩ
t_{NS}	Pulse width ignored (Input Filter on SCL and SDA)	Single glitch		100	ns

Note: 1. $T_A = 25°C$, f = 400kHz
2. Sampled only, not 100% tested.

Table 10. DC Characteristics (M24Cxx, Device Grade 6)

Symbol	Parameter	Test Condition (in addition to those in Table 5.)	Min.	Max.	Unit
I_{LI}	Input Leakage Current (SCL, SDA)	$V_{IN} = V_{SS}$ or V_{CC}		± 2	µA
I_{LO}	Output Leakage Current	$V_{OUT} = V_{SS}$ or V_{CC}, SDA in Hi-Z		± 2	µA
I_{CC}	Supply Current	V_{CC}=5V, f_c=400kHz (rise/fall time < 30ns)		2	mA
I_{CC1}	Stand-by Supply Current	$V_{IN} = V_{SS}$ or V_{CC} , $V_{CC} = 5$ V		1	µA
V_{IL}	Input Low Voltage (E2, E1, E0, SCL, SDA)		–0.45	$0.3V_{CC}$	V
	Input Low Voltage ($\overline{WC}$)		–0.45	0.5	V
V_{IH}	Input High Voltage (E2, E1, E0, SCL, SDA, $\overline{WC}$)		$0.7V_{CC}$	V_{CC}+1	V
V_{OL}	Output Low Voltage	$I_{OL} = 3$ mA, $V_{CC} = 5$ V		0.4	V

Note: 1. This range is Not for New Design, and will soon be replaced by the M24Cxx-Wxx6 range.

Table 11. DC Characteristics (M24Cxx, Device Grade 3)

Symbol	Parameter	Test Condition (in addition to those in Table 5.)	Min.	Max.	Unit
I_{LI}	Input Leakage Current (SCL, SDA)	$V_{IN} = V_{SS}$ or V_{CC}		± 2	µA
I_{LO}	Output Leakage Current	$V_{OUT} = V_{SS}$ or V_{CC}, SDA in Hi-Z		± 2	µA
I_{CC}	Supply Current	V_{CC}=5V, f_c=400kHz (rise/fall time < 30ns)		3	mA
I_{CC1}	Stand-by Supply Current	$V_{IN} = V_{SS}$ or V_{CC} , V_{CC} = 5 V		5	µA
V_{IL}	Input Low Voltage (E2, E1, E0, SCL, SDA)		–0.45	$0.3V_{CC}$	V
	Input Low Voltage ($\overline{WC}$)		–0.45	0.5	V
V_{IH}	Input High Voltage (E2, E1, E0, SCL, SDA, $\overline{WC}$)		$0.7V_{CC}$	V_{CC}+1	V
V_{OL}	Output Low Voltage	I_{OL} = 3 mA, V_{CC} = 5 V		0.4	V

Note: 1. This range is Not for New Design, and will soon be replaced by the M24Cxx-Wxx3 range.

Table 12. DC Characteristics (M24Cxx-W, Device Grade 6)

Symbol	Parameter	Test Condition (in addition to those in Table 6.)	Min.	Max.	Unit
I_{LI}	Input Leakage Current (SCL, SDA)	$V_{IN} = V_{SS}$ or V_{CC}		± 2	µA
I_{LO}	Output Leakage Current	$V_{OUT} = V_{SS}$ or V_{CC}, SDA in Hi-Z		± 2	µA
I_{CC}	Supply Current	V_{CC} =2.5V, f_c=400kHz (rise/fall time < 30ns)		1	mA
I_{CC1}	Stand-by Supply Current	$V_{IN} = V_{SS}$ or V_{CC} , V_{CC} = 2.5 V		0.5	µA
V_{IL}	Input Low Voltage (E2, E1, E0, SCL, SDA)		–0.45	$0.3V_{CC}$	V
	Input Low Voltage ($\overline{WC}$)		–0.45	0.5	V
V_{IH}	Input High Voltage (E2, E1, E0, SCL, SDA, $\overline{WC}$)		$0.7V_{CC}$	V_{CC}+1	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1 mA, V_{CC} = 2.5 V		0.4	V

Table 13. DC Characteristics (M24Cxx-W, Device Grade 3)

Symbol	Parameter	Test Condition (in addition to those in Table 6.)	Min.[1]	Max.[1]	Unit
I_{LI}	Input Leakage Current (SCL, SDA)	$V_{IN} = V_{SS}$ or V_{CC}		± 2	µA
I_{LO}	Output Leakage Current	$V_{OUT} = V_{SS}$ or V_{CC}, SDA in Hi-Z		± 2	µA
I_{CC}	Supply Current	V_{CC} =2.5V, f_c=400kHz (rise/fall time < 30ns)		3	mA
I_{CC1}	Stand-by Supply Current	$V_{IN} = V_{SS}$ or V_{CC} , V_{CC} = 2.5 V		2	µA
V_{IL}	Input Low Voltage (E2, E1, E0, SCL, SDA)		–0.45	$0.3V_{CC}$	V
	Input Low Voltage ($\overline{WC}$)		–0.45	0.5	V
V_{IH}	Input High Voltage (E2, E1, E0, SCL, SDA, $\overline{WC}$)		$0.7V_{CC}$	V_{CC}+1	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1 mA, V_{CC} = 2.5 V		0.4	V

Note: 1. This is preliminary data.

Table 14. DC Characteristics (M24Cxx-R)

Symbol	Parameter	Test Condition (in addition to those in Table 7.)	Min.	Max.	Unit
I_{LI}	Input Leakage Current (SCL, SDA)	$V_{IN} = V_{SS}$ or V_{CC}		± 2	µA
I_{LO}	Output Leakage Current	$V_{OUT} = V_{SS}$ or V_{CC}, SDA in Hi-Z		± 2	µA
I_{CC}	Supply Current	V_{CC} =1.8V, f_c=400kHz (rise/fall time < 30ns)		0.8	mA
I_{CC1}	Stand-by Supply Current	$V_{IN} = V_{SS}$ or V_{CC} , V_{CC} = 1.8 V		0.3	µA
V_{IL}	Input Low Voltage (E2, E1, E0, SCL, SDA)	2.5 V ≤ V_{CC}	–0.45	0.3 V_{CC}	V
		1.8 V ≤ V_{CC} < 2.5 V	–0.45	0.25 V_{CC}	V
	Input Low Voltage ($\overline{WC}$)		–0.45	0.5	V
V_{IH}	Input High Voltage (E2, E1, E0, SCL, SDA, $\overline{WC}$)		$0.7V_{CC}$	V_{CC}+1	V
V_{OL}	Output Low Voltage	I_{OL} = 0.7 mA, V_{CC} = 1.8 V		0.2	V

Table 15. AC Characteristics (M24Cxx, Device Grade 6)

Test conditions specified in Table 8. and Table 5.					
Symbol	**Alt.**	**Parameter**	**Min.[4]**	**Max.[4]**	**Unit**
f_C	f_{SCL}	Clock Frequency		400	kHz
t_{CHCL}	t_{HIGH}	Clock Pulse Width High	600		ns
t_{CLCH}	t_{LOW}	Clock Pulse Width Low	1300		ns
t_{DL1DL2} [2]	t_F	SDA Fall Time	20	300	ns
t_{DXCX}	$t_{SU:DAT}$	Data In Set Up Time	100		ns
t_{CLDX}	$t_{HD:DAT}$	Data In Hold Time	0		ns
t_{CLQX}	t_{DH}	Data Out Hold Time	200		ns
t_{CLQV} [3]	t_{AA}	Clock Low to Next Data Valid (Access Time)	200	900	ns
t_{CHDX} [1]	$t_{SU:STA}$	Start Condition Set Up Time	600		ns
t_{DLCL}	$t_{HD:STA}$	Start Condition Hold Time	600		ns
t_{CHDH}	$t_{SU:STO}$	Stop Condition Set Up Time	600		ns
t_{DHDL}	t_{BUF}	Time between Stop Condition and Next Start Condition	1300		ns
t_W	t_{WR}	Write Time		5	ms

Note: 1. For a reSTART condition, or following a Write cycle.
2. Sampled only, not 100% tested.
3. To avoid spurious START and STOP conditions, a minimum delay is placed between SCL=1 and the falling or rising edge of SDA.
4. This is preliminary data for M24Cxx-Wxx3.

Table 16. AC Characteristics (M24Cxx, Device Grade 3; M24Cxx-W, Device Grade 6 or 3)

Test conditions specified in Table 8. and Table 5. or Table 6.					
Symbol	**Alt.**	**Parameter**	**Min.**	**Max.**	**Unit**
f_C	f_{SCL}	Clock Frequency		400	kHz
t_{CHCL}	t_{HIGH}	Clock Pulse Width High	600		ns
t_{CLCH}	t_{LOW}	Clock Pulse Width Low	1300		ns
t_{DL1DL2} [2]	t_F	SDA Fall Time	20	300	ns
t_{DXCX}	$t_{SU:DAT}$	Data In Set Up Time	100		ns
t_{CLDX}	$t_{HD:DAT}$	Data In Hold Time	0		ns
t_{CLQX}	t_{DH}	Data Out Hold Time	200		ns
t_{CLQV} [3]	t_{AA}	Clock Low to Next Data Valid (Access Time)	200	900	ns
t_{CHDX} [1]	$t_{SU:STA}$	Start Condition Set Up Time	600		ns
t_{DLCL}	$t_{HD:STA}$	Start Condition Hold Time	600		ns
t_{CHDH}	$t_{SU:STO}$	Stop Condition Set Up Time	600		ns
t_{DHDL}	t_{BUF}	Time between Stop Condition and Next Start Condition	1300		ns
t_W	t_{WR}	Write Time		10 or[4] 5	ms

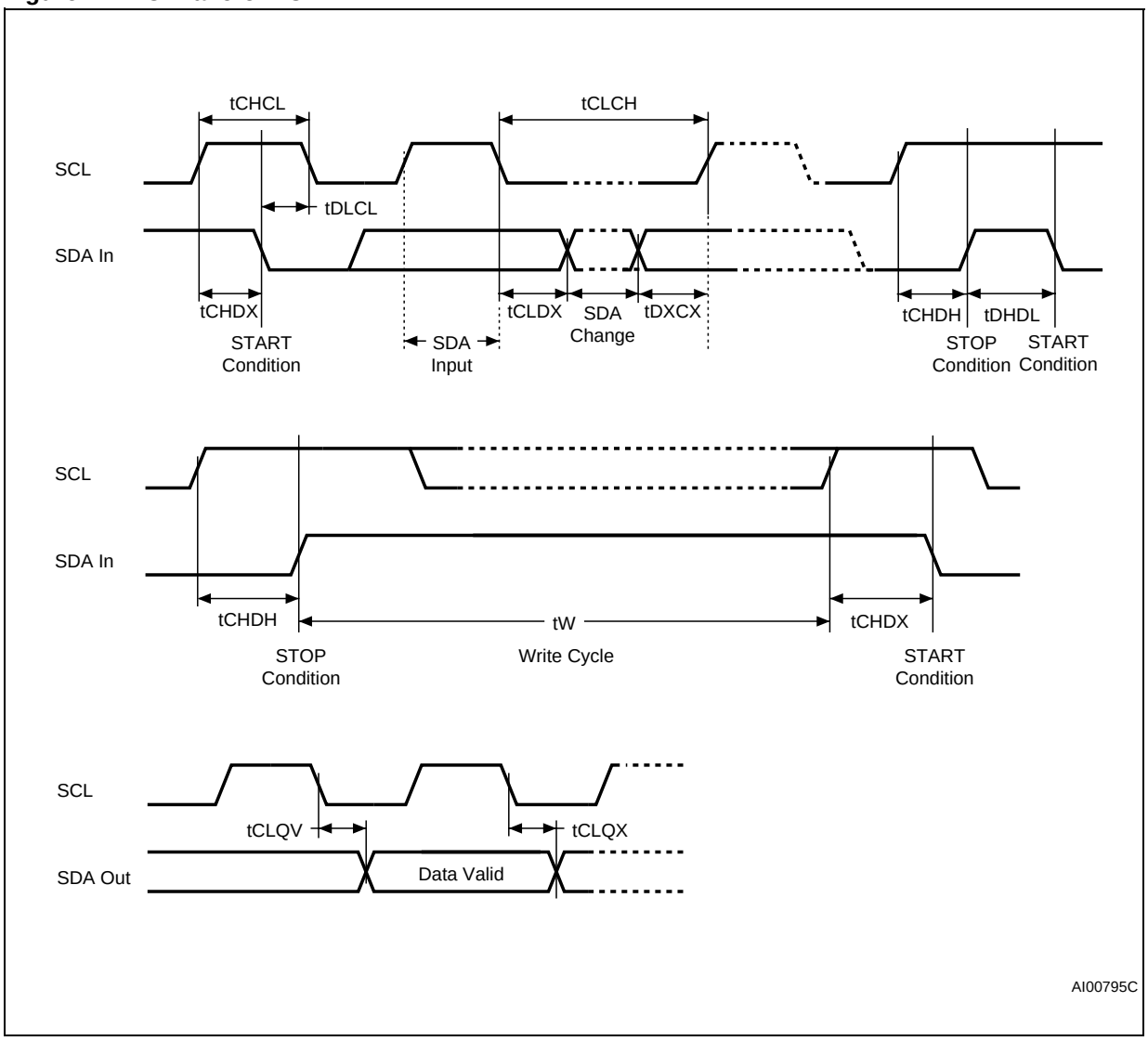
Note: 1. For a reSTART condition, or following a Write cycle.
2. Sampled only, not 100% tested.
3. To avoid spurious START and STOP conditions, a minimum delay is placed between SCL=1 and the falling or rising edge of SDA.
4. 10ms write time is offered on the standard device. 5ms write time is offered on new products bearing the Process Identification letter “W” or “G” on the package, as described in Table 24..

Table 17. AC Characteristics (M24Cxx-R)

Test conditions specified in Table 8. and Table 7.							
Symbol	**Alt.**	**Parameter**	**Min.**	**Max.**	**Min.[4]**	**Max.[4]**	**Unit**
f_C	f_{SCL}	Clock Frequency		100		400	kHz
t_{CHCL}	t_{HIGH}	Clock Pulse Width High	4000		600		ns
t_{CLCH}	t_{LOW}	Clock Pulse Width Low	4700		1300		ns
t_{DL1DL2} [2]	t_F	SDA Fall Time	20	300	20	300	ns
t_{DXCX}	$t_{SU:DAT}$	Data In Set Up Time	250		100		ns
t_{CLDX}	$t_{HD:DAT}$	Data In Hold Time	0		0		ns
t_{CLQX}	t_{DH}	Data Out Hold Time	200		200		ns
t_{CLQV} [3]	t_{AA}	Clock Low to Next Data Valid (Access Time)	200	3500	200	900	ns
t_{CHDX} [1]	$t_{SU:STA}$	Start Condition Set Up Time	4700		600		ns
t_{DLCL}	$t_{HD:STA}$	Start Condition Hold Time	4000		600		ns
t_{CHDH}	$t_{SU:STO}$	Stop Condition Set Up Time	4000		600		ns
t_{DHDL}	t_{BUF}	Time between Stop Condition and Next Start Condition	4700		1300		ns
t_W	t_{WR}	Write Time		10		10	ms

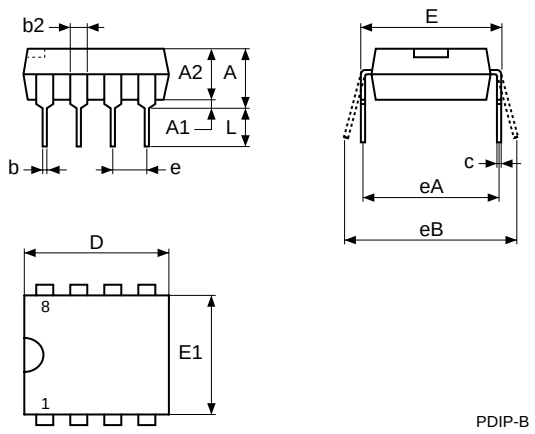
Note: 1. For a reSTART condition, or following a Write cycle.
2. Sampled only, not 100% tested.
3. To avoid spurious START and STOP conditions, a minimum delay is placed between SCL=1 and the falling or rising edge of SDA.
4. 100kHz clock frequency is offered on the standard device. 400kHz clock frequency is offered on new products bearing the Process Identification letter “W” or “G” on the package, as described in Table 24..

Figure 11. AC Waveforms



PACKAGE MECHANICAL

Figure 12. PDIP8 – 8 pin Plastic DIP, 0.25mm lead frame, Package Outline

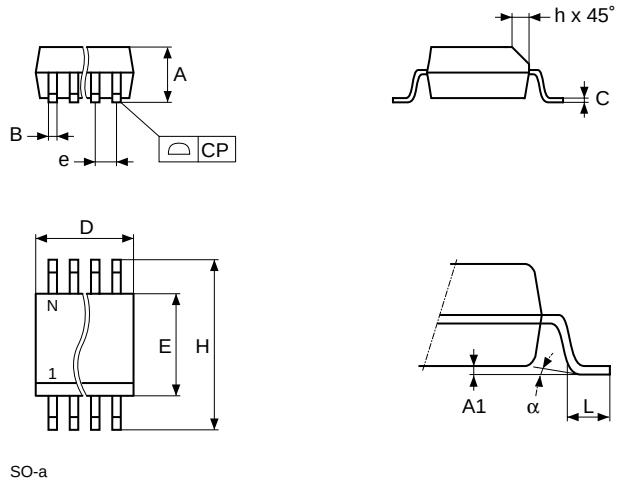


Note: Drawing is not to scale.

Table 18. PDIP8 – 8 pin Plastic DIP, 0.25mm lead frame, Package Mechanical Data

Symb.	mm			inches		
	Typ.	Min.	Max.	Typ.	Min.	Max.
A			5.33			0.210
A1		0.38			0.015	
A2	3.30	2.92	4.95	0.130	0.115	0.195
b	0.46	0.36	0.56	0.018	0.014	0.022
b2	1.52	1.14	1.78	0.060	0.045	0.070
c	0.25	0.20	0.36	0.010	0.008	0.014
D	9.27	9.02	10.16	0.365	0.355	0.400
E	7.87	7.62	8.26	0.310	0.300	0.325
E1	6.35	6.10	7.11	0.250	0.240	0.280
e	2.54	–	–	0.100	–	–
eA	7.62	–	–	0.300	–	–
eB			10.92			0.430
L	3.30	2.92	3.81	0.130	0.115	0.150

Figure 13. SO8 narrow – 8 lead Plastic Small Outline, 150 mils body width, Package Outline

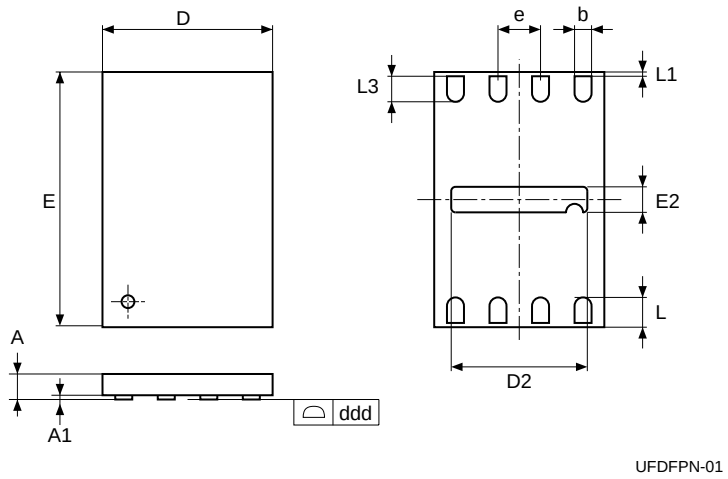


Note: Drawing is not to scale.

Table 19. SO8 narrow – 8 lead Plastic Small Outline, 150 mils body width, Package Mechanical Data

Symb.	mm			inches		
	Typ.	Min.	Max.	Typ.	Min.	Max.
A		1.35	1.75		0.053	0.069
A1		0.10	0.25		0.004	0.010
B		0.33	0.51		0.013	0.020
C		0.19	0.25		0.007	0.010
D		4.80	5.00		0.189	0.197
E		3.80	4.00		0.150	0.157
e	1.27	–	–	0.050	–	–
H		5.80	6.20		0.228	0.244
h		0.25	0.50		0.010	0.020
L		0.40	0.90		0.016	0.035
α		0°	8°		0°	8°
N	8			8		
CP			0.10			0.004

Figure 14. UFDFPN8 (MLP8) 8-lead Ultra thin Fine pitch Dual Flat Package No lead 2x3mm², Outline

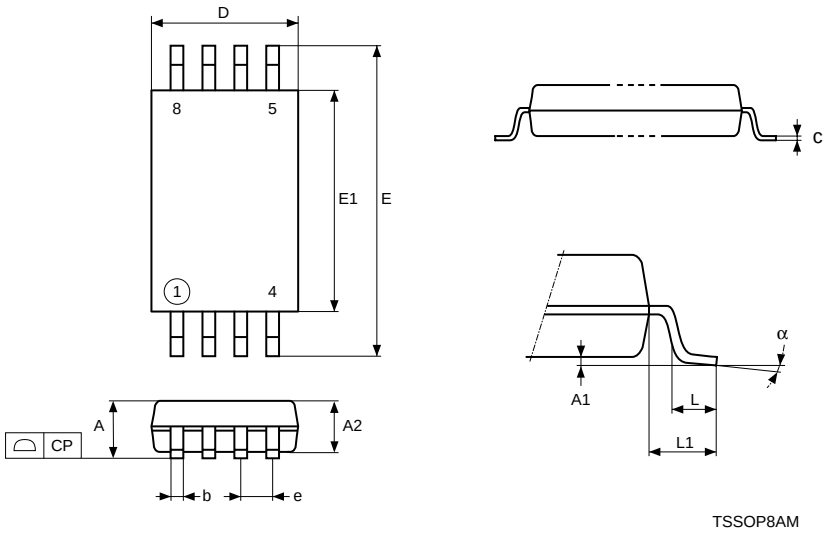


Note: 1. Drawing is not to scale.
2. The central pad (the area E2 by D2 in the above illustration) is pulled, internally, to V_{SS}. It must not be allowed to be connected to any other voltage or signal line on the PCB, for example during the soldering process.

Table 20. UFDFPN8 (MLP8) 8-lead Ultra thin Fine pitch Dual Flat Package No lead 2x3mm², Data

Symbol	mm			inches		
	Typ.	Min.	Max.	Typ.	Min.	Max.
A	0.55	0.50	0.60	0.022	0.020	0.024
A1		0.00	0.05		0.000	0.002
b	0.25	0.20	0.30	0.010	0.008	0.012
D	2.00			0.079		
D2		1.55	1.65		0.061	0.065
ddd			0.05			0.002
E	3.00			0.118		
E2		0.15	0.25		0.006	0.010
e	0.50	–	–	0.020	–	–
L	0.45	0.40	0.50	0.018	0.016	0.020
L1			0.15			0.006
L3		0.30			0.012	
N	8			8		

Figure 15. TSSOP8 – 8 lead Thin Shrink Small Outline, Package Outline

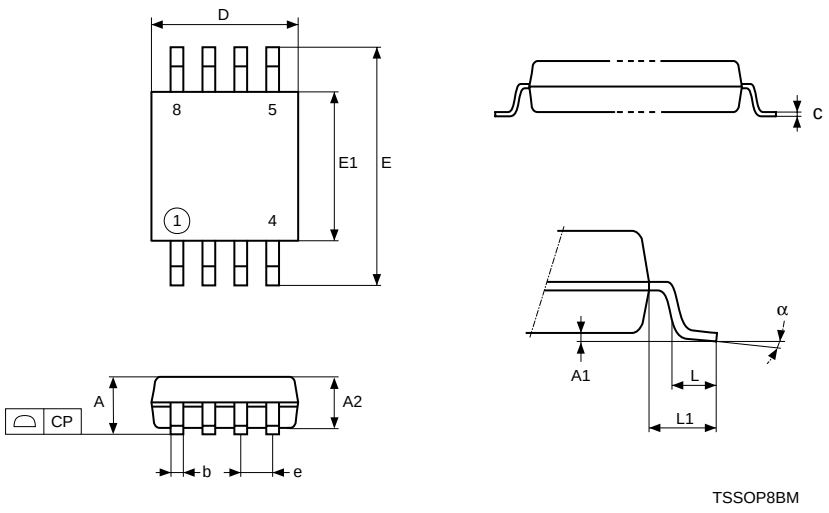


Note: Drawing is not to scale.

Table 21. TSSOP8 – 8 lead Thin Shrink Small Outline, Package Mechanical Data

Symbol	mm			inches		
	Typ.	Min.	Max.	Typ.	Min.	Max.
A			1.200			0.0472
A1		0.050	0.150		0.0020	0.0059
A2	1.000	0.800	1.050	0.0394	0.0315	0.0413
b		0.190	0.300		0.0075	0.0118
c		0.090	0.200		0.0035	0.0079
CP			0.100			0.0039
D	3.000	2.900	3.100	0.1181	0.1142	0.1220
e	0.650	–	–	0.0256	–	–
E	6.400	6.200	6.600	0.2520	0.2441	0.2598
E1	4.400	4.300	4.500	0.1732	0.1693	0.1772
L	0.600	0.450	0.750	0.0236	0.0177	0.0295
L1	1.000			0.0394		
α		0°	8°		0°	8°

Figure 16. TSSOP8 3x3mm² – 8 lead Thin Shrink Small Outline, 3x3mm² body size, Package Outline



Note: Drawing is not to scale.

Table 22. TSSOP8 3x3mm² – 8 lead Thin Shrink Small Outline, 3x3mm² body size, Mechanical Data

Symbol	mm			inches		
	Typ.	Min.	Max.	Typ.	Min.	Max.
A			1.100			0.0433
A1		0.050	0.150		0.0020	0.0059
A2	0.850	0.750	0.950	0.0335	0.0295	0.0374
b		0.250	0.400		0.0098	0.0157
c		0.130	0.230		0.0051	0.0091
D	3.000	2.900	3.100	0.1181	0.1142	0.1220
E	4.900	4.650	5.150	0.1929	0.1831	0.2028
E1	3.000	2.900	3.100	0.1181	0.1142	0.1220
e	0.650	–	–	0.0256	–	–
CP			0.100			0.0039
L	0.550	0.400	0.700	0.0217	0.0157	0.0276
L1	0.950			0.0374		
α		0°	6°		0°	6°

PART NUMBERING

Table 23. Ordering Information Scheme

Example: M24C08 – W DW 6 T P /W

Device Type

M24 = I^2C serial access EEPROM

Device Function

16 = 16 Kbit (2048 x 8)
08 = 8 Kbit (1024 x 8)
04 = 4 Kbit (512 x 8)
02 = 2 Kbit (256 x 8)
01 = 1 Kbit (128 x 8)

Operating Voltage

blank [4] = V_{CC} = 4.5 to 5.5V (400kHz)
W [2] = V_{CC} = 2.5 to 5.5V (400kHz)
R = V_{CC} = 1.8 to 5.5V (400kHz)

Package

BN = PDIP8
MN = SO8 (150 mil width)
MB = UDFDFPN8 (MLP8)
DW = TSSOP8 (169 mil width)
DS = TSSOP8 (3x3mm² body size, MSOP8)

Device Grade

6 = Industrial: device tested with standard test flow over –40 to 85 °C
3 = Automotive: device tested with High Reliability Certified Flow[1] over –40 to 125 °C

Option

T = Tape & Reel Packing

Plating Technology

blank = Standard SnPb plating
P = Lead-Free and RoHS compliant
G = Lead-Free, RoHS compliant, Sb_2O_3-free and TBBA-free

Process[3]

blank = F6SP20%
/W = F6SP36%
/G = F6SP36%

Note:
1. ST strongly recommends the use of the Automotive Grade devices for use in an automotive environment. The High Reliability Certified Flow (HRCF) is described in the quality note QNEE9801. Please ask your nearest ST sales office for a copy.
2. 2.5 to 5.5V devices bearing the process letter “W” or “G” in the package marking (on the top side of the package, on the right side, see Table 24.), guarantee a maximum write time of 5ms, instead of the standard 10ms. For more information about these devices, and their device identification, please ask your ST Sales Office for Process Change Notices PCN MPG/EE/0061 and 0062 (PCEE0061 and PCEE0062).
3. Used only for Device Grade 3
4. This range is Not for New Design, and will soon be replaced by the M24Cxx-W range.

For a list of available options (speed, package, etc.) or for further information on any aspect of this device, please contact your nearest ST Sales Office.

Table 24. How to Identify Current and New Products by the Process Identification Letter

Markings on Current Products[1]	Markings on New Products[1]	
24CxxW6 ST xxxx**L**	24CxxW6 ST xxxx**W**	24CxxW6 ST xxxx**G**

Note: 1. This example comes from the S08 package. Other packages have similar information. For further information, please ask your ST Sales Office for Process Change Notices PCN MPG/EE/0061 and 0062 (PCEE0061 and PCEE0062).

REVISION HISTORY

Table 25. Document Revision History

Date	Version	Description of Revision
10-Dec-1999	2.4	TSSOP8 Turned-Die package removed (p 2 and order information) Lead temperature added for TSSOP8 in table 2
18-Apr-2000	2.5	Labelling change to Fig-2D, correction of values for ‘E’ and main caption for Tab-13
05-May-2000	2.6	Extra labelling to Fig-2D
23-Nov-2000	3.0	SBGA package information removed to an annex document -R range changed to being the -S range, and the new -R range added
19-Feb-2001	3.1	SBGA package information put back in this document Lead Soldering Temperature in the Absolute Maximum Ratings table amended Write Cycle Polling Flow Chart using ACK illustration updated References to PSDIP changed to PDIP and Package Mechanical data updated Wording brought in to line with standard glossary
20-Apr-2001	3.2	Revision of DC and AC characteristics for the -S series
08-Oct-2001	3.3	Ball numbers added to the SBGA connections and package mechanical illustrations
09-Nov-2001	3.4	Specification of Test Condition for Leakage Currents in the DC Characteristics table improved
30-Jul-2002	3.5	Document reformatted using new template. SBGA5 package removed TSSOP8 (3x3mm² body size) package (MSOP8) added. -L voltage range added
04-Feb-2003	3.6	Document title spelt out more fully. “W”-marked devices with tw=5ms added.
05-May-2003	3.7	-R voltage range upgraded to 400kHz working, and no longer preliminary data. 5V voltage range at temperature range 3 (-xx3) no longer preliminary data. -S voltage range removed. -Wxx3 voltage+temp ranged added as preliminary data.
07-Oct-2003	4.0	Table of contents, and Pb-free options added. Minor wording changes in Summary Description, Power-On Reset, Memory Addressing, Read Operations. V_{IL}(min) improved to -0.45V. t_W(max) value for -R voltage range corrected.
17-Mar-2004	5.0	MLP package added. Absolute Maximum Ratings for V_{IO}(min) and V_{CC}(min) changed. Soldering temperature information clarified for RoHS compliant devices. Device grade information clarified. Process identification letter “G” information added. 2.2-5.5V range is removed, and 4.5-5.5V range is now Not for New Design

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