THAT Corporation

High-Performance Digital Preamplifier Controller IC

THAT 5171

FEATURES

- Ideal mate for THAT1570 preamplifier
- Wide gain range:
  - +13.6 to +68.6dB in 1dB steps, and
  - +5.6dB
- Wide supply range: ±5V to ±17V
- Wide output swing: +27dBu (±17V sup.)
- Wide input swing: +22dBu (±17V sup.)
- Low THD+N: 0.0003% @ 22dB gain
- Integrated differential servo minimizes output offset
- Zero-crossing detector minimizes switching noise
- Flexible, addressable SPI interface
- Four general-purpose digital outputs
- Small 7mm x 7mm QFN32 package

APPLICATIONS

- Digitally controlled microphone preamplifiers
- Digitally-controlled instrumentation amplifiers
- Digitally-controlled differential amplifiers
- Audio mixing consoles
- PC audio breakout boxes
- Audio distribution systems
- Digital audio snakes
- Portable audio recorders

Description

The THAT5171 is a digital gain controller for low-noise, analog, differential, current-feedback audio preamplifiers such as the THAT 1570. When used in conjunction with an appropriate analog gain block, the 5171 can set gain to 5.6dB, or any gain from 13.6dB to 68.6dB in 1dB steps, while preserving low noise and distortion. It operates from ±5V to ±17V supplies, supporting input signal levels as high as +22 dBu (at 5.6dB gain, and ±17V supplies) in combination with the 1570 (without an external input pad). The 5171 includes a differential servo and zero-crossing detector to minimize dc offsets and glitches (zipper noise) during gain adjustments.

The 5171 is controlled via an addressable serial-peripheral interface (SPI) port. Four General Purpose Outputs (GPOs) can be controlled via this interface. The GPOs may be connected to input pads, analog switches, mute circuits, LEDs, etc. The SPI bus supports read-back so that host software can verify proper operation.

The 5171 was designed to mate perfectly with the THAT 1570 Differential Audio Preamplifier IC. Together, these two ICs provide a best-of-class solution for digitally-controllable audio preamplifier applications. However, for designers who prefer a more customized solution, the 5171 may also be used to control a discrete preamplifier.

Fabricated in a high-voltage CMOS process, the 5171 integrates an astonishing amount of circuitry within a very small package. It comes in a small (7x7 mm) 32-pin QFN package, making it suitable for small portable devices.

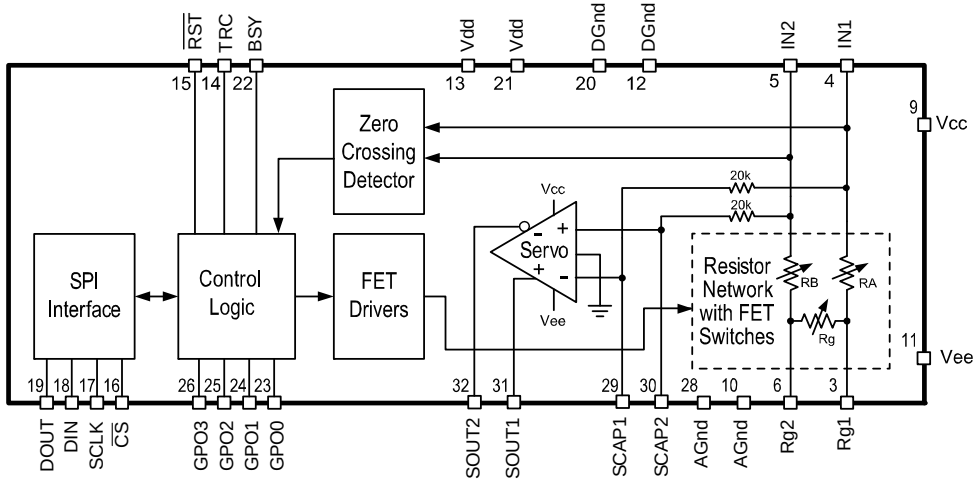


Figure 1. THAT 5171 Block Diagram

THAT Corporation; 45 Sumner Street; Milford, MA 01757-1656; USA
Tel: +1 508 478 9200; Fax: +1 508 478 0990; Web: www.thatcorp.com

Copyright © 2014, THAT Corporation Document 600133 Rev 08

Pin Number	Pin Name	Pin Description
1	NC	No Connect
2	NC	No Connect
3	RG1	Attenuator Network Output 1 [Connects to preamplifier feedback 1 (RG1)]
4	IN1	Attenuator Network Input 1 [Connects to preamplifier output 1]
5	IN2	Attenuator Network Input 2 [Connects to preamplifier Output 2]
6	RG2	Attenuator Network Output 2 [Connects to preamplifier feedback Input 2 (RG2)]
7	NC	No Connect
8	NC	No Connect
9	VCC	Positive Analog Supply Voltage
10	AGND	Analog Ground Reference
11	VEE	Negative Analog Supply Voltage
12	DGND	Logic Ground Reference
13	VDD	Logic Positive Supply Voltage
14	TRC	R/C Timeout or External Clock Input
15	RST'	Reset Input (Active Low)
16	CS'	Chip Select Input (Active Low)
17	SCLK	Serial Clock Input
18	DIN	Serial Data Input
19	DOUT	Serial Data Output
20	DGND	Logic Ground Reference
21	VDD	Logic Positive Power Supply
22	BSY	Busy Output (Active High)
23	GPO0	During Reset: SPI address bit 0 input; During run time: General Purpose Output 0
24	GPO1	During Reset: SPI address bit 1 input; During run time: General Purpose Output 1
25	GPO2	During Reset: SPI address bit 2 input; During run time: General Purpose Output 2
26	GPO3	General Purpose Output 3
27	NC	No Connect
28	AGND	Analog Ground Reference
29	SCAP1	DC Servo Capacitor Input 1
30	SCAP2	DC Servo Capacitor Input 2
31	SOUT1	DC Servo Output 1
32	SOUT2	DC Servo Output 2
Thermal Pad	PAD	Connected internally to Vee. Solder to PCB (optionally connect to Vee) for optimal performance.

Table 1. Pin Assignments

Copyright © 2014, THAT Corporation; All rights reserved.

SPECIFICATIONS[1]

Absolute Maximum Ratings[2,3]

Total Analog Supply Voltage (V_{CC}-V_{EE})	36 V	Minimum Analog Voltage at IN1, IN2 (V_{IAMin})	V_{EE}
Positive Analog Supply Voltage (V_{CC}-A_{GND})	18 V	Maximum Digital Input Voltage (V_{IDMax})	V_{DD} + 0.3 V
Negative Analog Supply Voltage (V_{EE}-A_{GND})	-18 V	Minimum Digital Input Voltage (V_{IDMin})	D_{GND} - 0.3 V
Digital Supply Voltage (V_{DD}-D_{GND})	4.5 V	Storage Temperature Range (T_{STG})	-40 to +125 ºC
Analog and Digital Ground Difference (D_{GND}-A_{GND})	±0.3 V	Operating Temperature Range (T_{OP})	-40 to +85 ºC
Maximum Analog Voltage at IN1, IN2 (V_{IAMax})	V_{CC}	Junction Temperature (T_{JMAX})	+125 ºC
Maximum Current Through V_{DD}, D_{GND}	100 mA		

Electrical Characteristics[2,4]

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Power Supply						
Analog Supply Voltage	V_{CC}; -V_{EE}	Referenced to A_{GND}	4.75	—	17	V
Digital Supply Voltage	V_{DD}	Referenced to D_{GND}	3.0	—	3.6	V
Analog Supply Current	I_{CC}; -I_{EE}	No Signal	—	8.3	11	mA
Digital Supply Current	I_{DD}	No Signal	—	2	11	µA
Resistor Ladder Characteristics (DC)						
Gain Range [-20 log (V_{IN1}-V_{IN2})/(V_{RG1}-V_{RG2})]		V_{CC} -1.6 > V_{IN1} >V_{EE}+1.6 V_{CC} -1.6 > V_{IN2} >V_{EE} +1.6	5.6	—	68.6	dB
Gain Step Size		13.6dB ≤ Gain ≤ 68.6dB	—	1	—	dB
Gain Error		All gain settings	-0.5	±0.15	0.5	dB
R_G Range (Resistance from IN_1 to IN_2)		All gain settings	4.5	5.6~1.41k	1.69k	Ω
R_A, R_B Range (Resistance from IN_1 to Rg_1) (Resistance from IN_2 to Rg_2)		All gain settings	2.1	2.65~7.5	9	kΩ
Servo Amp Characteristics (DC)						
Input Offset Voltage	V_{OS}	Includes bias current effects	-1.6	—	+1.6	mV
Power Supply Rejection Ratio	PSRR	V_{CC} = -V_{EE}; ±5V to ±15V	100	115	—	dB
Maximum Output Voltage	V_{OMax}		V_{CC}-4.5	—	—	V
Minimum Output Voltage	V_{OMin}		—	—	V_{EE}+4.5	V
Maximum Output Current	I_{OMax}		0.70	1.0	—	mA

1. All specifications are subject to change without notice.
2. Unless otherwise noted, T_A=25ºC, V_{CC}=+15V, V_{EE}= -15V, V_{DD}= +3.3V
3. Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only; the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not impli ed. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
4. 0 dBu = 0.775 Vrms

Copyright © 2014, THAT Corporation; All rights reserved.

Electrical Characteristics (con't)[1,3,4]

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Zero-Crossing Detector Characteristics (DC)						
Zero-Crossing Detector Threshold			—	±5	—	mV
ZCD Timeout	t_{ZTO}	R_T = 22MΩ, C_T = 1 nF	—	22	—	ms
ZCD Timing Capacitor	C_T			1	2	nF
ZCD Timing Resistor	R_T		1k	22M	100M	Ω
AC Characteristics						
THD+N (Differential signal applied tof = 1 kHz, Gain = 21.6 dB, IN_1, IN_2, measured at RG_1, RG_2) V_{IN1} - V_{IN2} = < +22 dBu			—	0.0003	—	%
Maximum Signal Voltage at IN_1, IN_2			—	V_{CC} - 2.5	—	V
Minimum Signal Voltage at IN_1, IN_2			—	V_{EE} + 2.5	—	V
Maximum Signal Voltage at RG_1, RG_2			—	V_{CC} - 2.5	—	V
Minimum Signal Voltage at RG_1, RG_2			—	V_{EE} + 1.5	—	V
Digital I/O Characteristics						
High-Level Input Voltage	V_{IH}		.7*V_{DD}	—	V_{DD} + 0.3	V
Low-Level Input Voltage	V_{IL}		-0.3	—	0.3*V_{DD}	V
High-Level Output Voltage	V_{OH}	I_O = 4 mA	.8*V_{DD}	—	—	V
Low-Level Output Voltage	V_{OL}	I_O = -4 mA	.	——	0.4	V
High-Level Output Current	I_{OH}		—	4	25	mA
Low-Level Output Current	I_{OL}		—	-4	-25	mA
Input Leakage Current	I_{IN}		—	2	10	µA
Serial Clock (SCLK) Characteristics						
Frequency	f_{SCLK}		0	—	10	MHz
Pulse Width Low	t_{PL}		40	—	—	ns
Pulse Width High	t_{PH}		40	—	—	ns
Input Timing						
DIN Setup; Hold Time	t_{SDS}, t_{SDH}		15	—	—	ns
CS Falling to SCLK Rising; SCLK Falling to CS Inactive	t_{CSCR} t_{CFCS}		50	—	—	ns
CS Inactive to SCLK Rising	t_{CICR}		100	—	—	ns
RST Hold Time	t_{RST}		50	—	—	ns
TRC Hold Time	t_{TRC}		50	—	—	ns
Output Timing						
SCLK Rising to D_{OUT} Active	t_{CRDA}		5	—	10	ns
SCLK Falling to D_{OUT} Data Valid	t_{CFDO}		—	—	15	ns
CS Inactive to D_{OUT} High Impedance	t_{CSZ}		5	—	20	ns

Copyright © 2014, THAT Corporation; All rights reserved.

Theory of Operation

The THAT 5171 is a gain controller in the form of a digitally controlled differential attenuator; it is not an amplifier. It contains a set of precision resistors, switched by a set of CMOS FET switches, configured to create a variable, switched, differential attenuation network. The network's impedances are ideal for controlling gain in low-voltage-noise, current-feedback instrumentation amplifiers, and are optimized for low source impedance applications. For example, when coupled with a low-noise gain stage like the THAT 1570, it maintains 1.5nV/√Hz noise floor at 68.6dB gain in the complete circuit.

Using the 5171

The attenuator is intended primarily for use in the feedback loop of differential current-feedback gain stages, such as the THAT 1570. Designed specifically for use in high-performance microphone preamplifiers, THAT's engineers paid careful attention to precision, stability, and control over the resistors and their switches, in order to maintain excellent audio performance over a wide range of gains and signal levels.

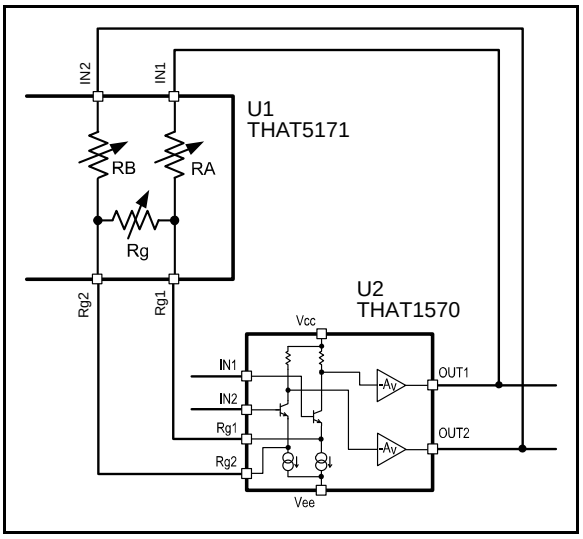


Figure 2. Analog portion of 5171 connected to a 1570.

Figure 2 shows the analog portion of the 5171 connected to a 1570. Resistors R_A, R_B, and R_G form a differential attenuator ("U-pad"). The 1570's differential output is applied to R_A and R_B. The output of the attenuator, appearing across R_G, is connected to the inverting differential input of the dual current-feedback amplifiers in the 1570 (the R_{G1} and R_{G2} pins). The voltage divider ratio thus controls the differential gain of the circuit.

The 5171 changes the attenuator settings based on the gain command provided via the SPI control interface. At minimum gain, R_G is ~7.93kΩ, while $R_A = R_B$ = ~3.56kΩ, which sets the circuit gain to +5.6dB. To achieve other gains, all three resistors are varied by CMOS switches in order to produce 1dB gain steps from +13.6 to +68.5dB. At all gains, the impedance levels are chosen to minimize noise and distortion within the circuit as a whole.

Table 2 lists the typical internal attenuator resistor values for each gain setting.

Gain Setting	Rg (ohms)	Ra, Rb (ohms)	"Gain" Register
5.6	7.9k	3.6k	0
13.6	1.4k	2.7k	8
14.6	1.4k	3.1k	9
15.6	1.4k	3.5k	10
16.6	1.4k	4.0k	11
17.6	1.4k	4.6k	12
18.6	1.4k	5.3k	13
19.6	1.4k	6.0k	14
20.6	1.4k	6.8k	15
21.6	560	3.1k	16
22.6	560	3.5k	17
23.6	560	3.9k	18
24.6	560	4.5k	19
25.6	560	5.0k	20
26.6	560	5.7k	21
27.6	560	6.4k	22
28.6	560	7.2k	23
29.6	220	3.2k	24
30.6	220	3.7k	25
31.6	220	4.1k	26
32.6	220	4.6k	27
33.6	220	5.2k	28
34.6	220	5.9k	29
35.6	220	6.6k	30
36.6	220	7.4k	31
37.6	89	3.3k	32
38.6	89	3.7k	33
39.6	89	4.2k	34
40.6	89	4.7k	35
41.6	89	5.3k	36
42.6	89	5.9k	37
43.6	89	6.7k	38
44.6	89	7.5k	39
45.6	35	3.3k	40
46.6	35	3.8k	41
47.6	35	4.2k	42
48.6	35	4.7k	43
49.6	35	5.3k	44
50.6	35	6.0k	45
51.6	35	6.7k	46
52.6	35	7.5k	47
53.6	14	3.4k	48
54.6	14	3.8k	49
55.6	14	4.2k	50
56.6	14	4.7k	51
57.6	14	5.3k	52
58.6	14	6.0k	53
59.6	14	6.7k	54
60.6	14	7.5k	55
61.6	5.6	3.4k	56
62.6	5.6	3.8k	57
63.6	5.6	4.2k	58
64.6	5.6	4.7k	59
65.6	5.6	5.3k	60
66.6	5.6	6.0k	61
67.6	5.6	6.7k	62
68.6	5.6	7.5k	63

Table 2. Internal attenuator resistor values.

Copyright © 2014, THAT Corporation; All rights reserved.

Maximizing Dynamic Range

The gain (actually attenuation) settings in the 5171 were chosen after careful consideration of the dynamic range available from the 1570 and similar designs. In particular, the unusual choice of 5.6dB was based on the available output headroom plus our objective to preserve as much dynamic range as possible. This led us to eschew the "round number" of 6.0dB; while the round number would make for simpler calculations, it would have compromised dynamic range by ~0.5dB.

We anticipate that in almost all cases, the 5171/1570 combination will be followed by one of two things. First would be an attenuator network which drops the +26.6dBu max (differential) output level (assuming ±15V rails) to one compatible with the input of an A/D converter. Alternatively, there might be an attenuating differential amplifier which converts the circuit's differential output to single-ended. In either case, nice "round" numbers for the system gain are easily achieved by changing the analog attenuation in these networks. See DN140 "Input and Output Circuits for THAT Preamplifier ICs" for circuits and ideas.

Accommodating High Signal Levels

One key objective of the 5171 design was to accommodate full professional-audio signal levels. Accordingly, it is fabricated in a high-voltage CMOS process which allows operation from up to ±17V analog power supplies. Along with proprietary (and patent-pending) drive circuitry to the switching FETs, this permits low-distortion operation at signal levels up to over +22dBu in, and nearly +27dBu out. See also DN140 for more discussion and ideas.

Switching Noise

The 5171 includes several features which minimize switching noise during gain changes. Special (patent pending) circuitry slows down the FET gate drive to minimize charge injection. This helps suppress clicks when changing gain. As well, the FET switches are implemented in a balanced fashion so as to maintain equal perturbation to the positive and negative sides of the balanced signal path.

A built-in zero-crossing detector can be used to restrict gain changes to times when the analog signal is very close to zero. The detector monitors the differential signal present between the IN_1 and IN_2 pins of the 5171. When enabled, it permits gain changes to take place only when the signal is within ±5mV. A timeout (set by external components R_T and C_T in figures 3~6) ensures that a gain change will always occur at the expiration of the timeout, in case the signal has not gotten within the voltage window by that time.

The period of a 20Hz waveform is 50ms and thus zero-crossings will occur every 25ms. Accordingly, THAT recommends that the timeout be set to less than or equal to 25ms in order to ensure that gain changes will be made at zero-crossings unless there is some unusual low-frequency signal present. 22mS is the time constant shown in the application schematics. Of course, for special applications, the designer may choose to disable the zero-crossing detection and force immediate gain changes without regard to the signal condition.

With the zero-crossing feature enabled, gain changes are very quiet – barely audible when performed in the absence of program, and all but inaudible with program material present.

Servo and DC Offsets

The 5171 also includes an integrated differential servo amplifier which minimizes dc offset at the output. Practically, it is impossible to ensure that the input offset voltage of the analog gain stage is low enough to maintain low output dc offset at high gains. (For <10mV output offset, the input offset at ~60dB gain would have to be under 10µV!) On the other hand, it is not too difficult to make amplifiers with under 1.5mV input offset. By using such an amplifier in feedback around the analog gain stage, it is possible to generate a correction voltage that maintains low output offset from the circuit as a whole.

The integrated differential servo amplifier has under 1.5mV input offset voltage. It requires two large non-polar capacitors in feedback around each half of the amp to form an integrator. The integrator's input is connected to the gain stage's output, and the integrator's output is applied to the gain stage's input. As the loop settles, the gain stage's output will be driven to the input offset voltage of the servo. The loop time constant must be set long enough so as not to interfere with low audio-frequency signals.

The combination of the input coupling capacitors (C_4 and C_5 in Figures 3~6), the bias resistors for the 1570 (R_1 and R_2 – which form a load for C_4 and C_5), and the servo, form a 2nd order highpass filter whose characteristics change with the gain setting. The Q of this filter is highest at the highest gain setting. (At low gains, the behavior is governed almost entirely by the input coupling network and bias resistors, since the poles split and the one related to the servo moves very low.) Assuming 1.2kΩ for R_1 and R_2, and 1.2MΩ for R_7 and R_8, we can set the highest Q to be about .87 (for approximately Butterworth response) if we choose C_{12} and C_{13} to be 1/5 the values of C_4 and C_5.

We recommend a 1000:1 ratio between servo feed resistors (R_7 and R_8) to the analog gain stage bias resistors (R_1 and R_2) to minimize any noise contribution from the servo amp. Reducing R_7 and R_8 will lower the Q, while increasing them will raise the Q, proportional to the square-root of resistance.

Mathematically, we can express the cutoff frequency, f_o, and the Q as:

$$f_o = \frac{1}{2\pi\sqrt{\frac{1}{G}\,R_7\,20k\Omega\,C_4C_{13}}}, \text{ and}$$

$$Q = \frac{1}{2\pi f_0 \frac{1}{G} 20k\Omega\,C_{13}\,K}, \text{ where G is the preamp}$$

gain, $K=1+(R_7/R_1)$, $R_1=R_2$, $R_7=R_8$, $C_4=C_5$, $C_{12}=C_{13}$, and the source impedance is less than 1kΩ.

Copyright © 2014, THAT Corporation; All rights reserved.

While the servo is effective at minimizing dc offset at the outputs, it does require time to react. When gain is changed, particularly if a sudden large increase in gain is initiated (e.g., 5.6dB to 68.6dB), the servo output will not change instantaneously with the gain change. Immediately after the gain increase, the servo will be supplying a dc offset appropriate for the lower gain, and the dc at the output will thus change, on a transient basis, to a higher level. As the servo acquires the new required value, the dc offset will be driven down to under 1.5mV.

To minimize the sonic impact of the dc offset change, THAT recommends that gain be increased slowly by sending many commands to the 5171 that increase gain a few dB at a time, over a second or more of total time. This replaces the one big change in dc offset with a series of much smaller ones, allowing the servo some time to settle (at least partially) in between each step. Note that the problem is much less audible during stepwise decreases in gain, since the servo's output is not amplified as much at the new (lower) gain as it was at the previous one.

Control Interface

The 5171 includes an addressable serial-peripheral interface (SPI) port to accept external gain commands. The SPI inputs accept 3.3V logic levels. The 5171 address is established during reset by resistors or other appropriate loads connected to the first three general-purpose outputs (GPOs 0 through 2). During reset, these serve as inputs only for programming the device's three-bit address. Addresses from 0 through 7 (binary) are accepted.

The GPO3 is reserved as an input for future applications. To ensure compatibility with future revisions of the 5171, ensure that GPO3 is tied to a logic level of 0 during reset.

The SPI interface may be clocked at speeds of up to 10MHz.

As just mentioned, the 5171 offers four general purpose outputs (the fourth one is not used for chip addressing). These provide 3.3V logic signals to drive whatever a designer may require.

Copyright © 2014, THAT Corporation; All rights reserved.

Applications

While the 5171 is perfectly suitable for application to discrete current-feedback differential preamplifiers, the applications discussed herein are exclusively based on use with the companion THAT1570 IC. This part provides the essential low-noise, current-feedback, differential analog gain stage whose gain the 5171 can control.

The circuit of Figure 3 shows the most basic application of the 5171 and 1570 to form a complete low-noise microphone preamplifier.

Gain Ranges in Basic Configurations

The circuit of Figure 3 offers differential gain that varies from 5.6 to 68.6dB. There is one large ~8dB step from 5.6dB to 13.6dB. Above 13.6dB, gain may be controlled in 1dB steps to +68.6dB. For single-ended analog outputs, the circuit of Figure 3 can be followed by a differential-to-single-ended converter, as shown in Figure 4. Here, the differential amplifier is configured for -5.6dB gain in order to minimize noise and maximize headroom at the output of the circuit. Including the 5.6dB attenuation in the differential amplifier, the system gain can be set to 0dB, or any gain from +8dB to +63dB in 1dB steps.

At minimum system gain (0dB) and with ±15V supply rails, the maximum (differential) input signal level is +21dBu, and the maximum (differential) output signal level (at the OUT_1 and OUT_2 pins of the 1570) is +26.6dBu. At maximum system gain (+63dB), the maximum input signal level is -42dBu, and the maximum output signal level remains +26.6dBu. All these figures increase by a little over 1dB if the circuit is run from ±17V supplies.

With the circuit of Figure 4, the maximum input signal levels remain the same, but the (now single-ended) output levels drop by 5.6dB due to the loss of the differential amplifier. When converting to single-ended signals, take care to select a low-noise opamp, and pay attention to the noise generated by the impedances. The component values shown in Figure 4 will largely preserve the dynamic range of the 1570 and 5171 combination, though they do compromise noise by 1dB at the lowest gain settings.

For many applications, the output of the microphone preamplifier must drive an analog-to-digital converter. Most high-performance A/D converters have differential inputs, and cannot accept differential signals greater than ~+8dBu. For such applications, the output of the mic preamp must be attenuated to prevent overload of the A/D converter. The circuit of Figure 5 shows one typical circuit, using a simple resistive attenuator (R_9 through R_{11}). The impedance levels of the attenuator are chosen to minimize their self-generated voltage noise, and to stay within the load limits of the 1570 which drives them. Figure 5 assumes that the maximum differential input to the A/D converter is +8dBu. For higher

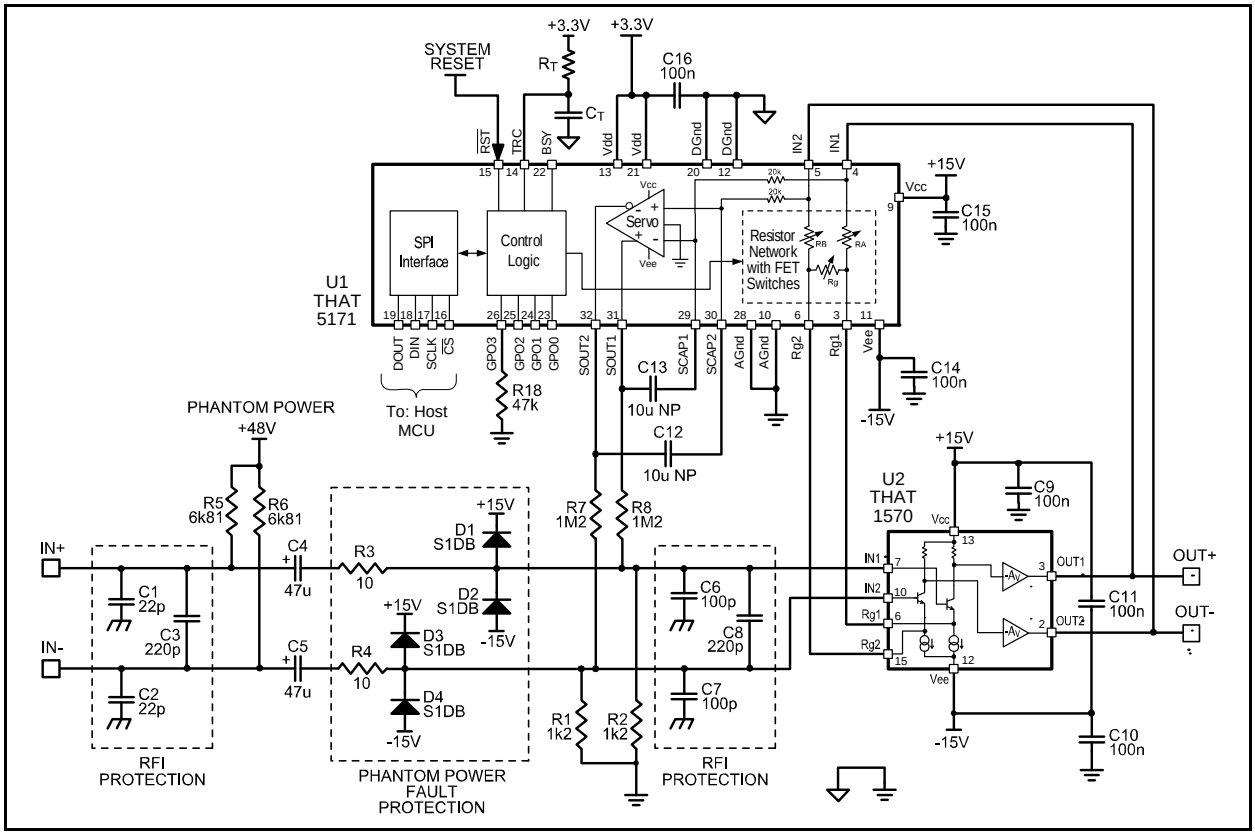


Figure 3. 5171/1570 basic application circuit.

Copyright © 2014, THAT Corporation; All rights reserved.

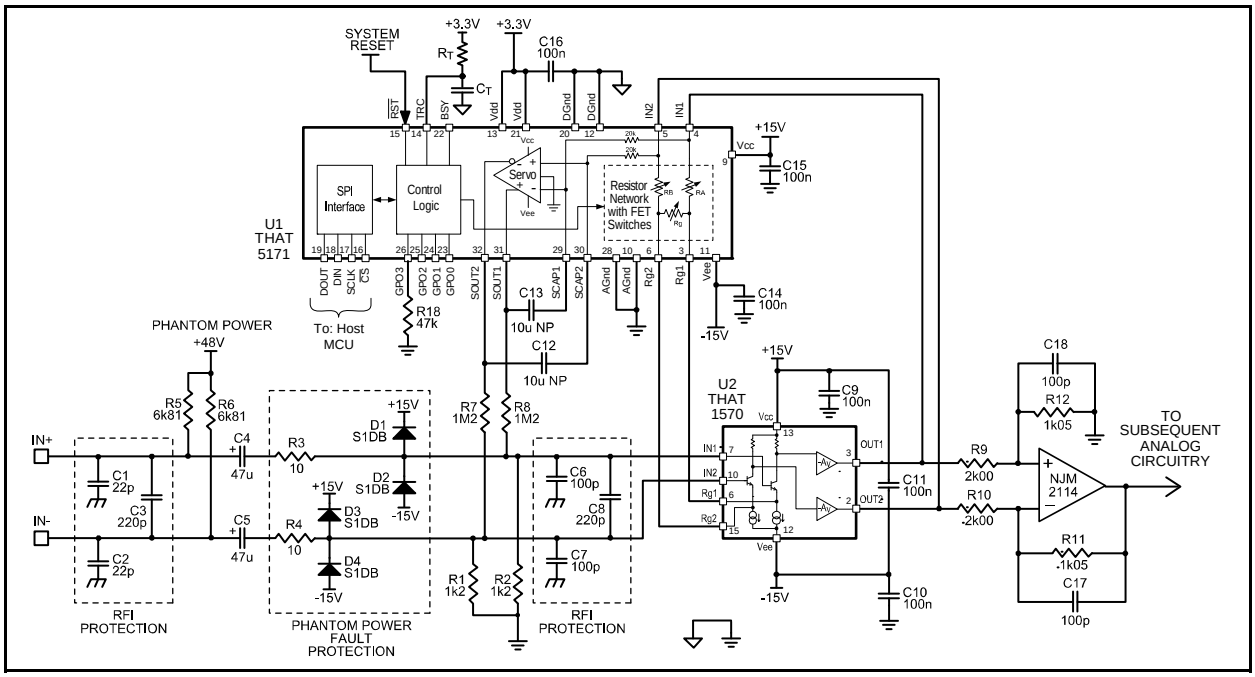


Figure 4. 5171/1570 typical application with single-ended output.

(or lower) maximum input levels, or for different supply voltages to the 1570 and 5171, scale the attenuator accordingly, keeping its total impedance ($R_9 + R_{10} + R_{11}$) the same. In this circuit, the noise at the A/D converter input (across R11) is -120.5dBu (in a 20kHz bandwidth). This compromises the theoretical noise floor of the 1570/5171 (at minimum gain) by about 0.65dB. However, the non-zero impedance drive to the converter may increase distortion with high-performance converters. The impact of this impedance depends on the ADC.

Note that one drawback of the circuit shown in Figure 5 is that it offers no common-mode rejection. The 1570 has unity common-mode gain regardless of

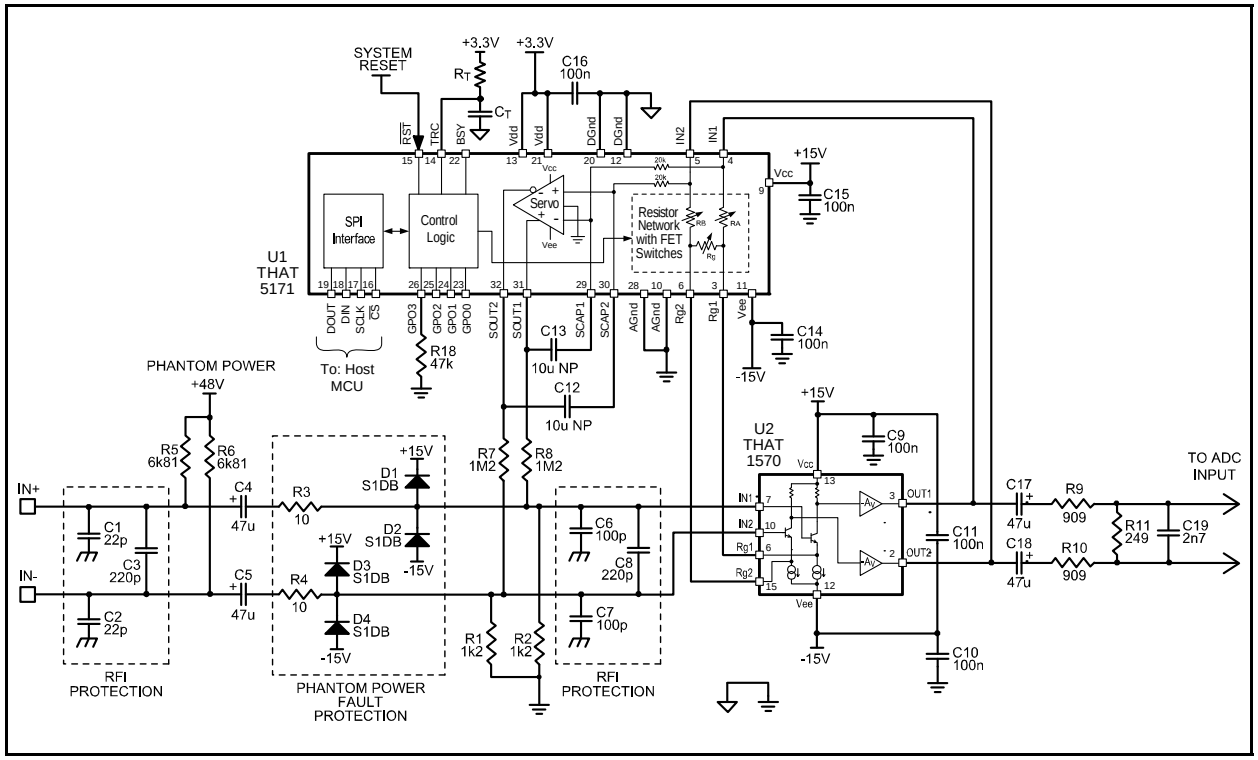


Figure 5. 5171/1570 low-cost application for output to an A/D convertor.

Copyright © 2014, THAT Corporation; All rights reserved.

its differential gain, as does the passive attenuator shown in Figure 5. This circuit 5 relies entirely upon the A/D converter's common-mode rejection.

For better distortion performance with high-quality A/D converters, and to improve common-mode rejection, consider circuits like the one in Figure 6. The active (buffered) attenuator provides differential drive to the ADC, which improves performance. Note, however, that noise in the 2114 opamps shown will compromise the performance of the 5171/1570 combination by ~3dB at minimum gains, so choose the active devices for low noise as well as good audio performance.

RFI Protection (and Common-Mode Rejection)

The circuits of Fig 3 through 6 include RFI protection in two sections. Small capacitors (C_1 and C_2) are used from the positive and negative signal inputs to chassis ground, along with a larger capacitor (C_3) across the two inputs. These components should be located as close as possible to the input signal connector, and are intended to prevent RF from entering the chassis of the device.

A second RF protection network is located close to the 1570, and is intended to prevent any RF picked up inside the unit from reaching the 1570's input, where it might be rectified and cause audio-band interference. This network consists of a pair of larger capacitors (C_6 and C_7) to ground and one more capacitor (C_8) across the two input lines. If RF is prevented from entering the unit, and none is generated inside the unit, then these capacitors may be omitted or reduced in value.

The design of these networks was arrived at after some consideration for common-mode rejection. Unbalanced capacitance from either input line (IN+ or IN-) to ground can unbalance common-mode signals, converting them to differential signals, which will be amplified along with the desired (differential) signal. The 1570 differential amplifier in the above circuits offers gain only to differential signals: common-mode signal gain is always 0dB. Therefore, its common-mode rejection is equal to the differential gain.

So long as common-mode signals are not converted to differential ones, this common-mode rejection will prevail. Because they are relatively small, differences in the values of C_1 and C_2 are less likely to cause imbalance than the larger capacitors at C_6 and C_7. For this reason, we recommend that capacitors C_6 and C_7 should be at least 5% types, in order to ensure matching between their values. Note that C_3 and C_8 affect only differential signals, and thus do not affect common-mode rejection.

Power Supply Decoupling

Power supply decoupling is required for stability of the 1570, the servo in the 5171, and to minimize digital switching noise from propagating on the power supplies. The V_{CC} and V_{EE} pins should be connected to the same analog supply which powers the analog gain stage, while the V_{DD} pins (13 and 21) may be powered in common with other logic circuitry (microprocessors, etc.) in the unit.

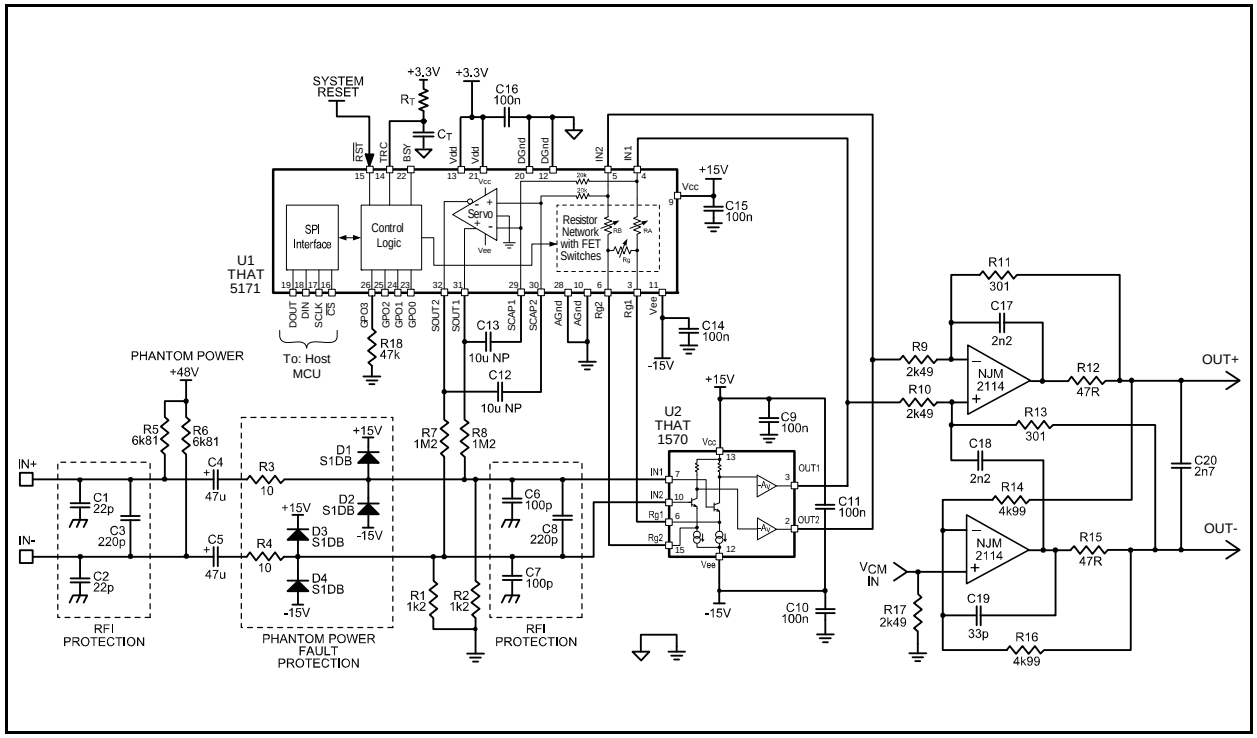


Figure 6. 5171/1570 high-performance application for output to an A/D convertor.

Copyright © 2014, THAT Corporation; All rights reserved.

THAT recommends one decoupling capacitor (C_{16}) for the digital power supply, placed close to pins 20 (D_{GND}) and 21 (V_{DD}), as these pins connect to the digital output driver bus. Pins 12 (D_{GND}) and Pin 13 (V_{DD}) should be connected to pins 20 and 21, respectively, through short, low-inductance paths.

A_{GND} and D_{GND} should be connected together directly under the 5171. Note that the part includes back-to-back diodes limiting the maximum voltage difference between these nodes. If even on a transient basis (e.g., supply spikes) a voltage difference of over 0.5 V exists between A_{GND} and D_{GND}, large currents will flow which may damage the part.

As described above (in the Theory section), the integrated differential servo is required for proper operation of the system as shown in the application schematics. By using the servo amplifier in feedback, output offset can be controlled over a wide range of gains.

In order to optimize settling behavior, THAT recommends that C_{12} and C_{13} be approximately one-half the size of C_4 and C_5. As well, to avoid the servo from contributing noise to the preamplifier, we recommend that the servo's output be divided down by approximately 1000:1 by the combination of R_7/R_1 and R_8/R_2.

Zero Crossing Detector

The integrated zero-crossing detector may be enabled or disabled. (See the digital control section below for details.) When enabled, it prevents gain changes from occurring until the differential output signal waveform is within ±5mV of zero. It is possible that in unusual cases where significant low-frequency material is present, the zero-crossing detector may unacceptably delay a gain change from taking place. A timeout, set by R_T and C_T, is provided to force a gain change to occur within R_TC_TmS of the time it is requested, even if zero crossing is enabled.

Digital Control

Reset (RST pin)

Asserting the RST pin low forces all internal registers to their default state (see register definitions in SPI Port section for default values after reset). This pin is typically connected to system reset or to a port on the host microcontroller.

During reset, the 5171 reads the 3-bit SPI address via the GPO[2:0] pins. These pins are typically connected to pull-up and pull-down resistors to establish the chip address, and serve as general purpose outputs during runtime. THAT Corporation intends to offer features in future versions of the 5171 that will be configured via a pull up resistor on GPO3. Thus, GPO3 should be pulled low by a resistor of 100 kΩ or less on early designs before these new features become available.

Busy (BSY pin)

The BSY pin is asserted high when the current gain setting is not equal to the value in the GAIN register, i.e. when a gain update is pending a zero-crossing. This pin may be monitored by the host microcontroller (e.g. connected to an external interrupt pin) in order to hold off a new gain command until the previous gain command has been executed.

Note that in ZERO-CROSSING mode, the BSY pin goes low when a pending gain change has been made. If finer gain steps are implemented in subsequent processing (typically via DSP) this signal can be used to assist in synchronizing subsequent gain changes with those implemented by the 5171. Note, of course, that latency in A/D conversion must be considered when attempting to synchronize digital with analog gain updates.

Gain Update Modes (and TRC pin)

The 5171 supports two gain update modes, selected by the MODE bits in the Control/Status Register (Table 13), as follows.

1) **IMMEDIATE Mode**: Gain updates are made immediately following a rising edge on the /CS pin.

2) **ZERO-CROSSING Mode:** Updates are made on the next output signal zero-crossing after a rising edge on the /CS pin. An RC time constant connected to the TRC pin (R_T/C_T in Figures 3~6) establishes a time-out period in case a zero-crossing does not occur within a desired time window. The zero-crossing time-out function operates as follows:

Signal	Pin	I/O	Function
$\overline{CS}$	16	Input	Device chip select input, active low. An SPI transfer begins with a high-to-low CS transition and ends with a low-to-high CS transition. When CS is high, SCLK transitions are ignored. Zero-crossing timeout capacitor C_T is discharged when CS goes low.
SCLK	17	Input	SPI serial clock input. An SPI master supplies this clock with frequencies up to 10MHz. Data is clocked into the DIN pin on the rising edge of SCLK. Data is clocked out of DOUT pin on the falling edge of SCLK.
DIN	18	Input	SPI serial data input (Master-Out, Slave-In). DIN is MSB first.
DOUT	19	Output/Tristate	SPI serial data output (Master-In, Slave-Out). DOUT is a tristate output. DOUT is tristated when CS is high. DOUT is MSB first.

Table 3. SPI signals.

Copyright © 2014, THAT Corporation; All rights reserved.

A) C_T is discharged when /CS goes low (the beginning of an SPI command sequence), and is allowed to start charging when /CS goes high (the end of an SPI command sequence). Note that, for the case of multiple devices with a common chip select line, the fact that C_T is discharged when /CS goes low means that if one 5171 is waiting for either a zero-crossing or a timeout to occur when a gain update is sent to a second 5171, the timeout of the first device is cancelled. The gain of that device will then only be updated after a zero-crossing is detected or another gain update is addressed to that device. To avoid this, commands to multiple devices with the same chip select line should be spaced in time by an interval that exceeds the timeout period set by R_T and C_T (typically 22 msec). Alternatively, the BSY pins on the 5171s can be monitored. The BSY pin will go low as soon as a pending gain update is completed, indicating that it is safe to update the gain on another device.[5]

B) Gain is updated on the next zero-crossing or when the voltage on the TRC pin charges to $0.7*V_{DD}$ -- whichever event occurs first.

The recommended time constant for R_TC_T is ~22mS (e.g. C_T = 1nF and R_T = 22MΩ).

The choice between IMMEDIATE vs ZERO-CROSSING mode depends on the application. Immediate mode has the advantage of providing immediate gain updates with deterministic latency and the ability to synchronize updates between the mic preamp and subsequent signal processing (e.g. digital interpolation of finer steps in gain), whereas ZERO-CROSSING mode has the advantage of minimizing glitches and zipper noise.

Serial Peripheral Interface (SPI) Port

SPI Signals

The 5171 is a Slave device on the SPI bus (the microcontroller host is the Master). The SPI signals are listed in Table 3. Figure 7 and Table 4 show the SPI timing parameters.

The SPI protocol consists of 16-bit read and write commands (Figure 8). In a write operation, data is clocked into the DIN pin, MSB first, on the rising edge of SCLK.

In a read operation, address bits are clocked into the DIN pin, MSB first, on the rising edge of SCLK, and an 8-bit data word is clocked out of the DOUT pin, MSB first, on the falling edge of SCLK.

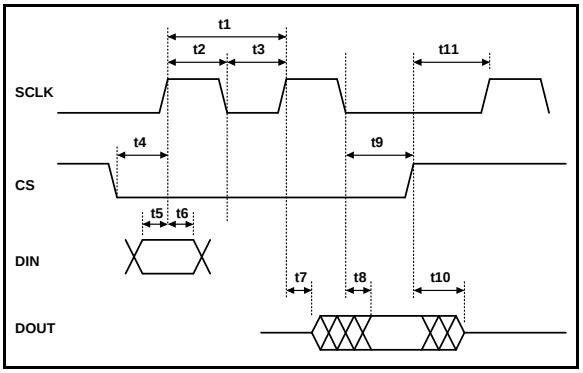


Figure 7. SPI Timing.

5. Thanks to Simon Jones of Focusrite for pointing out the importance of this issue.

SPI Command Format

SPI read and write commands are comprised of four bitfields, shown in Table 5. The 3-bit device

Param.	Description	Min	Max
t1	SCLK cycle time	100	-
t2	SCLK low time	40	-
t3	SCLK high time	40	-
t4	CS setup to SCK rising	50	-
t5	DIN setup time	15	-
t6	DIN hold time	15	-
t7	SCLK rising to DOUT out of tristate	5	10
t8	SCLK falling to DOUT valid	-	15
t9	SCLK falling to CS inactive	50	-
t10	CS inactive to DOUT tristate	5	20
t11	CS inactive to SCLK rising	100	-

Table 4. SPI timing parameters (ns).

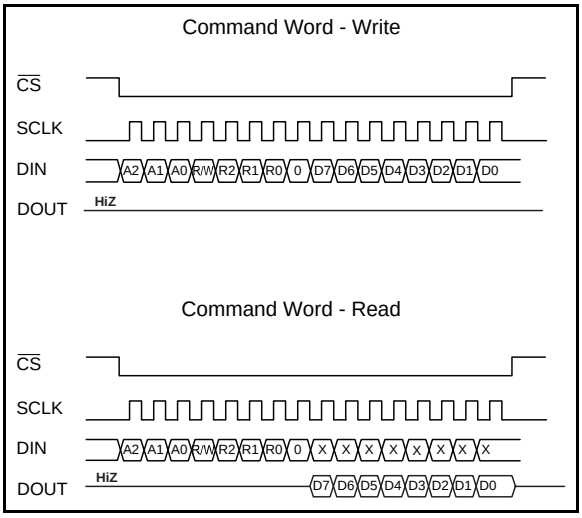


Figure 8. SPI command word formats (read and write). (See Table 5 for definitions of bitfields.)

Field	Function
A[2:0]	**Device address** During reset the GPIO[2:0] pins are read as inputs to establish the device address.
R/W	**Read/write control** R/W = 0 for read R/W = 1 for write
R[2:0]	**Register Address** Specifies which register within the 5171 will be read or written by the command.
D[7:0]	**Data** For R/W=1 this is the data to be written For R/W=0 the data is ignored

Table 5. SPI command format. (See Figure 8 for timing of the bits within these fields.)

Copyright © 2014, THAT Corporation; All rights reserved.

address, A[2:0], specifies which chip on the SPI bus is being targeted. The R/W bit specifies whether this command is a read (0) or write (1) operation. The 3-bit register address, R[2:0], specifies which register within the 5171 will be read or written. The data field, D[7:0], carries data for the command.

SPI Registers

SPI Read and Write commands access registers within the 5171. The registers and their addresses are listed in Table 6.

Register Address: R[2:0]	Function
000	CHIP ID
001	GAIN
010	GPO
011	CONTROL/STATUS
100 ~ 111	Reserved

Table 6. SPI Registers.

Chip ID Register (R[2:0] = 000)

The read-only Chip ID register identifies the chip version and revision. It consists of a 6-bit Chip code and a 2-bit Revision code, shown in Tables 7-9. The first version of the 5171 returns hex 0x84 (CHIPID = binary 100001; REV 00).

Bit #	7	6	5	4	3	2	1	0
Meaning	CH5	CH4	CH3	CH2	CH1	CH0	REV1	REV0
Type	RO	RO	RO	RO	RO	RO	RO	RO

Table 7. Chip ID Register.

CH[5:0]	Chip Field
100001	THAT5171 Digital Preamplifier Controller

Table 8. Chip ID.

REV[1:0]	Chip Revision
00	Revision 0
01	Revision 1
10	Revision 2
11	Revision 3

Table 9. Chip Revision.

Gain [5:0]	Gain Register Value (decimal)	Actual Gain (dB)
000000	0	5.6
000001	illegal	unchanged
000010	illegal	unchanged
000011	illegal	unchanged
000100	illegal	unchanged
000101	illegal	unchanged
000110	illegal	unchanged
000111	illegal	unchanged
001000	8	13.6
001001	9	14.6
...	...	...
111110	62	67.6
111111	63	68.6
RESET	0	5.6

Table 10. Gain Register.

Gain Register (R[2:0] = 001)

Gain of the 5171 is represented by the 6-bit GAIN register. The value of the GAIN register may be 0, or any value in the range 8 to 63 (decimal) as shown in Table 10. Note that read-only (RO) bits must be written as zeros. The actual gain setting is 5.6dB higher than the value in the GAIN register.

Values 1 to 7 are not allowed. If an illegal value is written to the GAIN register, the current gain setting will not be changed and the ERR bit in the CONTROL/STATUS register will be set until a valid value is written.

GPO Register (R[2:0] = 010)

The GPO register (Table 11) controls the state of the general purpose output pins. A logic 0 in any of the GPO[3:0] bits sets that port low. A logic 1 sets a port high. During reset, the GPO pins are configured as inputs and the device address is read on GPO[2:0]. THAT Corporation intends to offer features in future versions of the 5171 that will be configured via a pull up/down resistor on GPO3. To ensure compatibility with new versions of the chip, GPO3 should be pulled low with a 1-10 kΩ resistor on designs before these new features become available. After reset, the GPO pins are configured as outputs and are available for general use. Note that reading the GPO register returns the GPO[3:0] register bits, not the logic levels of the GPO pins during reset.

Bit #	7	6	5	4	3	2	1	0
Meaning	X	X	X	X	GPO 3	GPO 2	GPO 1	GPO 0
Type	RO	RO	RO	RO	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0

Table 11. GPO Register.

Control/Status Register (R[2:0] = 011)

The CONTROL/STATUS register controls the mode of the chip and returns current chip status. During a write to this register, the read-only bits must be written as zeros. The register fields are defined in Table 12, and the bitfields are described in Table 13.

Bit #	7	6	5	4	3	2	1	0
Meaning	BSY	Rsvd	ERR	Rsvd	Rsvd	Rsvd	Mode 1	Mode 0
Type	RO	RO	RO	RO	RO	RW	RW	RW
Reset	0	0	0	0	0	0	0	0

Table 12. Control/Status Register.

Copyright © 2014, THAT Corporation; All rights reserved.

Bit(s)	Description
MODE[1:0]	**Gain control mode** **00** - Immediate gain updates **01** - Gain update on zero crossings **10** - Reserved **11** - Reserved
Reserved	Unused
Reserved	Unused
Reserved	Unused
ERR	**Gain Error** **0** - No error **1** - Error If an illegal value is written to the GAIN register, it is ignored and the ERR bit is set until a valid gain value is written.
Reserved	Unused
BSY	**Busy** **0** - Not busy, the switched resistors have been updated by the value in the GAIN register **1** - Busy, a change to the switched resistors is pending a zero-crossing.

Table 13. Control/Status Register Bits.

Using the GPOs to Control Preamplifier Functions

While the General Purpose Outputs (GPOs) can be used to control any binary state functions, they are primarily intended to be used to control analog functions associated with a preamplifier. Figure 9 is a block diagram showing THAT 5171 GPO outputs controlling typical preamp functions such as an input pad (GPO0), mic/line switching (GPO1), signal polarity (GPO2), and phantom power (GPO3). There are many ways to control each of these functions, each with its own tradeoffs. See Design Note 140 ("Input and Output Circuits for THAT Preamplifier ICs") for basic circuit ideas on how to implement this control using relays.

Driving Relays from GPOs

Frequently, the switches which control analog functions will be relays. Relays will generally require a buffer to provide current to drive their coils without excessively loading the 5171.

Figure 10 provides examples of a discrete NPN buffer suitable to drive relays, and a discrete PNP buffer suitable to drive LEDs from the GPO outputs. (Of course, an NPN could be used to light an Led and a PNP to drive a relay, though the available voltage at the GPO pins may make it easier to drive a relay from an NPN driver.) Because the GPO pins are used as inputs for the device's SPI address during reset, the choice of buffer has an influence on the address which the 5171 will assume following reset.

Setting the SPI Address Via Hardware Design

If a hard-wired SPI address is appropriate for the application, the address may be set by choosing the polarity of buffer. During reset, NPN drivers provide the corresponding GPO with a low logic level ("0"), while PNP drivers provide a high logic ("1") condition. The difference in logic levels stems from the base-emitter junction and associated bias resistors acting as a pull-up (PNP) or pull-down (NPN) on each pin in its address-setting mode (during reset).

After reset, the GPO outputs are initialized to logic 0. With PNP buffers the immediate post-reset condition is On. If this is an undesirable condition the 5171 should be immediately initialized to the proper state by setting the corresponding GPO output to a logic 1 level.

Flexibility in SPI Address Setting with a Tri-State Buffer

Figure 11 shows a circuit using a 74LV125A tri-state buffer. This offers greater flexibility by making the SPI address independent of the load connected to the ultimate GPO outputs, shown at GPO'0~GPO'3.

Besides making the SPI address independent of buffer polarity, the tri-state buffer increases the output drive compared to that available from the 5171. One additional benefit of the circuit shown is that during reset, the buffers prevent the address-setting resistors from turning on circuitry connected to the GPO' connections. During reset, the GPO output buffers, sections A-D, are tri-stated by their output enable /OE. This is accomplished by complementing the /RST line using inverter E.

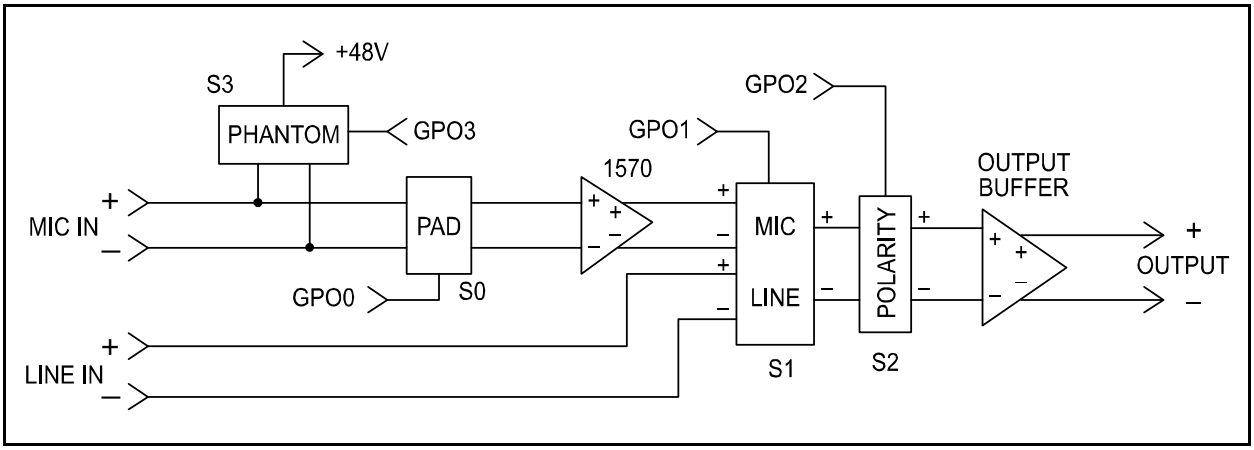


Figure 9. GPO outputs control preamp functions.

Copyright © 2014, THAT Corporation; All rights reserved.

The 5171 SPI address is set by pull-up or pull-down resistors R0A through R2B. In the example above the address is "101b" or "5d". The value of the pull-up resistors typically range from 4.7k to 47k.

Add R4B to Ensure Future Compatibility

In future revisions of the 5171, THAT has plans to use GPO3 as an input to set alternate SPI operation modes. To ensure compatibility with future versions of the 5171, current designs should include R3B.

Field Programming the SPI Address

If the SPI address must be field programmable, a combination of strong pull-up and weak pull-down may be used in conjunction with switches, links, or jumpers as shown in Figure 11 in the dotted box. In the above example the pull-up is 4.7kΩ, the pull-down is 47kΩ.

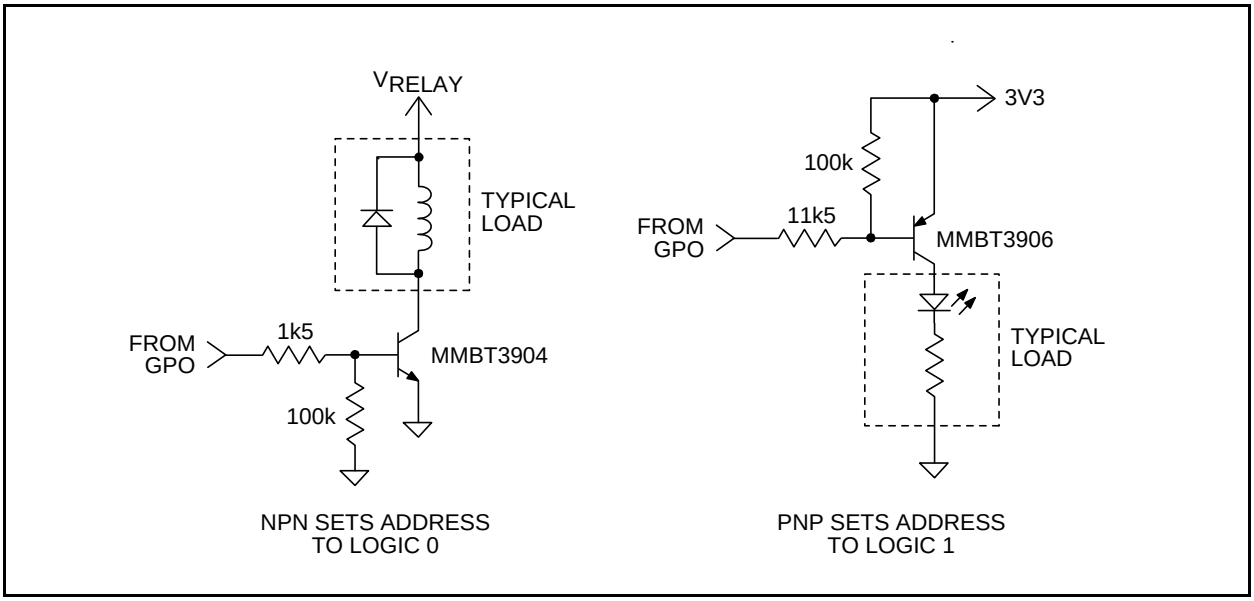


Figure 10. Output drivers polarity sets 5171 address during reset.

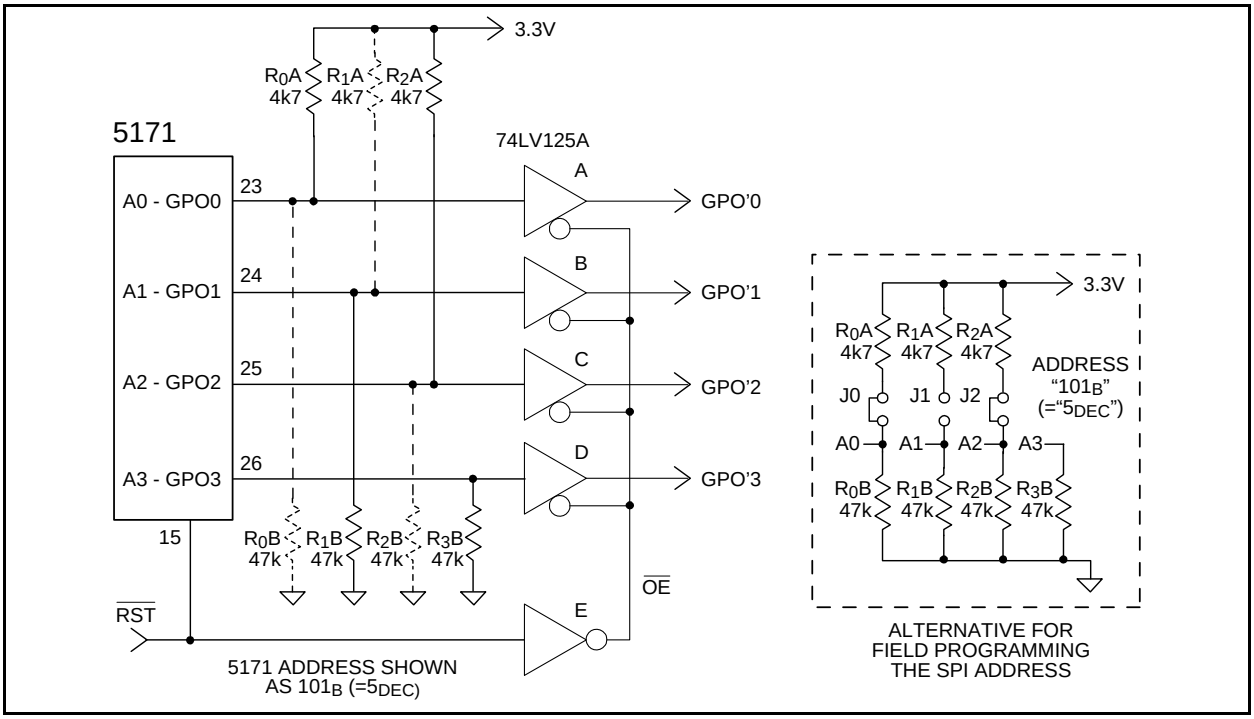


Figure 11. 5171 device addressing with buffered GPO outputs.

Copyright © 2014, THAT Corporation; All rights reserved.

SPI Bus Topologies

The 5171 SPI port is very flexible, supporting single-device and multiple-device applications and read-back of internal registers. Figures 12 through 14 show several common configurations. Note that the 5171 always operates as the SLAVE device on an SPI bus.

The configuration of Figure 13 allows read and write operations to be communicated to individual devices by addressing them individually. In order to send commands to multiple devices in parallel, see the configuration in Figure 14. This configuration supports parallel write operations to multiple 5171s with the same chip address when their chip selects are asserted together. Note that in this configuration, read operations can not be performed in parallel due to contention on DOUT.

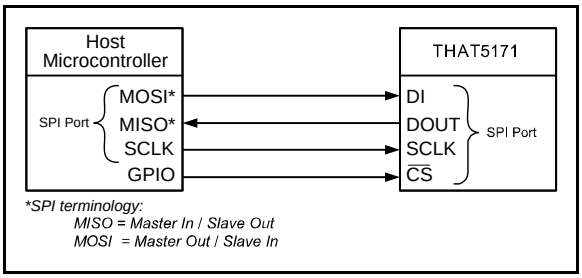


Figure 12. Single 5171 connected to a host microcontroller.

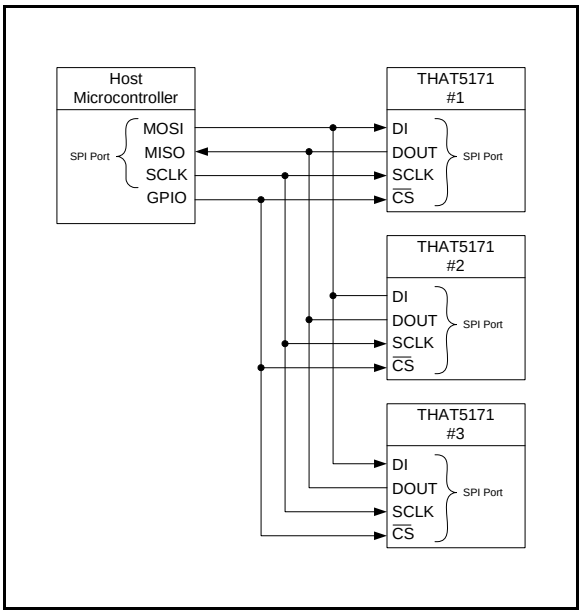


Figure 13. Multiple 5171 ICs connected in parallel to a host microcontroller.

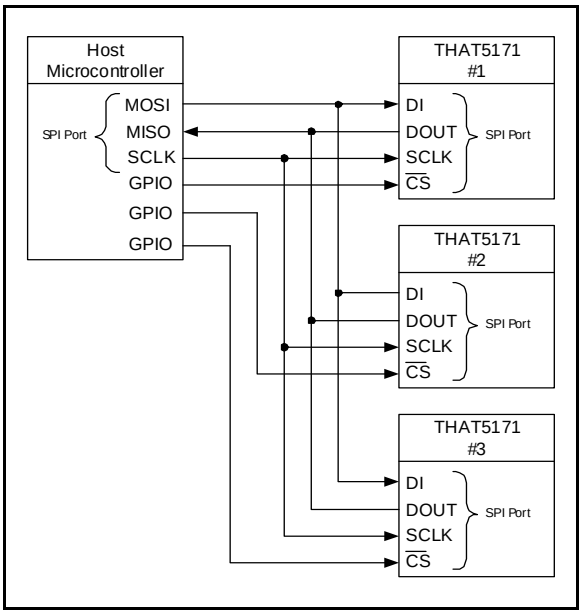


Figure 14. Multiple 5171 ICs connected in parallel to a host microcontroller, with independent chip selects.

Copyright © 2014, THAT Corporation; All rights reserved.

PCB Layout Information

The 5171 and 1570 are intended to lay out side-by-side, with pins 1 through 4 on the 1570 facing pins 1 through 7 on the 5171. See Figure 15 for a suggested layout.

Designers should take care to minimize capacitance on the Rg pins, and to ensure that power supply lines do not run close and/or parallel to either the input signal lines or the traces and pins connected to the Rg pins. For current feedback amplifiers such as the 1570, stray capacitance to ground or power planes results in higher gains at high frequencies. As a result, mismatches in the capacitance on these two nodes will degrade common-mode performance at high frequencies.

Additionally, power supply lines, which often carry non-linear (e.g., half-wave rectified) versions of the signal can magnetically and capacitively couple into the input and Rg lines. This can create distortion, particularly at high gains.

Therefore, THAT recommends avoiding ground plane under the IN_1 and IN_2 pins and associated traces. We also recommend a symmetrical PCB layout to match the capacitance on these nodes.

As is customary with QFN packages, we recommend that the metal "slug" on the bottom of the QFN package be soldered to provide physical attachment and improve thermal performance. The QFN's thermal resistance with the slug soldered to the PCB is not yet determined, but will be lower than the unsoldered resistance of 90° C/W. The slug may be left unconnected electrically, or connected to V_{EE}.

When laying out the board, we recommend following advice offered by Henry W. Ott in his recent book Electromagnetic Compatibility Engineering, published in August 2009 by Wiley (ISBN: 978-0-470-18930-6). In it, Mr. Ott recommends laying out the digital and analog ground scheme using ground planes as if they were separate planes, but do not actually separate them in the final design. As noted earlier, all bypass capacitors should be located very close to their respective power and ground pins. In particular, for the digital supplies, C16 should connect close to pins 20 and 21, with a short, low-inductance path running from pin 21 to pin 13, and another one from pin 12 to 20.

A useful reference for PCB layout is the demonstration circuit board for the 5171/1570 part pair, available from THAT. While the board itself is of course useful to designers, the layout and schematic are published in the data sheet which covers the board, and is available for downloading from THAT's web site.

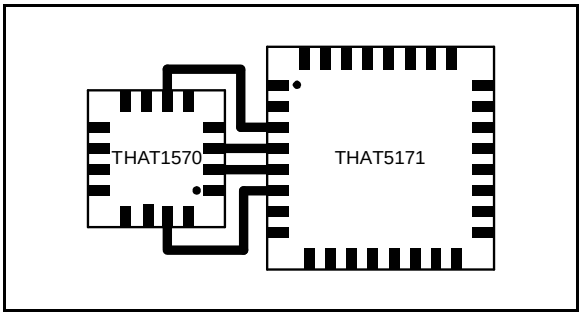


Figure 15. Recommended THAT1570/THAT5171 PCB Layout (mounted on same-side of PCB).

Copyright © 2014, THAT Corporation; All rights reserved.

Package and Soldering Information

Package Characteristics

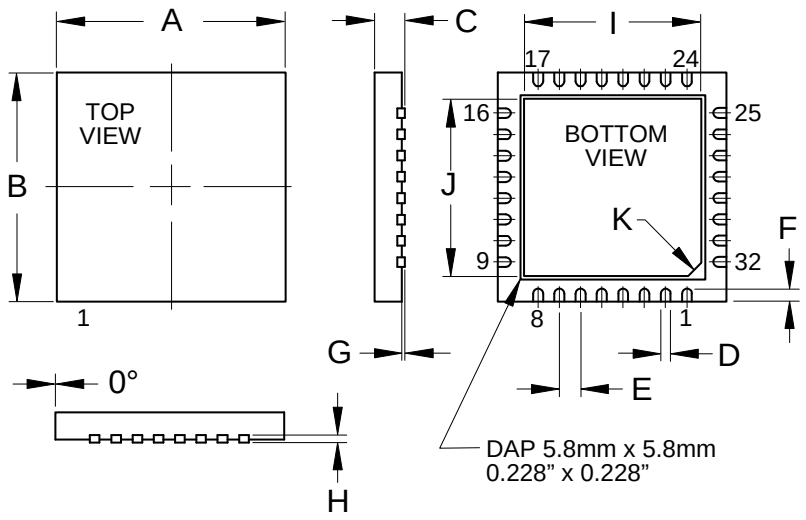
Parameter	Symbol	Conditions	Min	Typ	Max	Units
Package Style		See Fig. 16 for dimensions		32 Pin QFN		
Thermal Resistance	θ_{JA}	QFN package, and thermal pad not soldered to board		90		ºC/W
Environmental Regulation Compliance				Complies with January 27, 2003 RoHS requirements		
Soldering Reflow Profile				JEDEC JESD22-A113-D (250 ºC)		
Moisture Sensitivity Level	MSL	Above-referenced JEDEC soldering profile		3		

The THAT 5171 is available in a 7mm x 7mm 32-pin QFN package. The package dimensions are shown in Figure 16. Pinouts are given in Table 1.

The 5171 is lead free and RoHS compliant. Material Declaration Data Sheets on the parts are available at our web site, www.thatcorp.com or upon request. For ordering information, see Table 14.

Package	Order Number
32 pin QFN	5171N32-U

Table 14. Ordering information.



	MM		Mils	
SYM	MIn	Max	MIn	Max
A	6.90	7.10	271.65	279.53
B	6.90	7.10	271.65	279.53
C	0.85	0.95	33.46	37.40
D	0.2	0.3	7.87	11.81
E	0.65 BSC		25.59 BSC	
F	0.35	0.45	13.78	17.72
G	0.00	0.05	0.00	1.97
H	0.175	0.225	6.89	8.86
I	5.35	5.45	210.63	214.57
J	5.35	5.45	210.63	214.57
K	C' 0.4 mm x 45°		C‘ 15.7 mils x 45°	

Figure 16. 7 x 7mm QFN32 Package Dimensions.

Copyright © 2014, THAT Corporation; All rights reserved.

Revision History

Revision	ECO	Date	Changes	Page
00	—	September 2009	Preliminary release	
01	2341	October 2009	Corrected error in figure six, input inverted.	10
02	2364	January 2010	Corrected error in Table 6 - SPI registers Corrected error in Table 8 - Chip ID	12 13
03	2442	July 2010	Revised Input Offset Voltage specification. Revised Max and Min Output Current specs. Added clarification to package slug soldering text. Corrected pin number in bypass cap layout text. Updated Thermal Resistance spec. Removed “Preliminary” watermark.	3 3 17 17 18 All
04	2476	December 2010	Minor typographical corrections.	—
05	2659	February 2012	Revised Max Output Current specification	3
06	2766	March 2013	Expanded text in "Gain Update Modes" section 2-A. Corrected typo in the PCB Layout section	12 17
07	2873	May 2014	Optimized capacitor values in application figures	—
08	2898	August 2014	Removed text reference to forthcoming design note	14

Copyright © 2014, THAT Corporation; All rights reserved.

Notes

THAT Corporation; 45 Sumner Street; Milford, MA 01757-1656; USA
Tel: +1 508 478 9200; Fax: +1 508 478 0990; Web: www.thatcorp.com
Copyright © 2014, THAT Corporation; All rights reserved.

Общество с ограниченной ответственностью «МосЧип» ИНН 7719860671 / КПП 771901001
Адрес: 105318, г.Москва, ул.Щербаковская д.3, офис 1107

Данный компонент на территории Российской Федерации

Вы можете приобрести в компании MosChip.

Для оперативного оформления запроса Вам необходимо перейти по данной ссылке:

http://moschip.ru/get-element

Вы можете разместить у нас заказ для любого Вашего проекта, будь то серийное производство или разработка единичного прибора.

В нашем ассортименте представлены ведущие мировые производители активных и пассивных электронных компонентов.

Нашей специализацией является поставка электронной компонентной базы двойного назначения, продукции таких производителей как XILINX, Intel (ex.ALTERA), Vicor, Microchip, Texas Instruments, Analog Devices, Mini-Circuits, Amphenol, Glenair.

Сотрудничество с глобальными дистрибьюторами электронных компонентов, предоставляет возможность заказывать и получать с международных складов практически любой перечень компонентов в оптимальные для Вас сроки.

На всех этапах разработки и производства наши партнеры могут получить квалифицированную поддержку опытных инженеров.

Система менеджмента качества компании отвечает требованиям в соответствии с ГОСТ Р ИСО 9001, ГОСТ РВ 0015-002 и ЭС РД 009

Офис по работе с юридическими лицами:

105318, г.Москва, ул.Щербаковская д.3, офис 1107, 1118, ДЦ «Щербаковский»

Телефон: +7 495 668-12-70 (многоканальный)

Факс: +7 495 668-12-70 (доб.304)

E-mail: info@moschip.ru

Skype отдела продаж:
moschip.ru
moschip.ru_4
moschip.ru_6
moschip.ru_9