# 3.3V PECL/ECL DIFFERENTIAL PHASE-FREQUENCY DETECTOR

**Precision Edge®**
**SY100EP140L**

## FEATURES

- **>2GHz maximum frequency**
- **< 220ps rise/fall time**
- **Low-voltage: +3.3V ±10% operation**
- **Wide operating temperature range: –40°C to +85°C**
- **Fully differential throughput architecture**
- **Transfer gain:**
  - **1.0mV/degree at 1.4GHz**
  - **1.2mV/degree at 1.0GHz**
- **Available in 8-Pin SOIC package**



**ECL Pro™**

## DESCRIPTION

The SY100EP140L is a high-speed, 2GHz phase-frequency detector optimized to control ultra-low noise VCXOs (voltage-controlled crystal oscillators) in telecom and datacom systems. The phase-frequency detector compares two input signals—a reference input and a feedback input. Any mismatches in the two input signal's phase or frequency will result in the output UP or DOWN pulse stream. When the difference between the UP and DOWN outputs are integrated, the resulting control signal speeds-up or slows-down a VCO or acts as the error voltage for a precision VCXO.

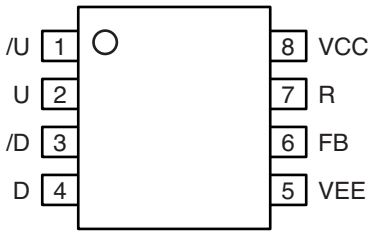
The SY100EP140L I/O is 100K LVECL/LVPECL compatible. The device operates from a +3.0V to +3.6V (LVPECL) or –3.0V to -3.6V (LVECL) supply voltage. The output swing is 400mV with < 220ps rise/fall times, which enables the part to operate at a very high frequency. Operating temperature range is guaranteed over the –40°C to +85°C industrial range.

## PIN NAMES

| Pin | Function |
|---|---|
| D, /D | LVPECL/LVECL differential UP outputs. Terminate with 50Ω to $V_{CC}$–2V. |
| U, /U | LVPECL/LVECL differential DOWN outputs. Terminate with 50Ω to $V_{CC}$–2V. |
| R | LVPECL/LVECL reference input. Internal 75kΩ pulldown to $V_{EE}$. Default state is logic LOW when left floating. |
| FB | LVPECL/LVECL feedback input. Internal 75kΩ pulldown resistor to $V_{EE}$. Default state is logic LOW when left floating. |
| $V_{CC}$ | Positive supply. Bypass with 0.1μF//0.01μF low ESR capacitors. |
| $V_{EE}$ | Negative power supply. For PECL operation, connect to GND. |

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## PACKAGE/ORDERING INFORMATION




**8-pin SOIC package**

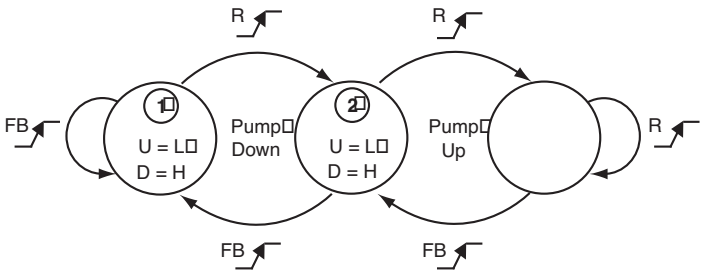
### Ordering Information[1]

| Part Number | Package Type | Operating Range | Package Marking | Lead Finish |
|---|---|---|---|---|
| SY100EP140LZC | Z8-1 | Commercial | XP140L | Sn-Pb |
| SY100EP140LZCTR[2] | Z8-1 | Commercial | XP140L | Sn-Pb |
| SY100EP140LZI | Z8-1 | Industrial | XP140L | Sn-Pb |
| SY100EP140LZITR[2] | Z8-1 | Industrial | XP140L | Sn-Pb |
| SY100EP140LZG[3] | Z8-1 | Industrial | XP140L with Pb-Free bar-line indicator | NiPdAu Pb-Free |
| SY100EP140LZGTR[2, 3] | Z8-1 | Industrial | XP140L with Pb-Free bar-line indicator | NiPdAu Pb-Free |

**Notes:**

1. Contact factory for die availability. Dice are guaranteed at $T_A = 25°C$, DC Electricals only.
2. Tape and Reel.
3. Pb-Free package is recommended for new designs.

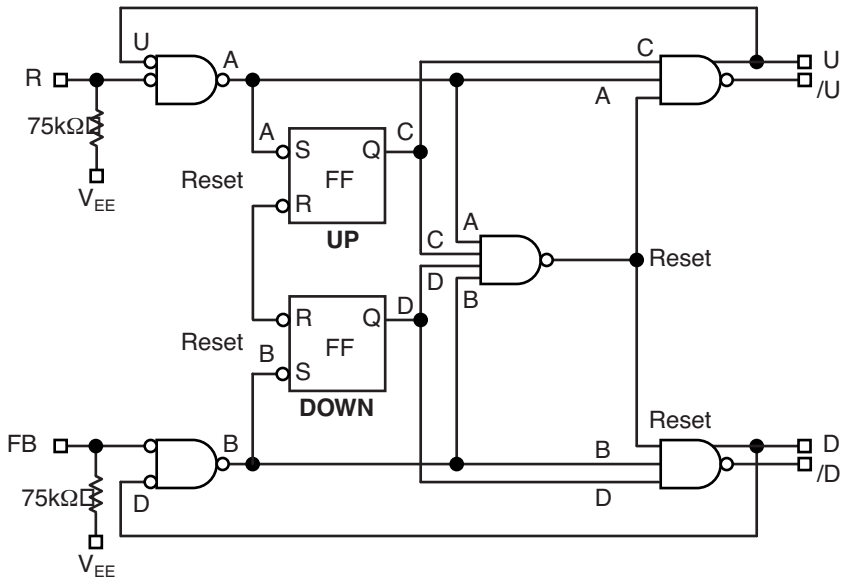
## PHASE DETECTOR LOGIC MODEL




## TRUTH TABLE

| Phase Dector State | Input R | Input FB | Output U | Output D |
|---|---|---|---|---|
| Pump Down (2–1–2) | | | | |
| 2 | L | L | L | L |
| 2–1 | L | H | L | H |
| 1–2 | H | X | L | L |
| 2 | L | L | L | L |
| Pump Up (2–3–2) | | | | |
| 2 | L | L | L | L |
| 2–3 | H | L | H | L |
| 3–2 | X | H | L | L |
| 2 | L | L | L | L |

## LOGIC DIAGRAM



## ABSOLUTE MAXIMUM RATINGS(1)

| Symbol | Rating | | | Value | Unit |
|---|---|---|---|---|---|
| $V_{CC} - V_{EE}$ | Power Supply Voltage | | | 6V | V |
| $V_{IN}$ | Input Voltage ($V_{CC}$ = 0V, $V_{IN}$ not more negative than $V_{EE}$)<br>Input Voltage ($V_{EE}$ = 0V, $V_{IN}$ not more positive than $V_{CC}$) | | | –6.0 to 0<br>+6.0 to 0 | V<br>V |
| $I_{OUT}$ | Output Current | –Continuous<br>–Surge | | 50<br>100 | mA |
| $T_A$ | Operating Temperature Range | | | –40 to +85 | °C |
| $T_{LEAD}$ | Lead Temperature (Soldering, 20sec.) | | | +260 | °C |
| $T_{store}$ | Storage Temperature Range | | | –65 to +150 | °C |
| | Maximum Junction Temperature | | | 135 | °C |
| $\theta_{JA}$ | Package Thermal Resistance<br>(Junction-to-Ambient) | –Still-Air<br>–500lfpm<br>–Still-Air<br>–500lfpm | (SOIC)<br>(SOIC)<br>(MSOP)<br>(MSOP) | 160<br>109<br>206<br>155 | °C/W<br><br>°C/W<br> |
| $\theta_{JC}$ | Package Thermal Resistance<br>(Junction-to-Case) | | (SOIC)<br>(MSOP) | 39<br>39 | °C/W<br> |

**Note 1.** Permanent device damage may occur if absolute maximum ratings are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to absolute maximum ratlng conditions for extended periods may affect device reliability.

## DC ELECTRICAL CHARACTERISTICS(1)

| Symbol | Parameter | $T_A$ = –40°C | | | $T_A$ = +25°C | | | $T_A$ = +85°C | | | Unit | Condition |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | Min. | Typ. | Max. | Min. | Typ. | Max. | | |
| $V_{CC}$ | Power Supply Voltage<br>(LVPECL)<br>(LVECL) | <br>3.0<br>–3.6 | <br>—<br>— | <br>3.6<br>–3.0 | <br>3.0<br>–3.6 | <br>—<br>— | <br>3.6<br>–3.0 | <br>3.0<br>–3.6 | <br>—<br>— | <br>3.6<br>–3.0 | V | |
| $I_{EE}$ | Power Supply Current | 55 | 70 | 85 | 60 | 74 | 90 | 63 | 78 | 93 | mA | |
| $I_{IH}$ | Input HIGH Current | — | — | 150 | — | — | 150 | — | — | 150 | µA | $V_{IN} = V_{IH}$ |
| $I_{IL}$ | Input LOW Current R, FB | 0.5 | — | — | 0.5 | — | — | 0.5 | — | — | µA | $V_{IN} = V_{IL}$ |
| $C_{IN}$ | Input Capacitance (MSOP)<br>(SOIC) | —<br>— | —<br>— | —<br>— | —<br>— | 0.75<br>1.1 | —<br>— | —<br>— | —<br>— | —<br>— | pF<br>pF | |

**Note 1.** 100KEP circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and traverse airflow greater than 500lfpm is maintained.

## LVPECL DC ELECTRICAL CHARACTERISTICS(1)

$V_{CC}$ = 3.3V ±10%, $V_{EE}$ = 0V

| Symbol | Parameter | $T_A$ = –40°C | | | $T_A$ = +25°C | | | $T_A$ = +85°C | | | Unit | Condition |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | Min. | Typ. | Max. | Min. | Typ. | Max. | | |
| $V_{IL}$ | Input LOW Voltage (Single-Ended) | 1355 | — | 1675 | 1355 | — | 1675 | 1355 | — | 1675 | mV | |
| $V_{IH}$ | Input HIGH Voltage (Single-Ended) | 2075 | — | 2420 | 2075 | — | 2420 | 2075 | — | 2420 | mV | |
| $V_{OL}$ | Output LOW Voltage | 1355 | 1480 | 1605 | 1355 | 1480 | 1605 | 1355 | 1480 | 1605 | mV | 50Ω to $V_{CC}$–2V |
| $V_{OH}$ | Output HIGH Voltage | 2155 | 2280 | 2405 | 2155 | 2280 | 2405 | 2155 | 2280 | 2405 | mV | 50Ω to $V_{CC}$–2V |

**Note 1.** 100KEP circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and traverse airflow greater than 500lfpm is maintained. Input and output parameters are at $V_{CC}$ = 3.3V. They vary 1:1 with $V_{CC}$.

## ECL DC ELECTRICAL CHARACTERISTICS[1]

$V_{CC}$ = 0V, $V_{EE}$ = –3.6V to –3.0V

| Symbol | Parameter | $T_A$ = –40°C | | | $T_A$ = +25°C | | | $T_A$ = +85°C | | | Unit | Condition |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | Min. | Typ. | Max. | Min. | Typ. | Max. | | |
| $V_{IL}$ | Input LOW Voltage | –1945 | — | –1625 | –1945 | — | –1625 | –1945 | — | –1625 | mV | |
| $V_{IH}$ | Input HIGH Voltage | –1225 | — | –880 | –1225 | — | –880 | –1225 | — | –880 | mV | |
| $V_{OL}$ | Outuput LOW Voltage | –1545 | –1420 | –1295 | –1545 | –1420 | –1295 | –1545 | –1420 | –1295 | mV | 50Ω to $V_{CC}$–2V |
| $V_{OH}$ | Output HIGH Voltage | –1145 | –1020 | –895 | –1145 | –1020 | –895 | –1145 | –1020 | –895 | mV | 50Ω to $V_{CC}$–2V |

**Note 1.** 100KEP circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and traverse airflow greater than 500lfpm is maintained. Input and output parameters are at $V_{CC}$ = 3.3V. They vary 1:1 with $V_{CC}$.

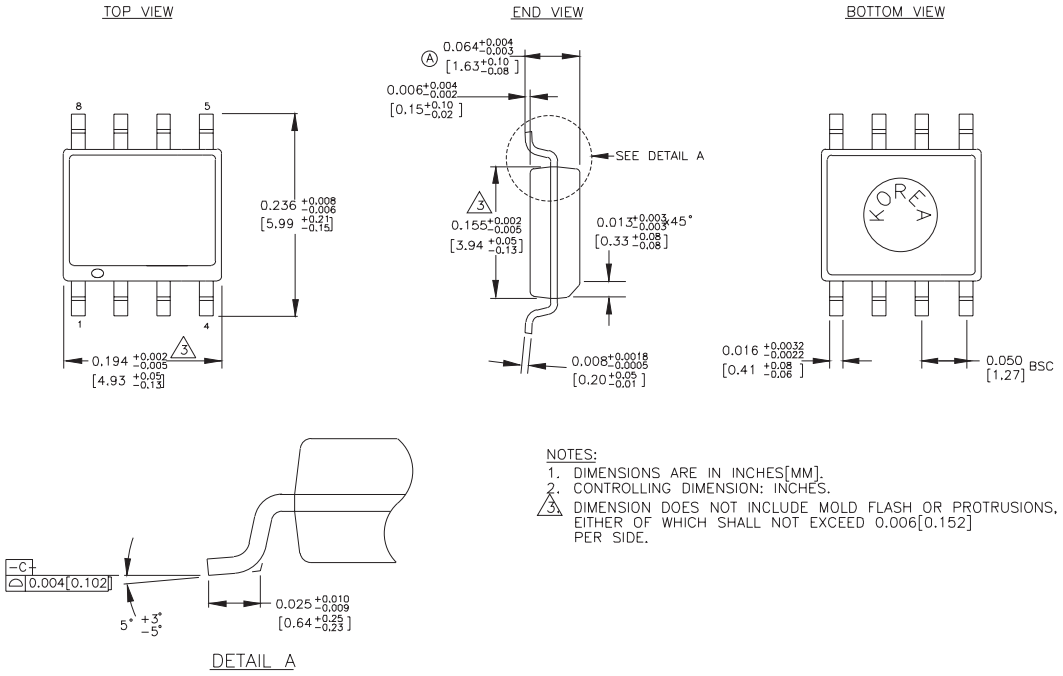
## AC ELECTRICAL CHARACTERISTICS[1]

LVPECL: $V_{CC}$ = 3.3V±10%, $V_{EE}$ = 0V; LVECL: $V_{EE}$ = –3.3V±10%, $V_{CC}$ = 0V

| Symbol | Parameter | $T_A$ = –40°C | | | $T_A$ = +25°C | | | $T_A$ = +85°C | | | Unit | Condition |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | Min. | Typ. | Max. | Min. | Typ. | Max. | | |
| $f_{MAX}$ | Maximum Frequency[1] | — | >2 | — | — | >2 | — | — | >2 | — | GHz | |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation Delay to Output (Differential) | | | | | | | | | | | |
| | R to U, FB to D | 220 | 450 | 600 | 230 | 475 | 625 | 240 | 500 | 650 | ps | |
| | FB to U, R to D | 280 | 650 | 800 | 280 | 650 | 850 | 300 | 700 | 900 | ps | |
| $t_{JITTER}$ | Cycle-to-Cycle Jitter (rms) | — | 0.2 | < 1 | — | 0.2 | < 1 | — | 0.2 | < 1 | $ps_{rms}$ | |
| $V_{PP}$ | Input Voltage Swing | 400 | 800 | 1200 | 400 | 800 | 1200 | 400 | 800 | 1200 | mV | |
| $t_r$, $t_f$ | Output Rise/Fall Time Q, /Q (20% to 80%) | 50 | 90 | 180 | 60 | 100 | 200 | 70 | 120 | 220 | ps | |

**Note 1.** Measured with 750mV input signal, 50% duty cycle. All loading with a 50Ω to $V_{CC}$–2.0V.

## 8-PIN PLASTIC SOIC (Z8-1)




NOTES:
1. DIMENSIONS ARE IN INCHES[MM].
2. CONTROLLING DIMENSION: INCHES.
3. DIMENSION DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS, EITHER OF WHICH SHALL NOT EXCEED 0.006[0.152] PER SIDE.

Rev. 03

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