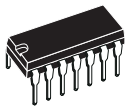
HCF4021

Asynchronous parallel input or synchronous serial-in/serial-out 8-stage static shift register

Datasheet - production data



PDIP-16

SO-16

Features

- Medium speed operation: 12 MHz (typ.) clock rate at V_{DD} - V_{SS} = 10 V
- Fully static operation
- 8 master-slave flip-flops plus output buffering and control gating
- Quiescent current specified up to 20 V
- 5 V, 10 V, and 15 V parametric ratings
- Input leakage current I_I = 100 nA (max.) at V_{DD} = 18 V, T_A = 25 °C
- 100% tested for quiescent current
- ESD performance
  - CDM: 1 kV
  - HBM: 2 kV
  - MM: 200 V

Applications

- Automotive
- Industrial
- Computer
- Consumer

Description

The HCF4021 is a monolithic integrated circuit fabricated in metal oxide semiconductor technology available in PDIP-16 and SO-16 packages.

This device is an 8-stage parallel or serial-input/serial-output register having common clock and parallel/serial control inputs, a single serial data input, and individual parallel "jam" inputs to each register stage. Each register stage is a D-type, master-slave flip-flop in addition to an output from stage 8. "Q" outputs are also available from stages 6 and 7. Serial entry is synchronous with the clock but parallel entry is asynchronous.

In this device, entry is controlled by the parallel/serial control input. When the parallel/serial control input is low, data are serially shifted into the 8-stage register synchronously with the positive transition of the clock line. When the parallel/serial control input is high, data are jammed into the 8-stage register via the parallel input lines and synchronous with the positive transition of the clock line. The clock input of the internal stage is “forced” when asynchronous parallel entry is made. Register expansion using multiple packages is permitted.

Table 1. Device summary

Order code	Temperature range	Package	Packing	Marking
HCF4021M013TR	-55 ° C to +125 ° C	SO-16	Tape & reel	HCF4021
HCF4021YM013TR(1)	-40 ° C to +125 ° C	SO-16 (automotive grade)(1)		HCF4021Y
HCF4021BEY	-55 ° C to +125 ° C	PDIP-16	Tube	HCF4021BE

1. Qualification and characterization according to AEC Q100 and Q003 or equivalent, advanced screening according to AEC Q001 & Q002 or equivalent.

Contents

1 Pin information

Figure 1. Pin connections (top view)

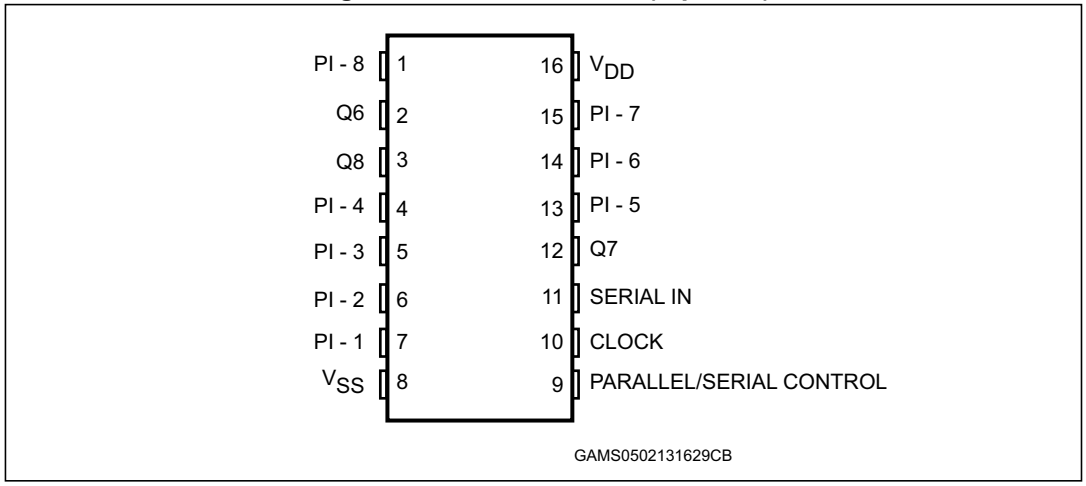


Table 2. Pin description

Pin number	Symbol	Name and function
7, 6, 5, 4, 13, 14, 15, 1	PI-1 to PI-8	Parallel input
11	SERIAL IN	Serial input
9	PARALLEL/SERIAL CONTROL	Parallel/serial input control
10	CLOCK	Clock input
2, 3, 12	Q6, Q7, Q8	Buffered outputs
8	V_{SS}	Negative supply voltage
16	V_{DD}	Positive supply voltage

2 Functional description

Figure 2. Logic diagram

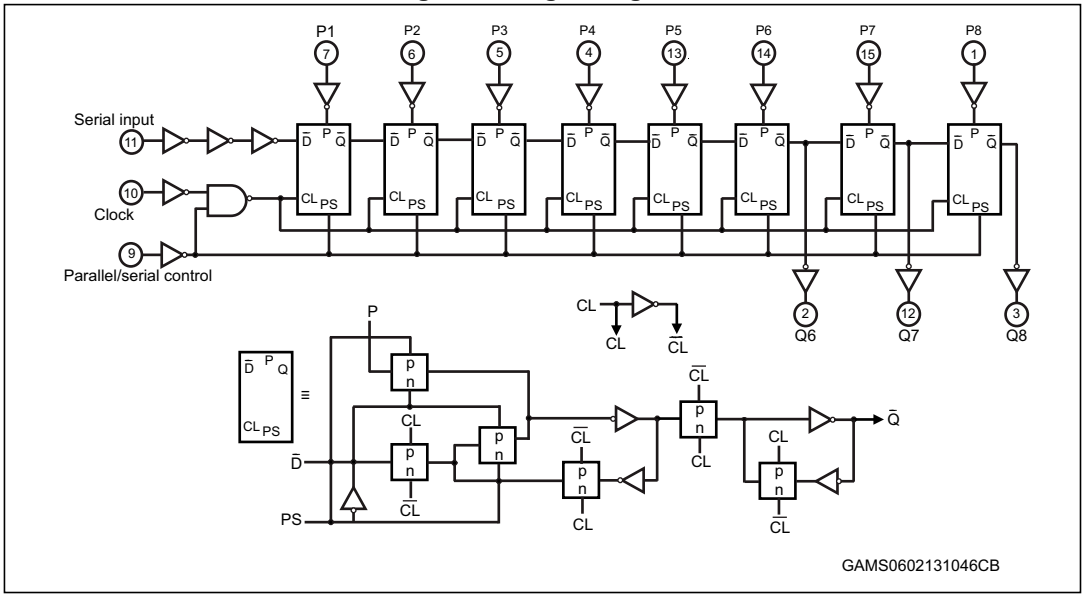
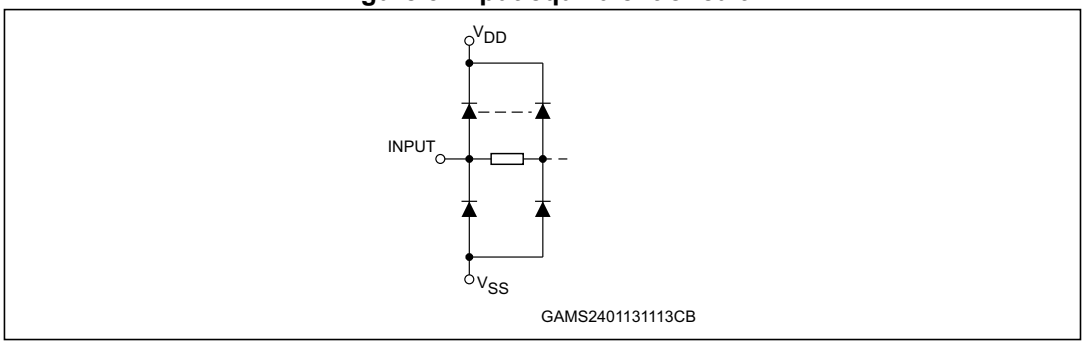


Table 3. Truth table

Clock	Serial input	Parallel/serial control	PI-1	PI-n	Q_1 (internal)	Q_n
X(1)	X(1)	1	0	0	0	0
X(1)	X(1)	1	0	1	0	1
X(1)	X(1)	1	1	0	1	0
X(1)	X(1)	1	1	1	1	1
⎍	0	0	X(1)	X(1)	0	Q_{n-1}
⎍	1	0	X(1)	X(1)	1	Q_{n-1}
⎏	X(1)	X(1)	X(1)	X(1)	Q_1	Q_n

1. Don't care

Figure 3. Input equivalent circuit



3 Electrical characteristics

Absolute maximum ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. All voltage values are referred to V_{SS} pin voltage.

Table 4. Absolute maximum ratings (AMR)

Symbol	Parameter	Value	Unit
V_{DD}	Supply voltage	-0.5 to +22	V
V_I	DC input voltage	-0.5 to V_{DD} + 0.5	
I_I	DC input current	±10	mA
P_D	Power dissipation per package	200	mW
	Power dissipation per output transistor	100	
T_{op}	Operating temperature	-55 to +125	°C
T_{stg}	Storage temperature	-65 to +150	

Table 5. Recommended operating conditions

Symbol	Parameter	Value	Unit
V_{DD}	Supply voltage	3 to 20	V
V_I	Input voltage	0 to V_{DD}	
T_{op}	Operating temperature	-55 to 125	°C

Table 6. DC specifications(1)

Sym.	Parameter	Test condition				Value							Unit
		V_I (V)	V_O (V)	$\|I_O\|$ (µA)	V_{DD}(V)	T_A = 25 °C			-40 to 85 °C		-55 to 125°C		
						Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
I_L	Quiescent current	0/5			5			5		150		150	µA
		0/10			10		0.04	10		300		300	
		0/15			15			20		600		600	
		0/20			20		0.08	100		3000		3000	
V_{OH}	High-level output voltage	0/5		<1	5	4.95			4.95		4.95		V
		0/10			10	9.95			9.95		9.95		
		0/15			15	14.95			14.95		14.95		
V_{OL}	Low-level output voltage	5/0		<1	5		0.05			0.05		0.05	
		10/0			10								
		15/0			15								
V_{IH}	High-level input voltage		0.5/4.5	<1	5	3.5			3.5		3.5		
			1/9		10	7			7		7		
			1.5/13.5		15	11			11		11		
V_{IL}	Low-level input voltage		4.5/0.5	<1	5			1.5		1.5		1.5	
			9/1		10			3		3		3	
			13.5/1.5		15			4		4		4	
I_{OH}	Output drive current	0/5	2.5	<1	5	-1.36	-3.2		-1.1		-1.1		mA
			4.6			-0.44	-1		-0.36		-0.36		
		0/10	9.5		10	-1.1	-2.6		-0.9		-0.9		
		0/15	13.5		15	-3.0	-6.8		-2.4		-2.4		
I_{OL}	Output sink current	0/5	0.4	<1	5	0.44	1		0.36		0.36		
		0/10	0.5		10	1.1	2.6		0.9		0.9		
		0/15	1.5		15	3.0	6.8		2.4		2.4		
I_I	Input leakage current	0/18	Any input		18		$\pm 10^{-5}$	±0.1		±1		±1	µA
C_I	Input capacitance		Any input				5	7.5					pF

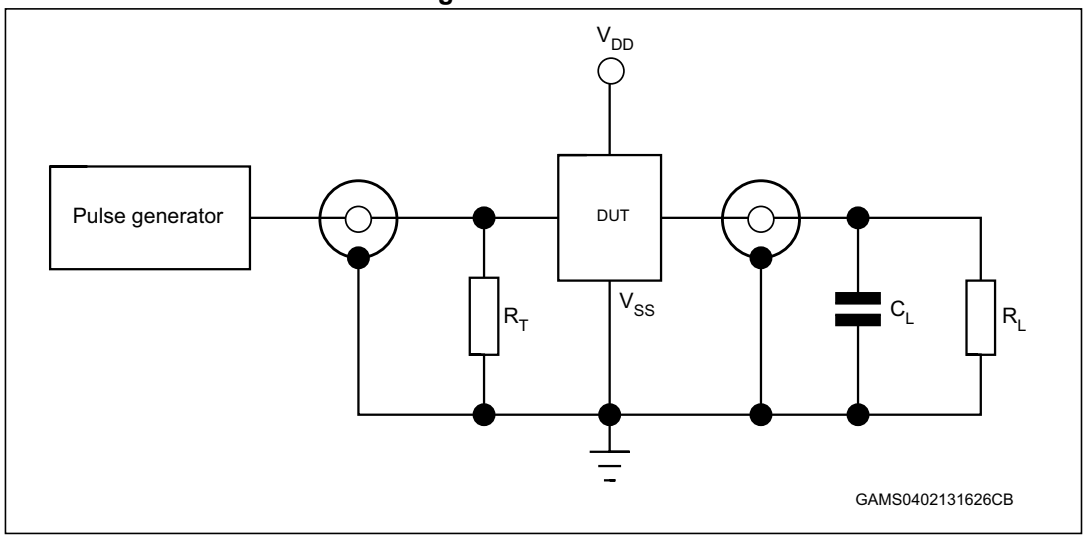
1. The noise margin for both level "1" and "0" is: 1 V min. with V_{DD} = 5 V, 2 V min. with V_{DD} = 10 V, and 2.5 V min. with V_{DD} = 15 V.

Table 7. Dynamic electrical characteristics (T_{amb} = 25 °C, C_L = 50 pF, R_L = 200 kΩ, t_r = t_f = 20 ns)

Symbol	Parameter	Test condition	Value[1]			Unit
		V_{DD} (V)	Min.	Typ.	Max.	
t_{PLH}, t_{PHL}	Propagation delay time	5		160	320	ns
		10		80	160	
		15		60	120	
t_{THL}, t_{TLH}	Transition time	5		100	200	
		10		50	100	
		15		40	80	
f_{CL}[2]	Maximum clock input frequency	5	3	6		MHz
		10	6	12		
		15	8.5	17		
t_w	Clock pulse width	5	180	90		ns
		10	80	40		
		15	50	25		
t_r , t_f	Clock input rise or fall time	5			15	µs
		10				
		15				
t_s	Minimum setup time, serial input $t_H \geq 200$ ns (ref to CL)	5	120	60		ns
		10	80	40		
		15	60	30		
	Minimum setup time, parallel inputs $t_H \leq 200$ ns (ref to P/S)	5	50	25		
		10	30	15		
		15	20	10		
t_h	Hold time, serial in, parallel in, parallel/serial control	5	0			
		10				
		15				
t_{WH}	P/S pulse width	5	160	80		
		10	80	40		
		15	50	25		
t_{rem}	P/S removal time ref to CL)	5	280	140		
		10	140	70		
		15	100	50		

1. The typical temperature coefficient for all V_{DD} values is 0.3 %/°C.
2. If more than one unit is cascaded, t_rCL should be made less than or equal to the sum of the transition time and the fixed propagation delay of the output of the driving stage of the estimated capacitive load.

Figure 4. Test circuit



1. Legend: C_L = 50 pF or equivalent (includes jig and probe capacitance), R_L = 200 KΩ, R_T = Z_{OUT} of pulse generator (typically 50 Ω)

Figure 5. Waveform 1: propagation delay times, clock pulse width (f = 1 MHz; 50 % duty cycle)

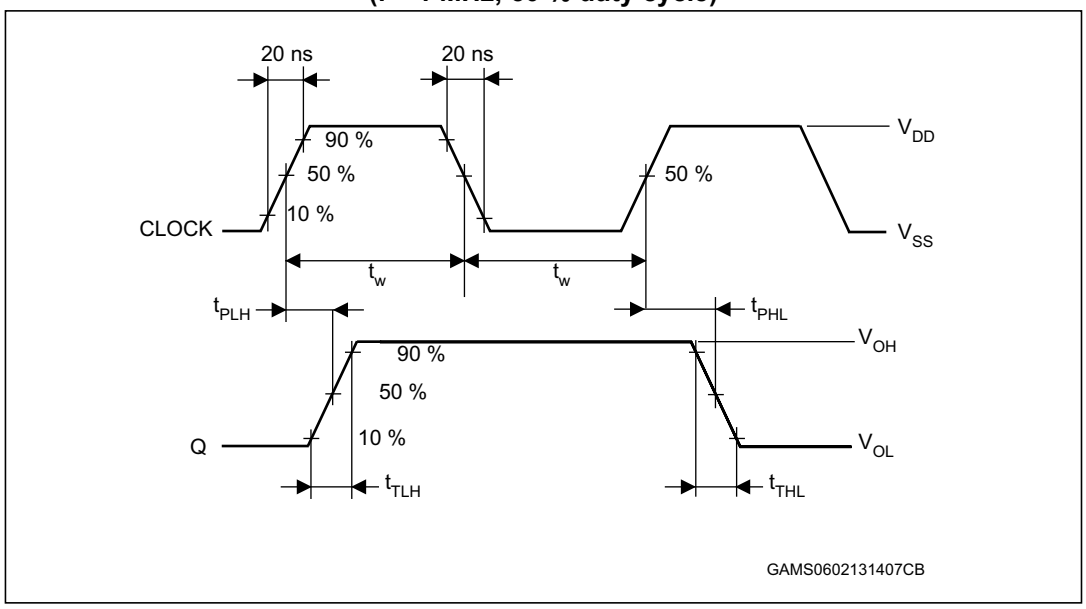


Figure 6. Waveform 2: setup and hold times (SI to CLOCK) (f = 1 MHz; 50 % duty cycle)

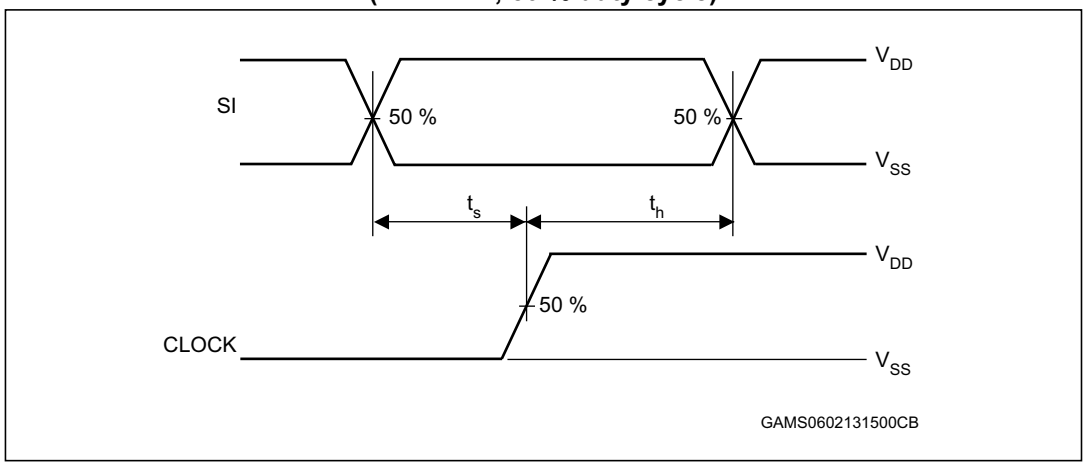


Figure 7. Waveform 3: setup and hold time (PI to P/S) (f = 1 MHz; 50 % duty cycle)

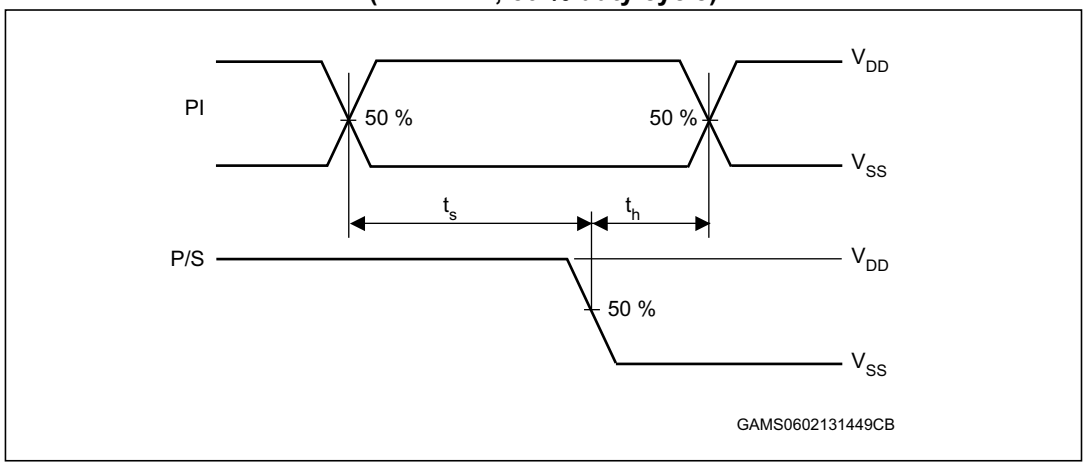
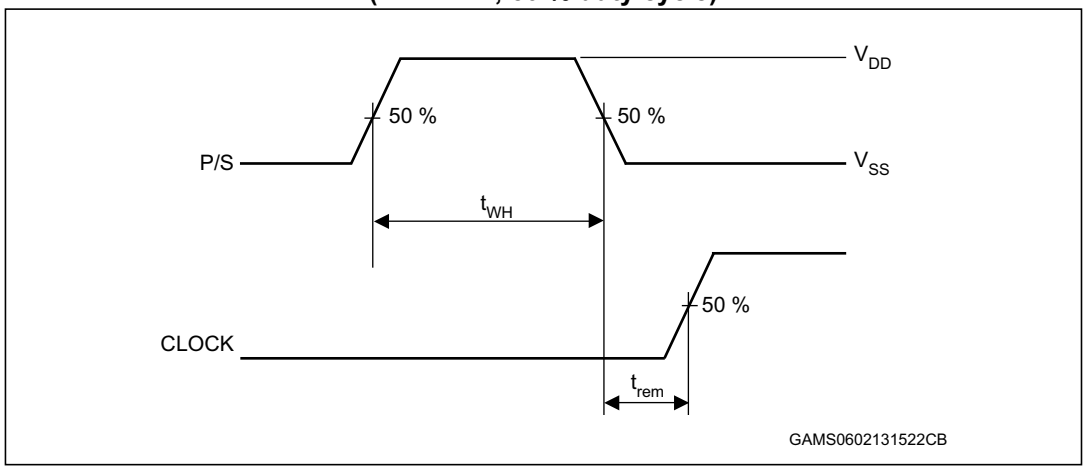


Figure 8. Waveform 4: pulse width and removal time (P/S to clock) (f = 1 MHz; 50 % duty cycle)



4 Package information

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4.1 PDIP-16 (0.25) package information

Figure 9. PDIP-16 (0.25) package mechanical drawing

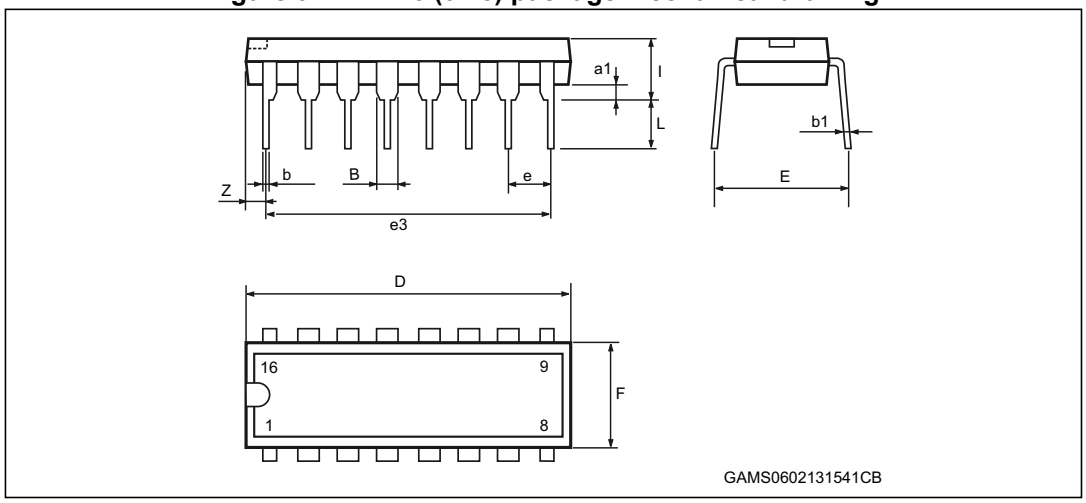

Table 8. PDIP-16 (0.25) package mechanical data

Ref	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
a1	0.51			0.020		
B	0.77		1.65	0.030		0.065
b		0.5			0.020	
b1		0.25			0.010	
D			20			0.787
E		8.5			0.335	
e		2.54			0.100	
e3		17.78			0.700	
F			7.1			0.280
I			5.1			0.201
L		3.3			0.130	
Z	1.27		1.27	0.050		0.050

4.2 SO-16 package information

Figure 10. SO-16 package mechanical drawing

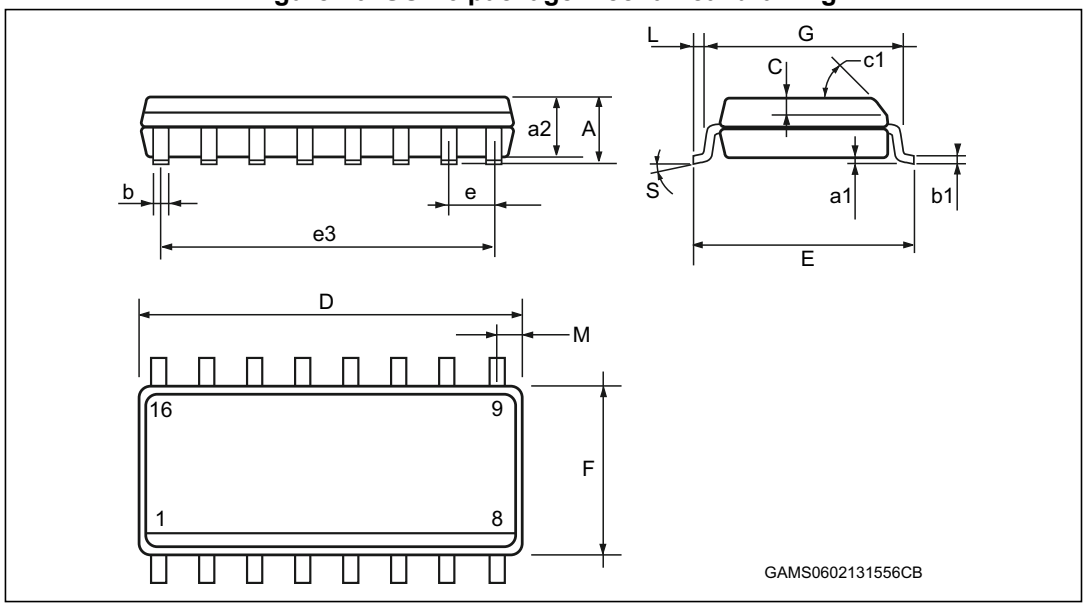

Table 9. SO-16 package mechanical data

Ref	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.75			0.068
a1	0.1		0.2	0.003		0.007
a2			1.65			0.064
b	0.35		0.46	0.013		0.018
b1	0.19		0.25	0.007		0.010
C		0.5			0.019	
c1		45 °			45 °	
D	9.8		10	0.385		0.393
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		8.89			0.350	
F	3.8		4.0	0.149		0.157
G	4.6		5.3	0.181		0.208
L	0.5		1.27	0.019		0.050
M			0.62			0.024
S			8 °			8 °

5 Ordering information

Table 10. Order codes

Order code	Temperature range	Package	Packing	Marking
HCF4021M013TR	-55 ° C to +125 ° C	SO-16	Tape & reel	HCF4021
HCF4021YM013TR (1)	-40 ° C to +125 ° C	SO-16 (automotive grade)(1)		HCF4021Y
HCF4021BEY	-55 ° C to +125 ° C	PDIP-16	Tube	HCF4021BE

1. Qualification and characterization according to AEC Q100 and Q003 or equivalent, advanced screening according to AEC Q001 & Q002 or equivalent.

6 Revision history

Table 11. Document revision history

Date	Revision	Changes
Sep-2001	1	Initial release.
18-Feb-2013	2	Document template and layout updated Removed “B” from part number Updated package names (PDIP-16 and SO-16 instead of DIP-16 and SOP-16). Added *Applications* Added *Device summary* Updated symbol names in *Table 7* Added *Section 5: Ordering information*
12-Sep-2013	3	Added ESD performance to *Features* Updated footnote *1* of *Table 1* Updated footnote *1* of *Table 10*

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