General Description

The MAX14748 USB battery charger integrates a charger detector, boost/buck converter, and Li+ battery charger with smart power selector to provide fast and safe charging of 2s Li+ battery packs.

The MAX14748 provides support for devices functioning as a UFP/DRP per the USB Type-C 1.1 standard, while also providing detection of legacy USB Battery Charging Specification, Revision 1.2 (BC1.2) compliant chargers in addition to other nonstandard chargers. The programmable Automatic Input Current Limiting (AICL) feature ensures that maximum safe current is drawn from the charging adapter.

The Li+ charger includes an automatic Smart Power Selector™ to simultaneously charge the battery and provide power to the system load. The Smart Power Selector function will supplement the system power with the battery if power from the charging adapter is insufficient. The Li+ charger features JEITA thermal monitoring and charger voltage/current reduction or charger disable.

The MAX14748 is available in a 54-bump, 0.4mm pitch, 3.97mm x 2.77mm x 0.64mm wafer-level package (WLP) and operates over the -40°C to +85°C extended temperature range.

Applications

- Digital Imaging (DSC, DVC)
- Wireless Speakers
- Handheld Barcode Readers

Ordering Information appears at end of data sheet.

Benefits and Features

- Minimize Power Management Footprint Through High Integration
 - 13mΩ (typ) Integrated Battery To System Switch
 - · Thermal Current Limiting
 - · DC-DC Converter with Boost and Reverse Buck
 - · High Efficiency
 - 92% in Boost Mode at 1A Output Current and 7.4V Battery Voltage
 - 94% in Reverse Buck Mode at 500mA Output
 - Internal USB Switch for USB D+/D- Data Lines
- Easy-to-Implement Li+ Battery Charging
 - Charges 2s Li-lon Batteries from Legacy 5V USB Adapters
 - 15W Input Power with 3A Type-C Adapter
 - 7.5W Input Power with DCP Adapter
 - 1A System/Charge Current From DCP Adapter
 - 2A System/Charge Current From 3A Type-C Adapter
 - DRP Mode USB Type-C Specification, Rev 1.1 Compliant
 - UFP Mode USB Type-C Specification, Rev 1.1 Support
 - V_{CONN} and Super-Speed Multiplexer Logic Controls
 - · Non-Standard DCP Detection
 - · USB Battery Charging Specification, Rev 1.2 Compliant
- Automatic Input Current Limit (AICL) Power Management
- Support Weak/Dead Batteries Detection
 - · Smart Power Selector
 - Thermistor Monitor
- Various Protection Features
 - · 28V Integrated Overvoltage Protection
 - JEITA Charge Protection
 - ±15kV ESD Protection on USB Adapter Pins

Smart Power Selector is a trademark of Maxim Integrated Products, Inc.



Absolute Maximum Ratings

Voltages Referenced to GND
CHGIN0.3V to +30V
BST0.3V to +16V
SYS to BAT0.3V to +12V
BAT, SYS0.3V to +12V
BYP to CHGIN30V to +0.3V
BYP, THM, INT, SYSOK, FLTIN, FSUS,
LED, SDA, SCL0.3V to 6V
COMP, SET0.3V to V _{CCINT} + 0.3V
CC1, CC2, TDN, TDP, CDN, CDP, V _{CONN} 0.3V to +6V
CC1, CC2, in fault mode through a 10k resistor0.3V to +20V
CDIR0.3V to +6V
VTPU (VTPU-TPU switch open)0.3V to V _{CCINT} + 0.3V
TPU (VTPU-TPU switch open)0.3V to 6 or VTPU + 0.3V
VTPU, TPU Maximum Current
(VTPU-TPU switch closed)100mA to +100mA
BVCEN0.3V to V _{CCINT} + 0.3V

SFOUT, V _{CCINT} , BREG0.3V to min ((V _{CHGIN} LX0.3V to V _S NVP0.3	_{SYS} + 0.3V
AGND, DGND, PGND, GND0.3	V to +0.3V
Continuous Current into	
CHGIN, SYS	+6.4A
BAT	
Any Other Terminal	
Continuous Power Dissipation	
(multilayer board at +70°C): 9 x 6 Array 54-Bump,	
3.97mm x 2.77mm 0.4mm Pitch WLP	
(derate 24.46mW/°C)	1.957W
Operating Temperature Range40°C	
Junction Temperature	
Storage Temperature Range65°C	
Lead Temperature (soldering, 10s)	
Soldering Temperature (reflow)	

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

PACKAGE TYPE: 54 WLP				
Package Code	W151G2+1			
Outline Number	21-100122			
Land Pattern Number	Refer to Application Note 1891			
THERMAL RESISTANC, FOUR-LAYER BOARD				
Junction to Ambient (θ _{JA})	40.88°C/W			

For the latest package outline information and land patterns (footprints), go to www.maximintegrated.com/packages. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to www.maximintegrated.com/thermal-tutorial.

Electrical Characteristics

 $(V_{BAT} = 8.3V, T_A = -40^{\circ}C \text{ to } +85^{\circ}C, \text{ all registers in their default state, unless otherwise noted.}$ Typical values are at $V_{CHGIN} = 5.0V, V_{BAT} = 7.4V, T_A = +25^{\circ}C.)$ (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SUPPLY CURRENT						
BAT Supply Current	I _{BAT}	V _{CHGIN} = 0V or Floating, Type-C detection active		140		μA
	5,11	Low Power mode		25		μA
		V _{CHGIN} = +5V, T _A +25°C, ChgEn = 0		5.3		mA
CHGIN Supply Current	ICHG	V _{CHGIN} = +5V, T _A +25°C, Suspend Mode (FSUS = High)		0.98		mA
CHGIN TO BYP PATH						
Allowed CHGIN Input Voltage Range	V _{CHGIN_RNG}		0		28	V
CHGIN Detect	V _{BDET}	Rising	3.8	3.9	4.0	
Threshold	V _{BDET_F}	Falling	3.6	3.7	3.8	V
	V_{OVP}	Rising	5.59	5.66	5.72	V
CHGIN Overvoltage Threshold	V _{OVP_F}	Falling	5.56			V
Timochicia	V _{OVP_H}	Hysteresis		28		mV
CHGIN-BYP Resistance	R _{CHGIN_BYP}	V _{CHGIN} = 5V		45		mΩ
CHGIN-BYP Soft-Start Timeout	t _{BYP_SFTTO}	If V _{BYP} has not reached within 50mV of V _{CHGIN} at timeout, a fault is flagged by SysFlt of register 0x02.		100		ms
CHGIN-BYP Soft-Start Current	I _{BYP_SFT}			60		mA
CHGIN-BYP Soft-Start End Comparator	V _{BYP_SFTEND}		15	50	80	mV
CHGIN-BYP Overload Comparator	V _{BYP_OVL}		290	360	420	mV
		SpvChglLim[4:0] = 00100		0.4		
Input Current Limit	I _{LIM}	SpvChglLim[4:0] = 01110		1.5		Α
		SpvChglLim[4:0] = 11101		3		
Input Current Limit Programming Range	I _{LIM_RNG}		0.1		3	А
Input Current Limit Programming Step	I _{LIM_STEP}			100		mA
INTERNAL SUPPLIES						
Internal V _{CCINT} Regulator	V _{CCINT}	V _{CHGIN} = 5V, boost off	4.0	4.3	4.6	V
Boost Regulator BREG	V_{BREG}			4.3		V
V _{CCINT} UVLO		V _{CCINT} rising	3.1	3.4	3.7	
Threshold	V_{UVLO}	V _{CCINT} falling	3.0	3.3	3.6	V

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PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
V _{CCINT} UVLO Threshold Hysteresis	Vuvlo_HYS	Hysteresis		100		mV
		SfOutLvI = 1, V _{CHGIN} = 6V, I _{SFOUT} = 0	3.15	3.3	3.45	
SECULT LDO Voltago	W	SfOutLvI = 1, V _{CHGIN} = 6V, I _{SFOUT} = 15mA		2.95		V
SFOUT LDO Voltage	VsFout	SfOutLvI = 0, V _{CHGIN} = 6V, I _{SFOUT} = 0	5.0	5.25	5.5	V
		SfOutLvI = 0, VCHGIN = 6V, I _{SFOUT} = 15mA		4.9		
SFOUT Maximum Current	I _{SFOUT_MAX}		15			mA
Current Reduce Temperature	T _{CHG_LIM}			120		°C
Thermal Shutdown Temperature	T _{SHUTDOWN}			150		°C
Thermal Shutdown Hysteresis	T _{SHUTDOWN_H}			20		°C
	LO Threshold VBYPUVLO	BYPUVLO[2:0] = 000, V _{BYP} falling		3.8		
		BYPUVLO[2:0] = 001, V _{BYP} falling		3.9		V
		BYPUVLO[2:0] = 010, V _{BYP} falling		4.0		
BYP UVLO Threshold		BYPUVLO[2:0] = 011, V _{BYP} falling		4.1		
BTT GVEG TIMOGRAM	VBYPUVLO	BYPUVLO[2:0] = 100, V _{BYP} falling		4.2		
		BYPUVLO[2:0] = 101, V _{BYP} falling		4.3		
		BYPUVLO[2:0] = 110, V _{BYP} falling		4.4		
		BYPUVLO[2:0] = 111, V _{BYP} falling		4.5		
BYP UVLO Threshold Hysteresis	V _{BYPUVLO_} H			25		mV
		VPChg[2:0] = 000, V _{SYS} rising		5.9		
		VPChg[2:0] = 001, V _{SYS} rising		6.0		
		VPChg[2:0] = 010, V _{SYS} rising		6.1		
SYS UVLO (SYSOK)	V	VPChg[2:0] = 011, V _{SYS} rising		6.2		
Threshold	Vsysuvlo	VPChg[2:0] = 100, V _{SYS} rising		6.3		- V -
		VPChg[2:0] = 101, V _{SYS} rising		6.4		
		VPChg[2:0] = 110, V _{SYS} rising		6.5		
		VPChg[2:0] = 111, V _{SYS} rising		6.6		
SYS UVLO Threshold Hysteresis	V _{SYSUVLO_} H			500		mV

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PARAMETER	SYMBOL	CONDIT	TIONS	MIN	TYP	MAX	UNITS
BYP-SYS BOOST PATH		,		'			1
Switching Frequency	f _{BST_SW}				0.8		MHz
Maximum Input Current	I _{BST_MAX}	L = 2.2µH		3			А
Input Peak Current Limit	I _{BST_LIM_PK}				4.5		А
			00000		100		
			00001		200		
			00010		300		
			00011		400		
			00100	405	450	495	
			00101		600		
			00110		700		
			00111		800		
			01000		900		
			01001		1000		
			01010		1100		
			01011		1200		
	IILIM_F	CurLim1Frc = 1 , CurLim1Set[4:0] =	01100		1300		
			01101		1400		
			01110		1500		
Forced Input Current			01111		1600		mA
Limit			10000		1700		
			10001		1800		
			10010		1900		
			10011		2000		
			10100		2100		
			10101		2200		
			10110		2300		
			10111		2400		
			11000		2500		
			11001		2600		
			11010		2700		
			11011		2800		
			11100		2900		
			11101		3000]
			11110		3100		
			11111		3200		
Efficiency	EFF _{BST}	I _{SYS} = 1000mA, V _I L1 = Bourns SRP4	_{BAT} = 7.4V, 012TA-2R2M		91.6		%

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PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	
CVC D -+ \/- +	\/	Charger disabled		V _{BAT} + 0.4		V	
SYS Regulation Voltage	V _{SYS_REG}	Charger in precharge, V _{BAT} = 5V	V	V			
SYS Regulation Voltage Limit	V _{SYS_LIM}	See Battery Charger State Diagram		V _{SYS_REG} - 0.2			
BYP-SYS BUCK PATH							
Switching Frequency	f _{BK_SW}			0.8		MHz	
Maximum Output Current	I _{BK_MAX}	L = 2.2µH	500			mA	
Short-Circuit Peak Current Limit	I _{BK_LIM}			1.3		А	
Efficiency	EFF _{BK}	I _{CHGIN} = 500mA , V _{BAT} = 7.4V, L1 = Bourns SRP4012TA-2R2M		94		%	
Output Voltage Range	V _{BK_OUT_RNG}		4		5.5	V	
Output Accuracy	V _{BK_OUT_ACC}		-1.5		+1.5	%	
SYS-BAT CHARGER/SWI	TCH CONTROLLER						
BAT-to-SYS Regulation	V	MAX14748		-20		mV	
Voltage	V _{BAT-SYS} ON	MAX14748B		-40		IIIV	
BAT-to-SYS Switch Fast Turn-On Threshold	V _{BAT-SYS_OFF}	V _{SYS} falling		-100		mV	
BAT-to-SYS Switch On-Resistance	R _{BAT_SYS}	I _{BAT} = 1A		13		mΩ	
Charger Current Soft-Start Time	t _{CHG_SOFT}			1		ms	
PRECHARGE						1	
		IPChg[1:0] = 00		5			
Dracharga Current	1	IPChg[1:0] = 01		10		0/1	
Precharge Current	I _{PCHG}	IPChg[1:0] = 10		20		%lFCHG	
		IPChg[1:0] = 11, R_{SET} = 20kΩ	27	30	33		
		VPChg[2:0] = 000		5.7			
		VPChg[2:0] = 001		5.8			
		VPChg[2:0] = 010		5.9			
Prequalification	1/	VPChg[2:0] = 011		6.0		V	
Threshold	V _{PCHG}	VPChg[2:0] = 100		6.1		\ \ \	
		VPChg[2:0] = 101		6.2	6.2		
		VPChg[2:0] = 110	6.3			1	
		VPChg[2:0] = 111		6.4			
Prequalification Threshold Hysteresis	V _{PCHG_} H			100		mV	

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PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	
FAST CHARGE							
SET Current Gain Factor	K _{SET}			10000		A/A	
SET Regulation Voltage	V _{SET}			1		V	
		R _{SET} = 20kΩ	0.43	0.5	0.57		
F+ Ob		R _{SET} = 20kΩ, T = 25°C	0.475	0.5	0.525	1	
Fast-Charge Current	I _{FCHG}	R _{SET} = 10kΩ		1		A	
		R _{SET} = 4kΩ		2.5			
		T_T_IFChg[2:0] = 000		20			
		T_T_IFChg[2:0] = 001		30			
		T_T_IFChg[2:0] = 002		40			
Fast-Charge Current	1	T_T_IFChg[2:0] = 003		50		0/1	
Scaling	I _{FCHG_T}	T_T_IFChg[2:0] = 004		60		%lFCHG	
		T_T_IFChg[2:0] = 005		70			
		T_T_IFChg[2:0] = 006		80			
		T_T_IFChg[2:0] = 007		100]	
1/2 Fast-Charge Current Comparator Threshold	IFC_HALF			50		%lFCHG	
1/5 Fast-Charge Current Comparator Threshold	I _{FC_FIFTH}			20		%I _{FCHG}	
MAINTAIN CHARGE							
0		ChgDone[1:0] = 00		5			
Charge Done Qualification	I _{CHG_DONE}	ChgDone[1:0] = 01		10		%l _{FCHG}	
		ChgDone[1:0] = 10, R_{SET} = 20k Ω	18	20	22		
		BatReg[1:0] = 00, T _A = +25°C	8.258	8.3	8.342		
		BatReg[1:0] = 00, T _A = -40°C to +85°C	8.217	8.3	8.383		
BAT Regulation Voltage	V _{BATREG}	BatReg[1:0] = 01		8.4		V	
		BatReg[1:0] = 10		8.5			
		BatReg[1:0] = 11		8.6		1	
		BatReChg[1:0] = 00		200			
BAT Recharge	V	BatReChg[1:0] = 01		300		\/	
Threshold	V _{BATRECHG}	BatReChg[1:0] = 10		400		mV	
		BatReChg[1:0] = 11		500		1	

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PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
CHARGE TIMER						
		PChgTmr[1:0] =00		30		
Maximum		PChgTmr[1:0] = 01		60		1 .
Prequalification Time	^t PCHG	PChgTmr[1:0] = 10		120		- min
		PChgTmr[1:0] = 11		240		1
		FChgTmr[1:0] = 00		75		
Maximum Fast-Charge		FChgTmr[1:0] = 01		150		1
Time	^t FCHG	FChgTmr[1:0] = 10		300		Min
		FChgTmr[1:0] = 11		600		1
		MtChgTmr[1:0] = 00		0		
		MtChgTmr[1:0] = 01		15		1
Maintain Charge Time	^t TOCHG	MtChgTmr[1:0] = 10		30		— Min —
		MtChgTmr[1:0] = 11		60		
Timer Accuracy	tACC		-10		+10	%
Timer Extend Threshold	P _{TIMERX}	If charge current is reduced due to I _{LIM} or T _{DIE} , this is the percentage of charge current below which timer clock operates at half speed		50		%
Timer Suspend Threshold	PTIMERSUS	If charge current is reduced due to I _{LIM} or T _{DIE} , this is the percentage of charge current below which timer clock pauses		20		%
THERMISTOR MONITOR	AND NTC DETECTION	DN				
THM Hot Threshold	T4	V _{THM} falling, WarmCoolSel = 0	21.3	23.3	25.3	%V _{TPU}
Trim riot ringenera		V _{THM} falling, WarmCoolSel = 1	30.9	32.9	34.9	701110
THM Warm Threshold	Т3	V _{THM} falling, WarmCoolSel = 0	30.9	32.9	34.9	%V _{TPU}
Triwi vvaim miconola		V _{THM} falling, WarmCoolSel = 1	46.5	50	53.5	70 1 1 1 0
THM Cool Threshold	T2	V _{THM} rising, WarmCoolSel = 0 or 1	62.5	64.5	66.5	%V _{TPU}
THM Cold Threshold	T1	V _{THM} rising, WarmCoolSel = 0 or 1	71.9	73.9	75.9	%V _{TPU}
THM Disable Threshold	V _{THM_DIS}	V _{THM} rising	91.0	93.0	95.0	%V _{TPU}
THM Threshold Hysteresis	V _{THM_DIS_H}			60		mV
JEITA BAT Voltage Reduction	V _{BAT} _JEITA			300		mV
THM Input Leakage	ITHM_LK		-1		+1	μA
THM Detection Time	t _{THM_DET}			0.4		ms

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PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DIGITAL I/O (SDA, SCL, I	FLTIN, INT, SYSOK, F	SUS, LED, CDIR)	'			
Leakage Current	I _{IO_LK}		-1		+1	μA
Logic Input High-Voltage	V _{IO_IH}		1.4			V
Logic Input Low-Voltage	V _{IO_IL}				0.5	V
Logic Output Low-Voltage	V _{IO_OL}	I _{OL} = 4mA			0.4	V
FSUS Input Pulldown Resistance	R _{FSUS_PD}			470		kΩ
SDA, SCL Bus Low-Detection Current	I _{PD}	V _{SDA} = V _{SCL} = 0.4V		0.2	0.4	μA
SCL Clock Frequency	fscL	Note 2	0		400	kHz
Bus Free Time Between a STOP and START Condition	^t BUF		1.3			μs
START Condition (Repeated) Hold Time	t _{HD_SDA}	Note 2	0.6			μs
Low Period of SCL Clock	t _{LOW}		1.3			μs
High Period of SCL Clock	^t HIGH		0.6			μs
Setup Time for a Repeated START Condition	^t su_sta		0.6			μs
Data Hold Time	t _{HD_DAT}	Note 3	0		0.9	μs
Data Setup Time	tsu_dat	Note 3	100			ns
Setup Time for STOP Condition	t _{SU_STO}		0.6			μs
Spike Pulse Widths Suppressed by Input Filter	^t sp	Note 4		50		ns
BC1.2 DETECTION						
V _{DP_SRC} Voltage	V _{DP_SRC} /V _{SRC06}	I _{LOAD} = 0 to 200μA	0.5	0.6	0.7	V
V _{DM_SRC} Voltage	V _{DM_SRC} /V _{SRC06}	I _{LOAD} = 0 to 200μA	0.5	0.6	0.7	V
V _{D33} Voltage	V _{SRC33}	I _{LOAD} = 0 to 365μA	2.6		3.4	V
V _{DAT_REF} Voltage	V _{DAT_REF}		0.25	0.32	0.4	V
V _{LGC} Voltage	V_{LGC}		1.5	1.7	1.9	V
I _{DM_SINK} Current	I _{DM_SINK} /I _{DATSINK}	0.15V to 3.6V	55	80	105	μΑ
I _{DP_SRC} Current	I _{DP_SRC} /I _{DCD}	0V to 2.5V	7	10	13	μA

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PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
R _{DM_DWN} Resistor	R _{DM_DWN} /R _{DWN15}		12	20	24	kΩ
I _{WEAK} Current	I _{WEAK}		0.01	0.1	0.5	μA
V _{BUS31} Threshold	V _{BUS31}	DP and DN pins. Threshold in percent of V _{BUS} voltage 4V < V _{BUS} < 5.5V	26	31	36	%
V _{BUS47} Threshold	V _{BUS47}	DP and DN pins. Threshold in percent of V _{BUS} voltage 4V < V _{BUS} < 5.5V	43.3	47	51.7	%
V _{BUS64} Threshold	V _{BUS64}	DP and DN pins. Threshold in percent of V _{BUS} voltage 4V < V _{BUS} < 5.5V	57	64	71	%
Charger Detection Debounce	tCDDEB		45	50	55	ms
Primary-to-Secondary Timer	^t PDSDWAIT		27	35	39	ms
Proprietary Charger Debounce	t _{PRDEB}		5	7.5	10	ms
Data Contact Detect		DCD2s = 0	700	800	900	
Timeout	^t DCDTMO	DCD2s = 1	1.8	2.0	2.2	ms
DP/DN Overvoltage Debounce	t _{OVDXDEB}		90	100	110	μs
OVDX Comparator	OVDY	Rising	0		0.15	V
OVDA Comparator	OVDX _{THRESHOLD}	Falling	-0.04		+0.08	V
CDP/CDN Pulldown Resistor	R _{CDP/CDN_PD}		3	6	12	mΩ
TYPE-C DETECTION						
V _{CONN} Switch Voltage Drop	V _{CONN_REQ}	V _{CONN} = 5.5V, I _{CC_LOAD} = 20mA	5.5		5.6	V
V _{CONN} Bulk Capacitance	C _{VCONN}		10		220	μF
CC Pin Operational Voltage Range	V _{CONN_RNG}				5.5	V
CC Pin Voltage in DFP 3.0A Mode	V _{CC_PIN30}		3.1			V
CC Pin Voltage in DFP 1.5A Mode	V _{CC_PIN15}		1.85			V
CC Pin Low-Power Mode Pulldown Resistance	R _{LPPD_CC} _			170		kΩ

 $(V_{BAT} = 8.3V, T_A = -40^{\circ}C \text{ to } +85^{\circ}C, \text{ all registers in their default state, unless otherwise noted.}$ Typical values are at $V_{CHGIN} = 5.0V, V_{BAT} = 7.4V, T_A = +25^{\circ}C.)$ (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
CC Pin Low-Power Mode Voltage Threshold	V _{LP_CC} _	Rising		0.7		V
CC Pin Clamp Requirements	VCC_PIN_CLAMP	60μA ≤ I _{CC} _≤ 600μA		1.1	1.32	V
CC UFP Pulldown Resistance	R _{DUFP_CC_}		4.59	5.1	5.61	kΩ
CC DFP 0.5A Current Source	I _{DFP0.5} _CC_		72	80	88	μA
CC DFP 1.5A Current Source	I _{DFP1.5_CC_}		165.6	180	194.4	μA
CC DFP 3.0A Current Source	I _{DFP3.0_CC} _		303.6	330	356.4	μA
CC R _A and R _D	V	Rising	0.16	0.2	0.25	V
Threshold	V _{RA_RD0.5}	Falling	0.15			
CC UFP 0.5A R _D	\/	Rising	0.62	0.66	0.7	0.7 V
Threshold	V _{UFP_RD0.5}	Falling	0.61			
CC UFP 1.5A R _D	\/	Rising	1.17	1.23	1.31	V
Threshold	V _{UFP_RD1.5}	Falling	1.16]
CC V _{CONN} Detect	VVCONN_DET	Rising	2.11	2.25	2.4	V
Threshold		Falling	2.1			ľ
CC DFP V _{OPEN} Detect	\/	Rising	1.51	1.575	1.65	V
Threshold	V _{DFP_} VOPEN	Falling	1.5]
CC DFP V _{OPEN} with	V	Rising	2.46	2.6	2.75	V
3.0A Detect Threshold	V _{DFP_} VOPEN3A	Falling	2.45			V
V _{BUS} Valid	V_{BDET}	Rising	3.8	4.12	4.4	V
V _{BUS} Valid Hysteresis	V _{BDET_H}	Falling hysteresis		0.7		V
V _{BUS} Discharge Value	V _{SAFE0V}	Falling. Voltage level where a connected UFP will find V _{BUS} removed.	0.6	0.7	0.84	V
		Rising hysteresis		100		mV
CC Pin Power-Up Time	^t CLAMPSWAP	The maximum time allowed from removal of voltage clamp to attachment of the 5.1k resistor			15	ms
Type-C CC Pin Detection Debounce	tCCDEB		100		200	ms
Type-C Debounce	t _{PDDEB}		10		20	ms

 $(V_{BAT} = 8.3V, T_A = -40^{\circ}C \text{ to } +85^{\circ}C, \text{ all registers in their default state, unless otherwise noted. Typical values are at <math>V_{CHGIN} = 5.0V, T_{CHGIN} = 5.0V$ $V_{BAT} = 7.4V, T_A = +25^{\circ}C.)$ (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Type-C Quick Debounce	t _{QDEB}		0.9	1	1.9	ms
V _{BUS} Debounce	t _{VBDEB}		9	10	11	ms
V _{SAFE0V} Debounce	t _{VSAFE0VDEB}		9	10	11	ms
Type-C Error Recovery Delay	^t ERRORRECOVERY		25			ms
Type-C DRP Toggle Time	t _{DRP}		50		100	ms
Duty Cycle of DRP Swap	D _{DRP}	Duty cycle of UFP to DFP role swap	30		70	%
DRP Transition Time	^t DRPTRAN	Time a role swap from DFP to UFP or reverse is completed			1	ms
DRP Lock Time	^t DRPLOCK	DRP Lock wait time before transition to unattached state	100		150	ms
V _{CONN} Enable Time	^t VCONNON	Time from when V _{BUS} is supplied in DFP mode in state Attach.DFP. DRPWait			10	ms
V _{CONN} Disable Time	^t /CONNOFF	Time from UFP detached or as directed by I ² C command until V _{CONN} is removed			35	ms
CC Pin Current Change Time	[†] SINKADJ	Time from CC pin changes state in UFP mode until current drawn from DFP reaches new value			60	ms
V _{BUS} On-Time	^t VBUSON	Time from UFP is attached until V _{BUS} On			275	ms
V _{BUS} Off-Time	^t VBUSOFF	Time from UFP is detached until V _{BUS} reaches V _{SAFE0V}			650	ms
BVCEN Output Low-Voltage	V _{BVCEN_OL}	I _{SINK} = 1mA			0.4	V
BVCEN Output High-Voltage	V _{BVCEN_} OH	I _{SOURCE} = 1mA	VCCINT - 0.4			V

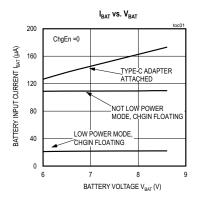
- Note 1: All devices are 100% production tested at $T_A = +25$ °C. Limits over the operating temperature range are guaranteed by design and characterization.
- Note 2: f_{SCL} must meet the minimum clock low time plus the rise/fall times.
- Note 3: The maximum $t_{\text{HD:DAT}}$ has to be met only if the device does not stretch the low period (t_{LOW}) of the SCL signal. Note 4: Filters on SDA and SCL suppress noise spikes at the input buffers and delay the sampling instant.

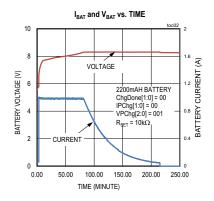
Maxim Integrated | 12 www.maximintegrated.com

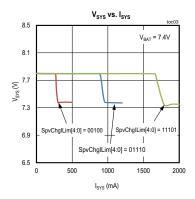
MAX14748

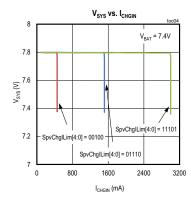
Typical Operating Characteristics

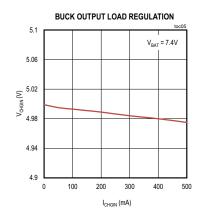
 $(V_{BAT} = 8.5V, T_A = -20^{\circ}C \text{ to } +70^{\circ}C, \text{ all registers in their default state, unless otherwise noted. Typical values are at <math>V_{CHGIN} = 5.0V, V_{BAT} = 7.4V, T_A = +25^{\circ}C.)$

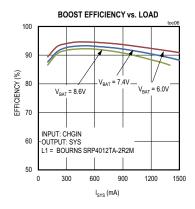


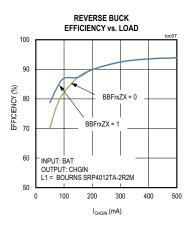


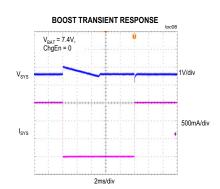


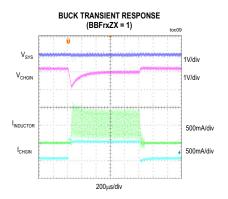






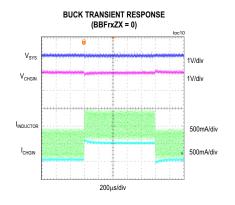


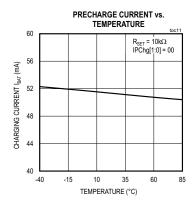


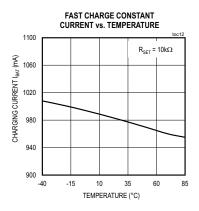


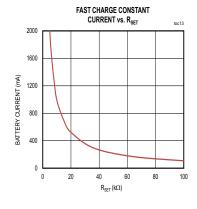
Typical Operating Characteristics (continued)

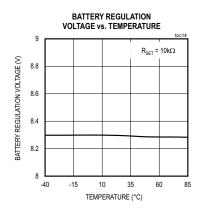
 $(V_{BAT} = 8.5V, T_A = -20^{\circ}C \text{ to } +70^{\circ}C, \text{ all registers in their default state, unless otherwise noted. Typical values are at <math>V_{CHGIN} = 5.0V, V_{BAT} = 7.4V, T_A = +25^{\circ}C.)$

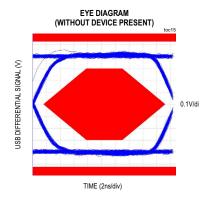


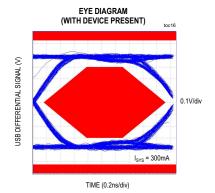




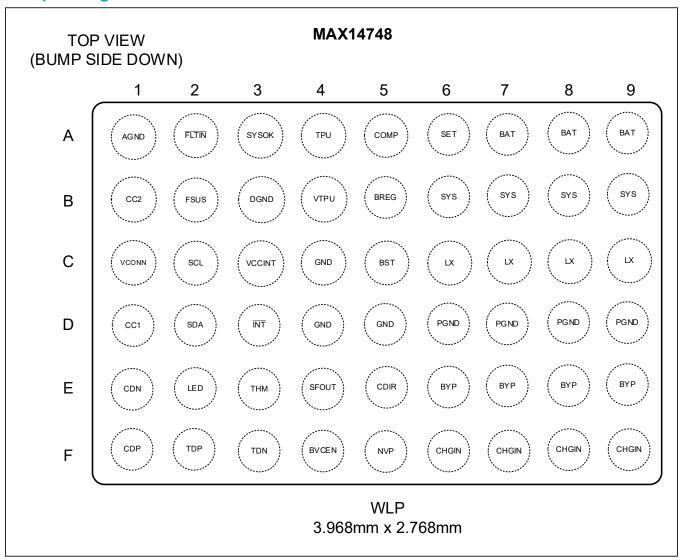








Bump Configuration



Bump Descriptions

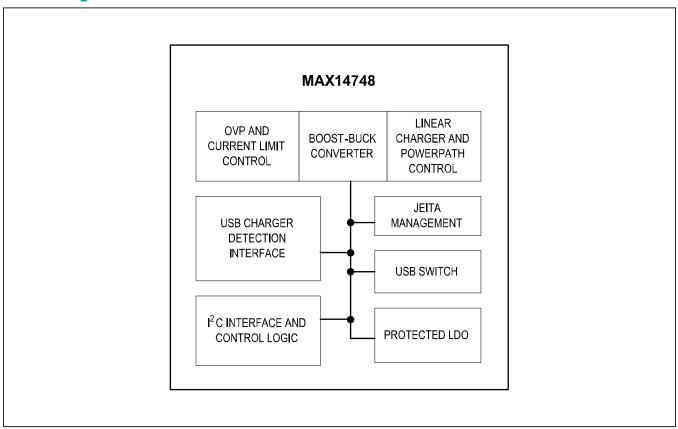
BUMP	NAME	FUNCTION
A1	AGND	Analog Ground.
A2	FLTIN	Charger Fault Input. Logic-low on this pin forces the charger into a fault state and generates an interrupt. See Register 0x35 description for more information. Connect to digital I/O supply if not used.
А3	SYSOK	Open-Drain Status Output of SYS Regulation. When V_{SYS} is above the SYS UVLO threshold and Boost is active, this output is high-impedance. When V_{SYS} is below the SYS UVLO threshold, this output is low. Leave unconnected if not used.
A4	TPU	High-Side of Internal Resistor for THM Detection. Connect a 10k resistor between this pin and THM.
A5	COMP	Buck/Boost Converter Compensation Connection. Connect a 3.9nF capacitor for internal Buck/Boost compensation
A6	SET	External Resistor Connection for Fast Charge Current Setting. Connect a resistor to this pin to set the fast charge current. Other charge currents are set as a proportion of fast charge current based on I ² C register settings.
A7–A9	BAT	Battery Connection. Connect a 2s Li-ion+ battery from BAT to GND. Bypass to PGND with a parallel combination of a 0.1μF capacitor and an effective 10μF - 30μF capacitor. Keep the capacitors as close to BAT as possible and keep the stray inductance and resistance of the trace from BAT to the battery terminal as low as possible.
B1	CC2	USB Type-C CC2. Connect to CC2 on USB Type-C connector.
B2	FSUS	Force Suspend Input. Logic-high on this pin causes the input limiter to open and input current from CHGIN is reduced to zero. This pin is internally pulled to GND through a $470k\Omega$ (typ) resistor and has no effect if FSUSMsk = 1.
В3	DGND	Digital Ground.
B4	V _{TPU}	External Voltage Input for TPU connection. Connect to external supply or V _{CCINT} .
B5	BREG	Bypass for Internal Switching Converter Supply. Bypass with 1µF capacitor to AGND.
B6-B9	SYS	System Load Connection. Connect SYS to the system load. Bypass to PGND with a parallel combination of a 0.1µF capacitor and an effective 22µF capacitor. (Note: there is a diode between SYS and BAT)
C1	V _{CONN}	External V _{CONN} Supply Input. Leave unconnected if not used.
C2	SCL	I ² C Serial Clock Input. Connect an external pull-up resistor.
C3	V _{CCINT}	Bypass For Internal Analog Supply. Bypass with 1µF capacitor to GND.
C4, D4, D5	GND	Ground.
C5	BST	Charge Pump Connection. Connect a 0.1µF capacitor between BST and LX.
C6, C7, C8, C9	LX	Switching Node of Boost Converter. Connect a 1.5µH or 2.2µH inductor between LX and BYP. See <i>Applications Information</i> section for more details.
D1	CC1	USB Type-C CC1. Connect to CC1 on USB Type-C connector.
D2	SDA	I ² C Serial Data Input/Output. Connect an external pullup resistor.
D3	ĪNT	Active-Low, Open-Drain Interrupt Output. Connect an external pullup resistor.
D6, D7, D8, D9	PGND	Power Ground.

Bump Descriptions (continued)

BUMP	NAME	FUNCTION
E1	CDN	USB Connector D-Input. Leave unconnected if not used.
E2	LED	LED Charging Status Indicator. Open-drain output indicating battery charging status. When LEDAuto = 1 and a temperature fault is detected, the output is pulsed at 50% duty cycle for a period of 1.5s. When a charge timer expires or SysFlt fault occurs, LED is pulsed at 50% for a period of 0.15s. When LEDAuto = 0, the open-drain output is controlled by the LEDCtrl bit. Connect this pin to GND if unused.
E3	ТНМ	Battery Temperature Thermistor Measurement Connection. This pin is used for NTC thermistor presence detection and JEITA compliant temperature control.
E4	SFOUT	Output of overvoltage protected LDO powered from CHGIN. Bypass SFOUT with a 1µF ceramic capacitor to GND.
E5	CDIR	USB Cable Orientation Open-drain Output. When CC1 is active, this output is pulled low. Otherwise, this output is high-impedance. Leave unconnected if not used.
E6-E9	BYP	Bypass Connection. Bypass to PGND with a parallel combination of a 0.1µF capacitor and an effective 10µF capacitor.
F1	CDP	USB Connector D+ Input. Leave unconnected if not used.
F2	TDP	USB Transceiver D+ Connection. Connect TDP to device microprocessor USB transceiver D+ line. Leave unconnected if not used.
F3	TDN	USB Transceiver D- Connection. Connect TDN to device microprocessor USB transceiver D- line. Leave unconnected if not used.
F4	BVCEN	External V _{CONN} Supply Enable Output. Push-pull output between V _{CCINT} and GND. Leave unconnected if not used.
F5	NVP	Negative Voltage PFET Gate Control. Leave unconnected if not used.
F6-F9	CHGIN	USB Charger Input. Bypass this pin with a 1µF capacitor to PGND.

Note: All capacitance values listed in this document refer to effective capacitance. Be sure to specify capacitors that will meet these requirements under typical system operating conditions taking into consideration the effects of voltage and temperature.

Block Diagram



Detailed Description

The MAX14748 is a battery charger with a Smart Power Selector that safely charges two Li+ cell in accordance with JEITA specifications*.

Input OVP

The MAX14748 CHGIN input is protected by an internal N-channel FET. The device monitors the voltage at CHGIN and, if CHGIN is greater than $V_{\rm OVP}$, switches off the internal FET to prevent damage to the device. If $V_{\rm CHGIN}$ is above the overvoltage threshold or below the USB valid voltage threshold, the MAX14748 enters overvoltage lockout (OVLO). During OVLO, the internal circuits remain powered, the SYSOK pin is high-impedance, and an interrupt is asserted. During OVLO, the charger turns off and the system load switch closes, allowing the battery to power SYS.

Negative Voltage Protection (NVP)

The MAX14748 provides a gate protection circuit for an external PFET that protects against negative voltages on V_{BUS} . NVP pin drives the gate of the external PFET. If a negative voltage is present on V_{BUS} (e.g., by a backwards connector) the NVP turns off the external PFET, therefore providing negative voltage protection.

Low Power Mode

The MAX14748 features a Low Power mode, which reduces the battery current consumption from $25\mu A$ to $140\mu A$. To enter Low Power mode, write 1 to LowPowEn (Register 0x33[7]). To manually exit Low Power mode, set LowPowAbort (Register 0x33[1]) to 1. If a DFP pullup connect to CC1/CC2 is detected, the device automatically exits Low Power mode and resumes normal operations.

Input Current Limiter

The primary function of the input limiter is supplying power from the external adapter at CHGIN to the system load and battery charger. In addition, it performs several other functions to optimize use of the available power efficiently and safely, including:

- 1) CHGIN Input Current Limiting: The CHGIN input current is limited to prevent input overload. The current limit can be automatically selected through charger detection to match the capabilities of the source. The result is indicated by SpvChgllim[4:0] in register 0x22. See <u>Table 1a</u> for more details. It can also be manually set through CurLim1Frc and CurLim1Set[4:0] in register 0x21. <u>Figure 1</u> illustrates how the current limit setting is selected.
- 2) Thermal Limiting: In case the die temperature exceeds the normal limit (T_{CHG_LIM}), the MAX14748 will attempt to limit temperature increase by reducing the input current at CHGIN. In this condition, the system load has priority over charger current, so the input current is first reduced by lowering the charge current. If the junction temperature continues to rise and reaches the maximum operating limit (T_{BUS_LIM}), no input current is drawn from CHGIN and the battery powers the entire system load.
- 3) Adaptive Battery Charging: While the system is powered from CHGIN, the charger draws power from SYS to charge the battery. If the total load exceeds the input current limit, the battery supplies supplemental current to the load.
- 4) Adaptive Input Current Limiting: If the MAX14748 input current limit is programmed in such a way that the adapter voltage collapses due to resistive drop, current limiting, or poor load transient response, the AICL loop allows the MAX14748 to regulate the input voltage above a value needed to ensure proper operation. Figure 2 illustrates high-level operation of the AICL block and associated parameters are found in the registers 0x2C to 0x2E.

^{*}JEITA (Japan Electronics and Information Technology Industries Association) Standard, A Guide to the Safe Use of Secondary Lithium Ion Batteries on Notebook–Type Personal Computers, April 20, 2007.

Table 1a. Automatic Input Current Limit Control

ChgTyp[1:0]	PrChgTyp[2:0]	CCIStat[1:0]	SDPMaxCur[1:0]	CDPMaxCur[1:0]	I _{LIM}	SpvChgllim[4:0]
"xx"	"xxx"	"11 = 3A"	"00"	"0"	3A	0x1D
"11 = 1.5A"	"xxx"	"11 = 3A"	"xx"	"x"	3A	0x1D
"xx"	"110 = 3A"	"xx"	"xx"	"x"	3A	0x1D
"xx"	"101 = 2.4A"	"00" or "01 = 500mA" or "10 = 1.5A"	"XX"	"x"	2.4A	0x17
"xx"	"100 = 2A" or "001 = 2A"	"00" or "01 = 500mA" or "10 = 1.5A"	"XX"	"x"	2A	0x13
"1x = 1.5A"	"000" or "010 = 500mA"	"00" or "01 = 500mA" or "10 = 1.5A"	"XX"	"x"	1.5A	0x0E
"1x = 1.5A"	"000" or "010 = 500mA" or "011 = 1A"	"10 = 1.5A"	"XX"	"x"	1.5A	0x0E
"xx"	"011 = 1A"	"00" or "01 = 500mA"	"XX"	"x"	1A	0x09
"01 = 500mA"	"000" or "010 = 500mA"	"00" or "01 = 500mA"	"xx"	"x"	0.5A	0x04
"01 = 500mA"	"000"	"10 = 1.5A" or "11 = 3A"	01	"x"	0.5A	0x04
"01 = 500mA"	"000"	"10 = 1.5A" or "11 = 3A"	10	"X"	1.0A	0x09
"01 = 500mA"	"000"	"10 = 1.5A" or "11 = 3A"	11	"x"	1.5A	0x0E
"10 = 1.5A"	"000"	"11 = 3A"	xx	"1"	1.5A	0x0E
"00"	"xxx"	"xx"	"xx"	"x"	NA	NA

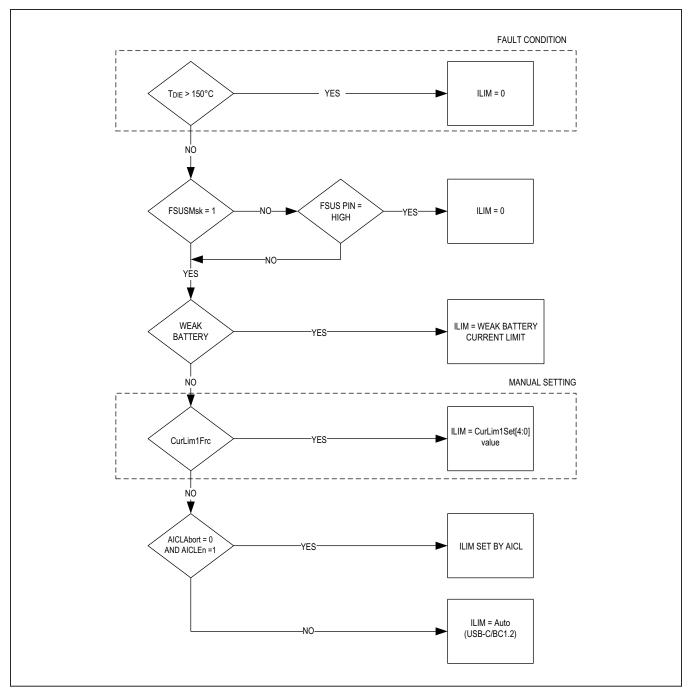


Figure 1. Input Current Limit Settings Flow Diagram

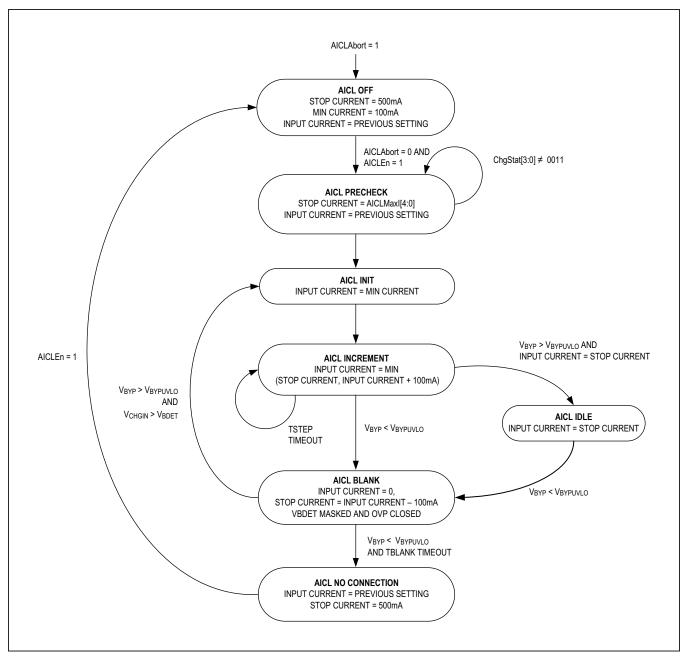


Figure 2. AICL Operation Flow Diagram

Boost Converter with Reverse Buck Boost Mode

The MAX14748 boost converter operates as either a current-limited voltage source, or current source, depending on the charger operational state. When a valid USB voltage is present at CHGIN, and the charger is disabled, V_{SYS} is regulated to $V_{BAT}\,+\,400\text{mV}.$ If the charger is in precharge mode, V_{SYS} is regulated to $V_{PCHG}\,+\,400\text{mV}.$ When the system is in fast-charge mode, the boost converter operates as a current source, delivering current into the SYS node that is shared by the battery and system loads.

The boost converter current limit may be acted upon by multiple system blocks, including the programmed input current limit, thermal status, charging current, SYS regulation voltage block, and battery termination voltage block. The minimum requested current from these blocks at any given time determines the active current limit in the boost.

Reverse Buck Mode

The CHGIN-SYS switching converter may operate as a buck converter when needed to supply a load attached to CHGIN. The load may be a Type-C sink or some other proprietary device.

If Type-C DRP operation is enabled, the buck converter can be enabled by the Type-C state machine. The output voltage of the buck can be programmed from 4V to 5.5V in 0.1V steps by writing to BuckVSet[3:0], however, it is not recommended to change the output voltage when the buck is active.

The output of the buck converter turns off when a fault occurs. The specific fault occurred is indicated by DCDCILim, DCDCRunAway, DCDCPGood status bits (register 0x04). See *I2C Register Descriptions* for more details. When the buck is disabled due to a fault, both VBUSDet (register 0x07) and VSAFE0V (register 0x0A) change to 0. After the fault condition is removed, the buck converter can be restarted by writing 1 to CCSnkRst, CCSrcRst, CCForceError, or USBCRset auto-reset bits.

Smart Power Selector

The Smart Power Selector seamlessly distributes power between CHGIN, battery (BAT) and the system (SYS). The basic modes of operation of the smart power selector are:

- 1. With a valid external power source:
 - The external power source at CHGIN is the primary source of energy.
 - b. The battery is the secondary source of energy.
 - c. Energy delivery to SYS is the highest priority.
 - d. Any energy that is not required by SYS is available to the battery.
- 2. With no power source available at CHGIN:
 - a. The battery is the primary source of energy.
 - b. Energy delivery to SYS has the highest priority.
- 3. With a Type-C Sink or other load present at CHGIN:
 - a. The battery is the primary source of energy.
 - b. Energy delivery to SYS is the highest priority.
 - c. Energy delivery to BYP is the second highest priority.

4. SYS Regulation Voltage:

- a. When the charger path is enabled and the charger is disabled, V_{SYS} is regulated to V_{BAT} + 400mV and BAT switch is off.
- b. When the charger is enabled but in a non-charging state such as maitain charge done, thermistor suspend, or timer fault, V_{SYS} is regulated to V_{BAT} + 400mV and BAT switch is off.
- c. When the input charger path is enabled and the battery is charging in prequalification, V_{SYS} is regulated to V_{PCHG} + 400mV. Charge current is reduced when V_{SYS} approaches V_{PCHG} + 200mV.
- d. When the input charger path is enabled and the battery is charging in fast-charge or maintain charge done, the BAT switch is closed and V_{SYS} = V_{BAT}. In maintain charge done state, the connection between SYS and BAT acts as an ideal diode. Therefore, when V_{SYS} drops below V_{BAT}, the BAT switch is turned fully on and the battery supplements the SYS load along with the current from CHGIN.
- e. When the switching converter is enabled as a reverse buck, the BAT switch is closed and V_{SYS} = V_{BAT}.

Short-Circuit Protection

The MAX14748 provides short-circuit protection to the power nodes. When SYS is shorted to ground, input current from CHGIN is limited by boost converter current limit. Note in this case, FET diode from BAT-SYS prevents control of FET BAT-SYS current. Battery current is not limited by the MAX14748 and a pack protector is needed to limit the battery current.

When either BYP or CHGIN is shorted to ground, the current from BAT is limited by the reverse buck converter.

USB Type-C 1.1

USB Type-C 1.1 UFP and DRP Support

The MAX14748 provides support for devices functioning as a Upstream Facing Port (UFP) or Dual Role Port (DRP) per the current USB Type-C 1.1 specification. When acting as a power source in DRP mode, the MAX14748 can provide a 5V VBUS on the CHGIN pin through operation of the reverse buck converter. The USB Type-C VCONN supply is provided externally via the VCONN pin, and switched internally onto one of the CC pins. An open-drain output pin, BVCEN, is provided to enable the external VCONN supply based on the Type-C state machine output. BVCEN is a push-pull output between GND and VCCINT.

USB BC1.2 Compliant and Nonstandard Charger Support

The BC1.2 charger detection and special charger detection routine is embedded within the Type-C state machine. The BC1.2 and Special Charger detection routine runs always when the state machine enters the 'AttachWait. SNK' state of the USB Type-C 1.1 state-machine.

USB Type-C Adapter Insertion

<u>Figure 3a</u> and <u>Figure 3b</u> depict the general timings when a USB Type-C adapter is attached. For more information on the behavior and timings of the USB Type-C 1.1 statemachine, please refer to the USB Type-C specification.

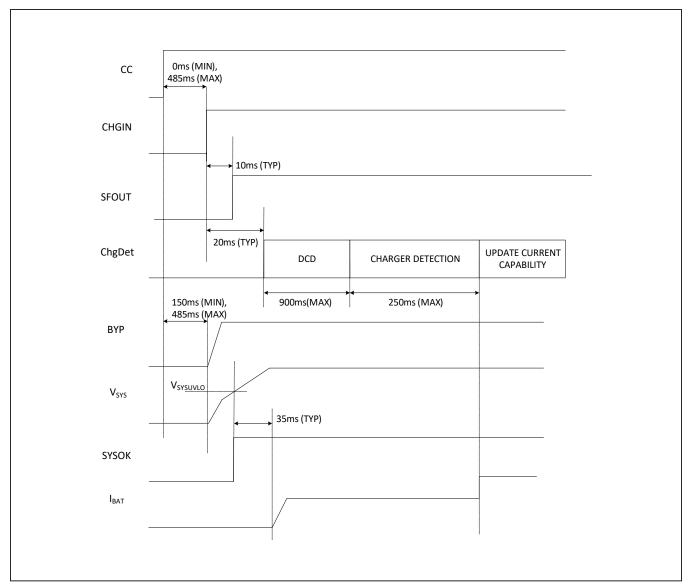


Figure 3a. Type-C Adapter Insertion (CHGINILimGate = 0)

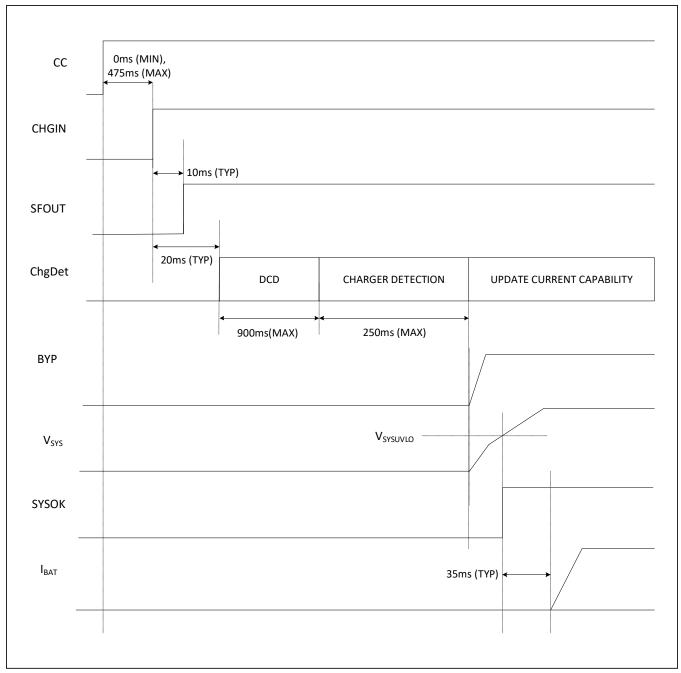


Figure 3b. Type-C Adapter Insertion (CHGINILimGate = 1)

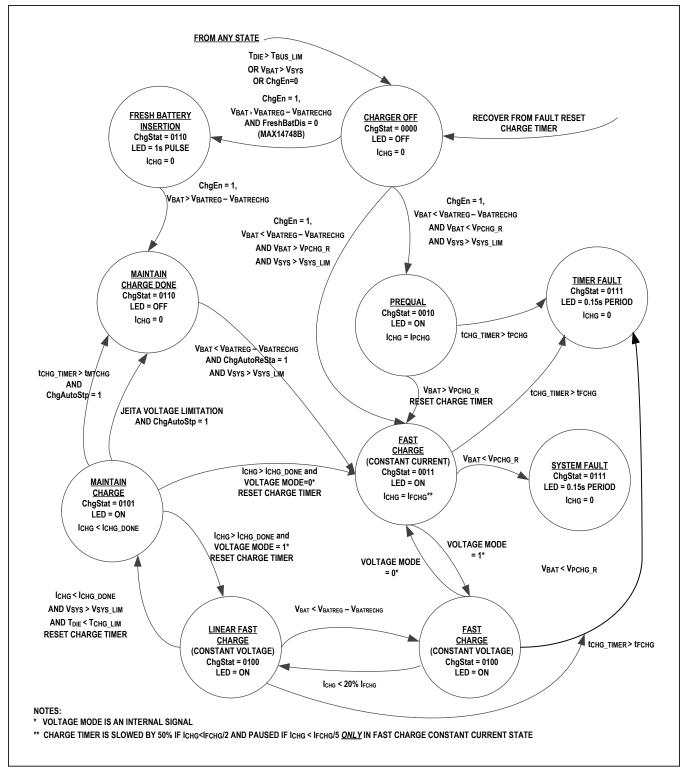


Figure 4. Battery Charger State Diagram

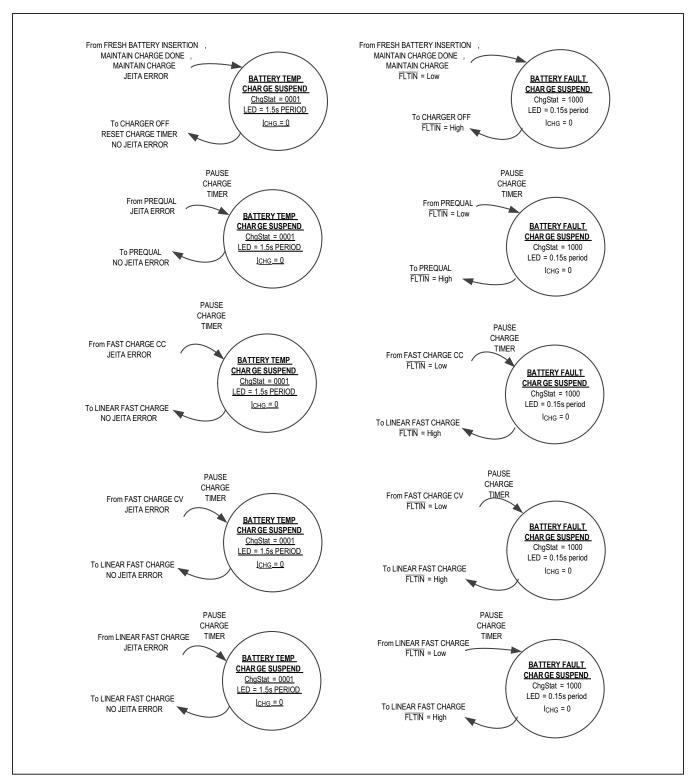


Figure 5. Battery Charger State Diagram (continued)

Li-ion Battery Charger

Charger Overview

The MAX14748 utilizes a boost converter to generate the necessary voltage to charge a 2s Li-ion battery from a nominal 5V USB charger input. Depending on the charging phase, the boost converter will operate as either a current-limited voltage source or current source. The charger is configured through a combination of external components and I²C registers settings. See Figure 4 and Figure 5 for the Battery Charger State Diagram. Note, for MAX14748, do not remove the battery while the charger is enabled (ChgEn=1).

Precharge

In precharge and charge termination phases, the boost converter functions as a current-limited voltage source and regulates V_{SYS} to V_{PCHG} +400mV. The battery is charged through an internal linear charging path with a maximum precharge current of 500mA (subject to thermal limitations), programmable through I²C. The precharge/fast-charge thresholds can be configured through register 0x1E and may not be less than the V_{OVP} (max).

Fast Charge

In the fast-charge phase, the boost converter functions as a current source delivering current into the SYS node. The SYS and BAT nodes are shorted together through the BAT-SYS FET, with a nominal resistance of $13m\Omega$ (typ). The fast-charge current is set by an external resistor, but may be modified by the T_T_IFchg[2:0] bits in registers 0x1A and 0x1B. The fast-charge current resistor can be calculated as $R_{SET} = K_{SET}/I_{FCHG}$, where K_{SET} has a typical value of 10000A/A. The range of acceptable resistors for R_{SET} is $3.3k\Omega$ to $100k\Omega$.

Charge Termination

During the charge termination phase, the battery current is monitored across the BAT-SYS FET. To prevent a 'false' termination of charge, the charge done condition is qualified by the state of the input current limit; if the input current limit is currently active, the charge done condition is not triggered. The charge done condition is also debounced for 140µs in order to prevent transient system currents from triggering an incorrect done condition.

Thermistor Monitoring

The MAX14748 provides highly programmable thermal/ JEITA charge management. All thermal/JEITA charge configuration parameters are set via the ThermCfg registers 0x1A - 0x1C. The charger is managed by thermal information only if JEITACtrSet = 1.

The battery pack temperature is measured from a divider formed by a pull-up resistor, an optional parallel resistor, and the battery pack thermistor. When required, the pullup resistor is connected to an internal supply through the TPU input, and the voltage on the THM pin is compared to an internal threshold. The supply voltage for the divider is applied to the V_{TPU} pin and may be connected to an external supply or to V_{CCINT}. The pullup resistor may be complemented with an additional parallel resistor to allow matching to different thermistor nominal values and charging cutoff temperatures, T1, T2, T3, and T4. There are two sets of cutoff temperatures optimized for a thermistor with Beta = 3380 (0°C/10°C/45°C/60°C or 0°C/10°C/25°C/45°C) which can be selected as factory default options. These cutoff temperatures divide the temperature range into three zones, T1_T2, T2_T3, and T3 T4. The charger is always turned off at temperatures outside these zones when any thermal monitoring mode is enabled. If the system needs to measure the THM temperature when not charging, the internal pullup switch may be enabled through the JeitaCfgR[1:0] bits.

Charging may be optionally disabled in the T1_T2 and T3_T4 zones through the T_T_EnSet bits. The charge current in each zone may be modified through T_T_IFchg[2:0]. Battery-voltage termination reduction may also be selectively applied through the T_T_VFset bits. See Figure 6 for more details.

Weak Battery Operation

The MAX14748 supports the weak battery provision of the USB 2.0 specification. If an SDP adapter is detected and the battery voltage is less than the precharge threshold, the input current limit is set to 500mA and a 2-minute timer starts. After the 2-minute timer expires, the input current limit is set to zero. Any time during the 2-minute countdown, the system may turn off the weak battery state machine and assert control of the input current limit by setting WeakBatEn to 0.

Battery Detection

The MAX14748 offers battery detection by detecting the presence of the battery thermistor. If the thermistor is not present, THM is pulled high by the external pullup resistor, and BatDet is set to 0 indicating that the battery is not connected.

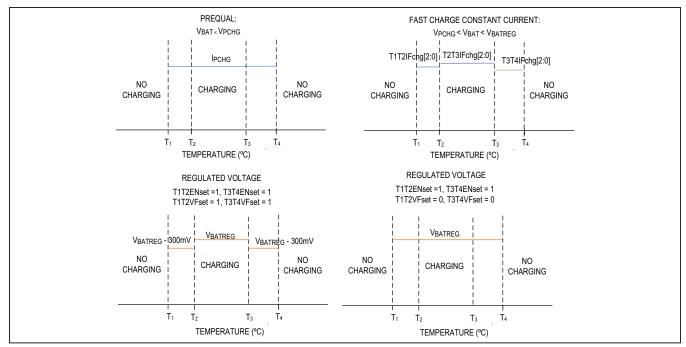


Figure 6. Thermistor Monitoring

Deeply Discharged Battery

Pack protectors that have a diode in series with the battery cell during recovery can cause the BAT voltage to rise above the precharge threshold of the charger. In the battery recovery state, if V_{CELL} + 0.6V > V_{PCHG} , the fast-charge state can be entered prematurely, eventually triggering a system fault. To avoid this issue in these pack protectors, ChgEn bit of ChargerCtr1 register (0x1D) can be controlled by the application processor in a manner such that charger does not enter fast charge mode until the battery pack successfully recovers from the deeply discharged state. The recommendation is to set ChgEn to 1 for 60ms to charge the battery in precharge mode followed by resetting ChgEn to 0 for 1ms to prevent the charger from entering fast-charge mode prematurely. This 60ms/1ms combination should be repeated until the battery pack successfully recovers. The total time to a successful recovery can be shortened by using a higher fast-charge current level IFCHG and a higher precharge current setting IPCHG. It is also recommended to use the highest setting for the prequalification threshold VPCHG.

Integrated USB 2.0 Analog Switch

A high-speed USB switch is integrated to provide the host data access to the connected USB device when an SDP or CDP port is detected. The analog switch may be controlled manually or automatically by configuring the AnSwCntl[1:0] bits in register 0x2F. When the analog switch control is set to the auto control setting then the CDN/CDP pins are connected to TDN/TDP only when a SDP or CDP port is detected. (See <u>I2C Register Descriptions</u> for further details.)

SFOUT LDO

The SFOUT LDO is powered directly from the CHGIN input and may be used to power a USB transceiver, or as an indicator signal that a SDP/CDP port is present. The LDO will operate with CHGIN voltages greater than V_{BDET} . The output voltage of SFOUT is selectable as either 5V or 3.3V through the SfOutLvI bit, depending on the system preference. SFOUT may be programmed to turn on automatically when an SDP or CDP is detected, or placed in manual mode and turned on through an I²C command. This supply is always available when CHGIN is present.

Internal Supplies and Regulators

The MAX14748 has two internal power supplies: V_{CCINT} and BREG. V_{CCINT} and BREG are always present when CHGIN or BAT is present. These supplies share a common source, but bypassed separately. The V_{CCINT} and BREG supplies require external bypass capacitors and are regulated to a nominal value of 4.3V (typ).

Device Control Interface

While the MAX14748 is primarily controlled by I²C, GPIO control is also offered for specific functions. The following GPIO control signals are provided (note that these signals only apply when CHGIN is present):

- FSUS (Input): Force Suspend. This pin enables the host microcontroller to force the input current limit to zero. When CHGIN is present, a logic-high on the pin causes the input OVP FET at CHGIN to open and the input current to MAX14748 is reduced to less than 2mA. This pin has no effect if FSUSMsk = 1.
- FLTIN (Input): Battery Fault Input. This pin allows the system or battery pack to place the charger into a fault condition using a GPIO pin. See Register 0x35 description for more details.
- 3) CDIR (Open-Drain Output): USB Superspeed MUX control. In USB Type-C plug configurations, it is necessary to detect the orientation of the connector and route the Superspeed lines accordingly. The pin can be used to automatically configure a USB Superspeed MUX according to the orientation information contained in the integrated Type-C detection block. (This information is also available through I²C) The

- CDIR output is pulled to GND when the CC1 pin is active on the Type-C connector, otherwise it is high-impedance.
- 4) SYSOK (Open-Drain Output): With CHGIN present, the SYSOK output is asserted if the boost regulator generates a V_{SYS} greater than SYS UVLO threshold, V_{SYSUVLO}. Otherwise, the output is high-impedance. This pin can be used as wake up the host system from a dead-battery. Note that when V_{SYS} falls below the SYS UVLO falling threshold, the input OVP switch is opened as the boost converter cannot operate in this state.
- 5) BVCEN (Open-Drain Output): When CHGIN is present and a Type-C device that requires V_{CONN} is found, this pin is asserted. This pin should be connected to the enable pin of the V_{CONN} power supply enable. The output of BVCEN is push-pull between GND and V_{CCINT}.

System Faults

The MAX14748 monitors the system for faults including OVP Soft Start Timeout, SYS UVLO, Direct Charging Fault, Charger Tlmeout, Forced Charger Fault, Dead Battery, CHGIN OVP. See Table 1b for more details.

Table 1b. System Faults Summary

FAULT NAME	EFFECT	CAUSE DESCRIPTION	HOW TO RECOVER	STAUS BIT
OVP Soft-Start TimeOut	System Fault Condition Latched. OVP/Boost/Charger Off	UFP: V _{BYP} is not within 50mV of V _{CHGIN} at Soft Start TimeOut (100ms typ)	Unplug/Replug Type-C cable or reset device via USBCRSet of Reg 0x30	SysFit (Reg 0x02)
SYS UVLO	System Fault Condition Latched. OVP/Boost/Charger Off	UFP: V _{SYS} falls below SYS UVLO threshold while in Boost mode or V _{SYS} fails to reach above SYS UVLO threshold within 20ms after V _{BYP} rises	Unplug/Replug Type-C cable or resert device via USBCRSet of Reg 0x30	SysFlt (Reg 0x02)
Direct Charging Fault	Charger Fault Condition Latched. Charger Off	UFP: V _{BAT} falls below V _{PCHG} while in Fast Charge mode	Cycle ChgEn or treat as System Fault	DirChgFault (Reg 0x05)
Charger Timeout	Charger Fault Condition Latched. Charger Off	UFP: Pre-charge or Fast- charge Timer expires	Cycle ChgEn or treat as System Fault	ChgStat[3:0] (Reg 0x05)
Forced Charger Fault	Charger Off	UFP: Logic-low applied on FLTIN pin	Logic-high applied on FLTIN pin	ChgStat[3:0] (Reg 0x05)
Dead Battery	System Fault Condition Latched. OVP/Boost/Charger Off	UFP: DeadBattery detection enabled and SDP detected: V _{BAT} fails to reach above V _{PCHG} within 2min	Treat as System Fault or disable DeadBattery	WbChg (Reg 0x02)
CHGIN OVP	OVP/Boost/Charger OFF	V _{CHGIN} rises above V _{OVP}	Reduce V _{CHGIN} below V _{OVP_F}	ChginOVP (Reg 0x02)

I²C Interface

The MAX14748 contains an I²C-compatible interface for data communication with a host controller (SCL and SDA). The interface supports a clock frequency of up to 400kHz. SCL and SDA require pullup resistors that are connected to a positive supply.

Start, Stop, And Repeated Start Conditions

When writing to the MAX14748 using I²C, the master sends a START condition (S) followed by the MAX14748 I²C address. After the address, the master sends the register address of the register that is to be programmed. The master then ends communication by issuing a STOP condition (P) to relinquish control of the bus, or a REPEATED START condition (Sr) to communicate to another I²C slave. See Figure 7.

Table 2. I2C Slave Addresses

ADDRESS FORMAT	HEX	BINARY
7-Bit Slave ID	0x0A	0001010
Write Address	0x14	00010100
Read Address	0x15	00010101

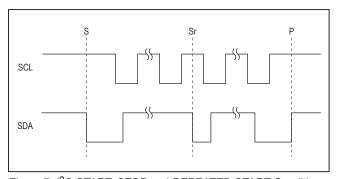


Figure 7. I²C START, STOP and REPEATED START Conditions

Slave Address

Set the Read/Write bit high to configure the MAX14748 to read mode (Table 2). Set the Read/Write bit low to configure the MAX14748 to write mode. The address is the first byte of information sent to the MAX14748 after the START condition.

Bit Transfer

One data bit is transferred on the rising edge of each SCL clock cycle. The data on SDA must remain stable during the high period of the SCL clock pulse. Changes in SDA while SCL is high and stable are considered control signals (see the <u>Start, Stop, And Repeated Start Conditions</u> section). Both SDA and SCL remain high when the bus is not active.

Single-Byte Write

In this operation, the master sends an address and two data bytes to the slave device (Figure 8). The following procedure describes the single byte write operation:

- 1) The master sends a START condition
- 2) The master sends the 7-bit slave address plus a write bit (low)
- 3) The addressed slave asserts an ACK on the data line
- 4) The master sends the 8-bit register address
- 5) The slave asserts an ACK on the data line only if the address is valid (NAK if not)
- 6) The master sends 8 data bits
- 7) The slave asserts an ACK on the data line
- 8) The master generates a STOP condition

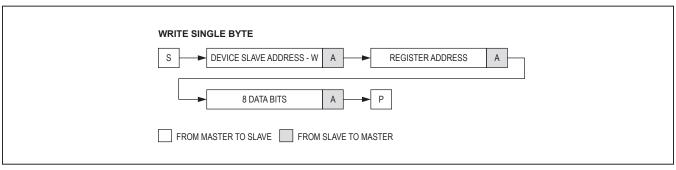


Figure 8. Write Byte Sequence

Burst Write

In this operation, the master sends an address and multiple data bytes to the slave device (Figure 9). The slave device automatically increments the register address after each data byte is sent. The following procedure describes the burst write operation:

- 1) The master sends a START condition.
- 2) The master sends the 7-bit slave address plus a write bit (low).
- 3) The addressed slave asserts an ACK on the data line.
- 4) The master sends the 8-bit register address.
- 5) The slave asserts an ACK on the data line only if the address is valid (NAK if not).
- 6) The master sends eight data bits.
- 7) The slave asserts an ACK on the data line.
- 8) Repeat 6 and 7 N-1 times.
- 9) The master generates a STOP condition.

Single-Byte Read

In this operation, the master sends an address plus two data bytes and receives one data byte from the slave device (Figure 10). The following procedure describes the single byte read operation:

- 1) The master sends a START condition.
- The master sends the 7-bit slave address plus a write bit (low).
- 3) The addressed slave asserts an ACK on the data line.
- 4) The master sends the 8-bit register address.
- 5) The slave asserts an ACK on the data line only if the address is valid (NAK if not).
- 6) The master sends a REPEATED START condition.
- 7) The master sends the 7-bit slave address plus a read bit (high).
- 8) The addressed slave asserts an ACK on the data line.
- 9) The slave sends eight data bits.
- 10) The master asserts a NACK on the data line.
- 11) The master generates a STOP condition.

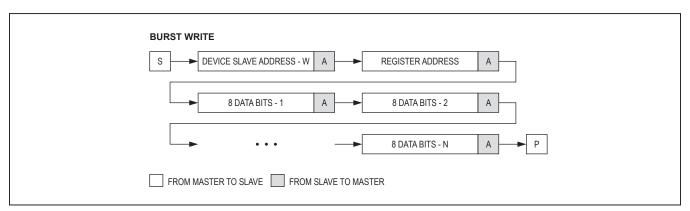


Figure 9. Burst Write Sequence

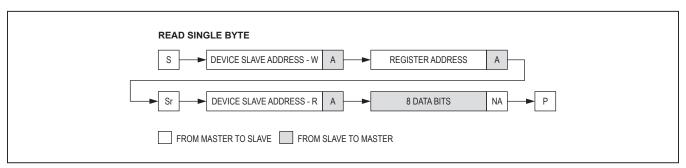


Figure 10. Read Byte Sequence

Burst Read

In this operation, the master sends an address plus two data bytes and receives multiple data bytes from the slave device (<u>Figure 11</u>). The following procedure describes the burst byte read operation:

- 1) The master sends a START condition.
- The master sends the 7-bit slave address plus a write bit (low).
- 3) The addressed slave asserts an ACK on the data line.
- 4) The master sends the 8-bit register address.
- 5) The slave asserts an ACK on the data line only if the address is valid (NAK if not).
- 6) The master sends a REPEATED START condition.
- 7) The master sends the 7-bit slave address plus a read bit (high).
- 8) The slave asserts an ACK on the data line.

- 9) The slave sends eight data bits.
- 10) The master asserts an ACK on the data line.
- 11) Repeat 9 and 10 N-2 times.
- 12) The slave sends the last eight data bits.
- 13) The master asserts a NACK on the data line.
- 14) The master generates a STOP condition.

Acknowledge Bits

Data transfers are acknowledged with an acknowledge bit (ACK) or a not-acknowledge bit (NACK). Both the master and the MAX14748 generate ACK bits. To generate an ACK, pull SDA low before the rising edge of the ninth clock pulse and hold it low during the high period of the ninth clock pulse (see Figure 12). To generate a NACK, leave SDA high before the rising edge of the ninth clock pulse and leave it high for the duration of the ninth clock pulse. Monitoring for NACK bits allows for detection of unsuccessful data transfers.

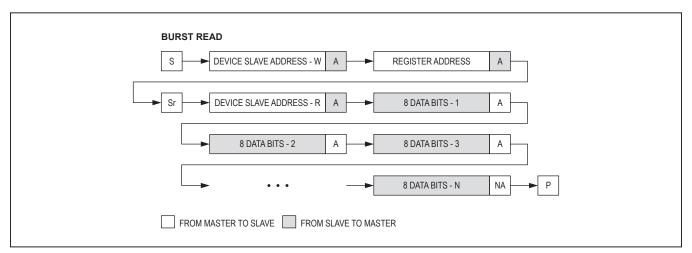


Figure 11. Burst Read Sequence

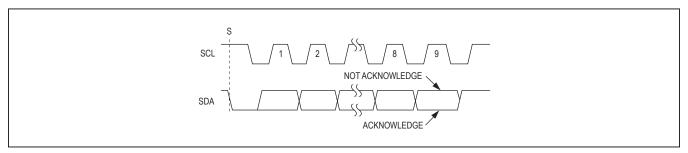


Figure 12. Acknowledge

REGISTER ADDRESS	REGISTER NAME	R/W	B7	B6	B5	B4	B3	B2	B3	B0
00×00	ChipID	œ				Ċ	ChipId[7:0]			
0x01	ChipRev	œ		Chip	ChipRevH[3:0]			ChipR	ChipRevL[3:0]	
0×02	DevStatus1	œ	SysFlt	ChglnOVP	ILim	VSysReg	ThrmSd150	ThrmSd120	BatDet	WbChg
0x03	AICLStatus	œ		AICLStatus[2:0]			d	AICLCurSet[4:0]		
0×04	DevStatus2	œ	I	BattPREQB	ı	BypUVLO	SysUVLOB	DCDCILim	DCDCRunAway	DCDCPGood
0x05	ChgStatus	œ	DirChgFault	ı	LowPow	ı		ChgS	ChgStat[3:0]	
90×0	JEITAStatus	œ	ı	ı	I	ChgThrmRegCur	ChgThrmRegVlt		ChgThrmStat[2:0]	
0×07	BCStatus	~	VBUSDet	ChgTypRun		PrChgTyp[2:0]		DCDTmo	ChgTyp[1:0]	[1:0]
0×08	Reserved	~	I	I	I	ı	I	I	I	I
60×0	CCStatus1	œ	CCPint	CCPinStat[1:0]	100	CCIStat[1:0]	CCVcnStat		CCStat[2:0]	
0x0A	CCStatus2	œ	1	ı	I	ı	VSAFE0V	DetAbrt	ı	I
0x0B	DevInt1	COR	SysFItI	ChglnOVPI	lLiml	VSysRegI	ThrmSd1501	ThrmSd1201	BatDetl	WbChgl
0x0C	AICLInt	COR	I	AICLI	ı	ı	I	ı	ı	ı
0x0D	DevInt2	COR	I	BattPREQi	I	BypUVLOI	SysUVLOI	I	I	DCDCPGoodl
0x0E	ChgInt	COR	DirChgFaultl	LowPowRI	LowPowFl	ı	I	ı	ı	ChgStatl
0x0F	JEITAInt	COR	I	ı	1	ChgThrmRegCurl	ChgThrmRegVltl	ı	ı	ChgThrmStatl
0x10	BCInt	COR	VBUSDetl	ı	1	ChgTypRunFl	ChgTypRunRl	PrChgTypl	DCDTmol	ChgTypl
0x11	CCInt	COR	ı	VSAFEOVI	DetAbrtl		CCPinStatl	CCIStatl	CCVcnStatl	CCStatl
0x12	DevInt1Mask	R/W	SysFitIM	ChglnOVPIM	ILimIM	VSysRegIM	ThrmSd150IM	ThrmSd120IM	BatDetIM	WbChgIM
0x13	AICLIntMask	R/W	I	AICLIM	ı	ı	I	ı	I	I
0x14	DevInt2Mask	R/W	I	BattPREQIM	I	BypUVLOIM	SysUVLOIM	DCDCILimIM	DCDCRunAwayIM	DCDCPGoodIM
0x15	ChglntMask	R/W	DirChgFaultlM	LowPowRIM	LowPowFIM	I	ı	ı	I	ChgStatIM
0x16	JEITAIntMask	R/W	I	I	I	ChgThrmReg CurlM	ChgThrmReg VItIM	I	I	ChgThrmStatIM
0x17	BCIntMask	R/W	VBUSDetIM	ı	ı	ChgTypRunFIM	ChgTypRunRIM	PrChgTypIM	DCDTmolM	ChgTypIM
0x18	CCIntMask	R/W	1	VSAFE0VIM	DetAbrtIM	I	CCPinStatIM	CCIStatIM	CCVcnStatIM	CCStatIM
0x19	LED_CTRL	R/W	I	ı	ı	ı	I	ı	LEDCtrl	LEDManual
0x1A	ThermaCfg1	R/W		T1T2IFchg[2:0]			T2T3IFchg[2:0]		JeitaCfgR[1:0]	R[1:0]
0x1B	ThermaCfg2	R/W		T3T4IFchg[2:0]		ı	T3T4ENset	T1T2ENset	T3T4VFset	T1T2VFset
0x1C	ThermaCfg3	R/W	ı	ı	-	ı	ı	ı	JEITACtrSet	WarmCoolSel*
0x1D	ChargerCtrl1	R/W**	ChgAutoStp	BatReC	BatReChg[1:0]	FreshBatDis (MAX14748B)	I	Batl	BatReg[1:0]	ChgEn
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REGISTER ADDRESS	REGISTER NAME	R/W	B7	B6	B5	B4	B3	B2	B1	B0
0x1F	ChargerCtrl3	R/W*	ı	ChgAutoSta	MtChç	MtChgTmr[1:0]	FChgTmr[1:0]	r[1:0]	PChgTmr[1:0]	nr[1:0]
0x20	ChargerCtrl4	R/W*		WeakBatStat[2:0]*	*	ı	I	WeakBatEn	I	ı
0x21	CurLimCtrl	R/W	CurLim1Frc	FSUSMsk				CurLim1Set[4:0]		
0x22	CurLimStatus	œ		CurLim2Rb[2:0]			0)	SpvChglLim[4:0]		
0x23	BBCFG1	R/W*		Boost	BoostRComp[3:0]		I	ı	I	ı
0x24	BBCFG2	R/W*	ı	ı	ı	BBFrcZX		BuckV	BuckVSet[3:0]	
0x25	BCCtrl1	R/W	DCD2s	SfOutLvI	1	ADC3PDet	SfOutCtrl[1:0]	1[1:0]	ChgDetMan	ChgDetEn
0x26	Reserved	82	ı	I	I	Ι	I	ı	-	ı
0x27	CCCtrl1	R/W	1	ı	ı	CCSrcSnk	CCSnkSrc	CCDbgEn	CCAudEn	CCDetEn
0x28	CCCtrl2	R/W	CCForceError	SnkAttached Lock	CCSnkSrcSwp	CCSrcSnkSwp	CCVcnSwp	CCVcnEn	CCSrcRst	CCSnkRst
0x29	CCCtrl3	R/W	I	I	I	_	CCTrySnk	CCPreferSnk	CCDRPPhase[1] CCDRPPhase[0]	hase[1] hase[0]
0x2A	CHGINILim1	<u>~</u>	ı				CHGINILim[6:0]			
0x2B	CHGINILim2	R/W	ı	ı	ı	_	CHGINILimGate	SDPM	SDPMaxCur[1:0]	CDPMaxCur
0x2C	AICLCFG1	R/W	AICLEn	I	I	I	I			AICLAbort
0x2D	AICLCFG2	R/W		BYPUVLO[2:0]				AICLMaxl[4:0]		
0x2E	AICLCFG3	R/W	ı	I	I	BYPDeb	AICLTBIK[1:0]	(1:0]	AICLTStep[1:0]	[0:1]de
0x2F	DPDNSw	R/W	ı	I	ı	-	ı	ı	AnSwCntl[1:0]	nt[[1:0]
0x30	Others	R/W	ı	ı	ı	_	-	ı	I	USBCRset
0x31	Reserved	X	ı	ı	ı	_	ı	ı	I	ı
0x32	Reserved	Я	ı	ı	ı	_	-	ı	I	ı
0x33	LowPow	R/W	LowPowEn	I	ı	_	ı	ı	I	LowPowAbort
0x34	Reserved	α.	-	1	I	_	_	ı	I	1
0x35	FLTSel	R/W	FLTSel	FLTSelect[1:0]	I	I	I	ı	I	I

Note:

COR = Clear-on-read
* Read Only
** Read Only if WriteProtect is enabled (See Table 61).
- Reserved bits must not be modified from their default states to ensure proper operation.

I²C Register Descriptions

Table 4. ChipID Register (0x00)

ADDRESS:	0x00							
MODE:	Read Only							
BIT	7	6	5	4	3	2	1	0
NAME				Chipl	d[7:0]			
ChipId[7:0]	Chipld[7:0] bi	ts show inforn	nation about th	e version of th	e MAX14748.			

Table 5. ChipRev Register (0x01)

ADDRESS:	0x01							
MODE:	Read Only							
BIT	7	6	5	4	3	2	1	0
NAME		ChipRe	evH[3:0]			ChipRe	evL[3:0]	
ChipRevH[3:0]	ChipRevH[3:0)] bits show in	formation abo	ut the revision	of the MAX147	48 silicon.		
ChipRevL[3:0]	ChipRevL[3:0] bits show in	formation abou	ut the revision o	of the MAX147	48 silicon.		

Table 6. DevStatus1 Register (0x02)

ADDRESS:	0x02									
MODE:	Read Only									
BIT	7	6	5	4	3	2	1	0		
NAME	SysFlt	ChgInOVP	ILim	VSysReg	ThrmSd150	ThrmSd120	BatDet	WbChg		
SysFlt	0 = System v	System Fault 0 = System voltage is normal 1 = SYS voltage below SYS UVLO Threshold and the condition latched.								
ChglnOVP	0 = CHGIN (CHGIN Overvoltage Protection Flag 0 = CHGIN OVP not active 1 = CHGIN OVP active								
ILim	0 = CHGIN i	Input Current Limiting 0 = CHGIN input current within limit 1 = CHGIN input in current limit								
VSysReg	0 = SYS volt			shold and boost hold or Boost n						
ThrmSd150		tdown n normal operat n thermal shutd		150°C)						
ThrmSd120		rm n normal operat T _{DIE} < 150°C	ion Mode							
BatDet	Status of Bar 0 = No batte 1 = Battery of	•								
WbChg		y Charging attery Charge T attery Charge T		or not running						

Table 7. AICLStatus Register (0x03)

ADDRESS:	0x03										
MODE:	Read Only										
BIT	7	7 6 5 4 3 2 1 0									
NAME	,	AICLStatus[2:0] AICLCurSet[4:0]									
AICLStatus[2:0]	001 = AICL F 010 = AICL II 011 = AICL B 100 = AICL I	AICL Status 000 = AICL Off 001 = AICL Precheck 010 = AICL Increment 011 = AICL Blank 100 = AICL Idle 101 = AICL No Connection									
AICLCurSet[4:0]	Current limit 0 = 100mA 1 = 200mA 30 = 3.1A 31 = 3.2A	set by AICL (if	factive)								

Table 8. DevStatus2 Register (0x04)

ADDRESS:	0x04								
MODE:	Read	Only							
BIT	7	6	5	4	3	2	1	0	
NAME	-	BattPREQB	-	BypUVLO	SysUVLOB	DCDCILim	DCDCRunAway	DCDCPGood	
BattPREQB	Battery 0 = V _B	V_{BAT} vs. V_{PCHG} (V_{PCHG} programmable from 5.7V to 6.4V, BattPreqB status is NOT valid while the Weak Battery 2min timer is running.) $0 = V_{BAT}$ below V_{PCHG} threshold $1 = V_{BAT}$ above V_{PCHG} threshold							
BypUVLO	0 = V _B	$V_{\rm BYP}$ vs. $V_{\rm BYPUVLO}$ ($V_{\rm BYPUVLO}$ programmable from 3.8V to 4.5V) 0 = $V_{\rm BYP}$ above $V_{\rm BYPUVLO}$ the shold 1 = $V_{\rm BYP}$ below $V_{\rm BYPUVLO}$ the shold							
SysUVLOB	mode v	vs. V _{SYSUVLO} (with CHGIN pre _{SYS} below V _{SYS} _{SYS} above V _{SYS}	esent)) _{UVLO} thresho	ld	from 6.1V to 6.	8V, SysUVLO	B status is only vali	d in boost	
DCDCILim	0 = No	se Buck Conver ormal Operation ock current limit							
DCDCRunAway	Reverse Buck Converter Runaway Status 0 = Normal Operation 1 = Buck runaway is asserted								
DCDCPGood	0 = Bu	se Buck Conver ck regulated va ormal operation	_		t value				

Table 9. ChgStatus Register (0x05)

ADDRESS:	0x05							
MODE:	Read Only							
BIT	7	6	5	4	3	2	1	0
NAME	DirChgFault	-	LowPow	-		ChgS	Stat[3:0]	
DirChgFault	Direct charging f 0 = Device in no 1 = V _{BAT} drops l	rmal operation		y is in supp	olement mode	e.		
LowPow	Low Power Mod 0 = Not In Low F 1 = In Low Power	ower Mode						
ChgStat[3:0]	Status of Charge 0000 = Charger 0001 = Charging 0010 = Pre-char 0011 = Fast-cha 0100 = Fast-cha 0101 = Maintain 0110 = Maintain 0111 = Charger i 1000 = Battery F	off Just suspended Just susp	ss current mod t voltage mod ogress n (see state o	e in progre le in progre liagram)	ss	m)		

Table 10. JEITAStatus Register (0x06)

ADDRESS:	0x06							
MODE:	Read On	nly						
BIT	7	6	5	4	3	2	1	0
NAME	-	-	-	ChgThrmRegCur	ChgThrmRegVlt	Ch	:0]	
ChgThrmRegCur	0 = Not c	FastCharge Current reduced due to JEITA status 0 = Not changed 1 = Reduced						
ChgThrmRegVIt	Battery F 0 = Not 0 1 = Redu	Changed	Voltage re	educed due to JEITA sta	atus			
ChgThrmStat[2:0]	000 = T < 001 = T1 010 = T2 011 = T3 100 = T > 101 = No thermistor 110 = NT	< T < T2 < T < T3 < T < T4 > T4 o thermistori TC input di	or detected ng, this mo sabled thro	(THM high due to exte ode may not function pr ough ThermEn. to CHGIN not present.	operly.	parallel res	istor is used	for

Table 11. BCStatus Register (0x07)

ADDRESS:	0x09							
MODE:	Read Only							
BIT	7	6	5	4	3	2	1	0
NAME	VBUSDet	ChgTypRun		PrChgTyp[2	0]	DCDTmo	ChgT	yp[1:0]
VBUSDet	Status of CHO 0 = VCHGIN < 1 = VCHGIN >							
ChgTypRun	Charger Dete 0 = Not Runn 1 = Running	ection Running S ing	tatus					
PrChgTyp[2:0]	Output of Pro 000 = Unknow 001 = Samsu 010 = Apple 0 011 = Apple 1 100 = Apple 2 101 = Apple 1 110 = 3A DCF 111 = RFU	ng 2A 0.5A IA 2A 12W	- Detection					
DCDTmo	continues as	required by BC1 out or detection r	.2, but SDP			ndicating D+/D- an	e open. BC1	.2 detection
ChgTyp[1:0]	00 = Nothing 01 = SDP, US 10 = CDP, Ch	arger Detection attached SB Cable attache narging Downstre edicated Charger	eam Port (cı		s on USB ope	erating speed)		

Table 12. Reserved Register (0x08)

ADDRESS:	0x08							
MODE:	Read Only							
BIT	7	6	5	4	3	2	1	0
NAME	-	-	-	-	-	-	-	-

Table 13. CCStatus1 Register (0x09)

ADDRESS:	0x09								
MODE:	Read Only								
BIT	7	6	5	4	3	2	1	0	
NAME	CCPins	Stat[1:0]	CC	SIStat	CCVcnStat		CCStat[2:0]		
CCPinStat[1:0]	Status of Act 00 = No Dete 01 = CC1 Ac 10 = CC2 Ac 11 = RFU	ermination tive							
CCIStat	CC Pin Dete 00 = Not in U 01 = 500mA 10 = 1.5A 11 = 3.0A		BUS Current	in UFP mode					
CCVcnStat	Status of VC 0 = VCONN 1 = VCONN	Disabled							
CCStat[2:0]	Output of CC 000 = No Co 001 = UFP 010 = DFP 011 = Audio of 100 = Debug 101 = Error 110 = Disable 111 = RFU	Accessory J Accessory	State Machin	ne					

Table 14. CCStatus2 Register (0x0A)

ADDRESS:	0x0A							
MODE:	Read Only							
BIT	7	6	5	4	3	2	1	0
NAME	-	-	-	-	VSAFE0V	DetAbrt	-	-
VSAFE0V	Status of VB 0 = V _{CHGIN} · 1 = V _{CHGIN} ·	< VSAFE0V	(Valid only in A	Attached.SRC_	_CCx, Attached	I.SNK_CCx sta	ite)	
DetAbrt	1 = Charger VBUS is valid	Detection runs Detection is at d for the debou	oorted by Type ince time. Chg	-C State Mach DetMan bit all	is valid for the nine. Charger do ows manual ru the in-progress	etection will rur n of charger de	n if ChgDetEn	

Table 15. DevInt1 Register (0x0B)

ADDRESS:	0x0B			,						
MODE:	Clear On Rea	d								
BIT	7	6	5	4	3	2	1	0		
NAME	SysFltI	ChglnOVPI	lLiml	VSysRegI	ThrmSd150I	ThrmSd120I	BatDetl	WbChgI		
SysFltI	0 = Status of S	SysFlt status change interrupt. 0 = Status of SysFlt has NOT changed since the last time SysFltl was read 1 = Status of SysFlt has changed since the last time SysFltl was read								
ChglnOVPI	0 = Status of 0	ChgInOVP status change interrupt. = Status of ChgInOVP has NOT changed since the last time ChgInOVPI was read = Status of ChgInOVP has changed since the last time ChgInOVPI was read								
ILimI	0 = Status of I	Lim status change interrupt. D = Status of ILim has NOT changed since the last time ILimI was read 1 = Status of ILim has changed since the last time ILimI was read								
VSysRegI	0 = Status of \		OT changed s		ne VSysRegI wa SysRegI was read					
ThrmSd150I	0 = Status of T		NOT change		time ThrmSd150 ThrmSd150I was					
ThrmSd120I	0 = Status of T		NOT change		time ThrmSd120 ThrmSd120I was					
BatDetI	0 = Status of E	BatDet status change interrupt. 0 = Status of BatDet has NOT changed since the last time BatDetI was read 1 = Status of BatDet has changed since the last time BatDetI was read								
WbChgI	0 = Status of V	change interru WbChg has NO WbChg has cha	T changed sir		e WbChgl was re Chgl was read	ad				

Table 16. AICLInt Register (0x0C)

ADDRESS:	0x0C										
MODE:	Clear On Re	Clear On Read									
BIT	7	6	5	4	3	2	1	0			
NAME	-	AICLI	-	-	-	-	-	-			
AICLI	0 = Status of		nterrupt. s NOT change s changed sinc								

Table 17. DevInt2 Register (0x0D)

ADDRESS:	0x0D										
MODE:	Clear On Re	ad									
BIT	7	6	5	4	3	2	1	0			
NAME	-	BattPREQI	_	BypUVLOI	SysUVLOI	DCDCILimI	DCDCRunAwayl	DCDCPGoodl			
BattPREQI	0 = Status of	BattPREQ status change interrupt. SattPREQ status of BattPREQ has NOT changed since the last time BattPREQI was read Status of BattPREQ has changed since the last time BattPREQI was read									
BypUVLOI	0 = Status of	BypUVLO status change interrupt. SypUVLO status change interrupt. SypUVLO status of BypUVLO has NOT changed since the last time BypUVLOI was read Status of BypUVLO has changed since the last time BypUVLOI was read									
SysUVLOI	0 = Status of	atus change int SysUVLO has SysUVLO has	NOT chang				ead				
DCDCILimI	0 = Status of	atus change in DCDCILim ha DCDCILim ha	s NOT chan				read				
DCDCRunAwayI	0 = Status of	DCDCRunAway status change interrupt. 0 = Status of DCDCRunAway has NOT changed since the last time DCDCRunAway was read 1 = Status of DCDCRunAway has changed since the last time DCDCRunAway was read									
DCDCPGoodl	0 = Status of	DCDCPGood status change interrupt. 0 = Status of DCDCPGood has NOT changed since the last time DCDCPGoodl was read 1 = Status of DCDCPGood has changed since the last time DCDCPGoodl was read									

Table 18. ChgInt Register (0x0E)

ADDRESS:	0x0E											
MODE:	Clear On Read											
BIT	7	6	5	4	3	2	1	0				
NAME	DirChgFaultl	DirChgFaultI LowPowRI LowPowFI ChgS										
DirChgFaultl	0 = Status of DirCho	DirChgFault status change interrupt. 0 = Status of DirChgFault has NOT changed since the last time DirChgFaultI was read 1 = Status of DirChgFault has changed since the last time DirChgFaultI was read										
LowPowRI	0 = LowPow bit rise	LowPow Rising Edge interrupt. 0 = LowPow bit rise edge has NOT occurred since the last time LowPowRI was read 1 = LowPow bit rise edge has occurred since the last time LowPowRI was read										
LowPowFI	LowPow Falling Edg 0 = LowPow bit fallin 1 = LowPow bit fallin	ng edge has NO										
ChgStatl	ChgStat[3:0] status 0 = Status of ChgSt 1 = Status of ChgSt	at[3:0] has NOT	changed since the		U							

Table 19. JEITAInt Register (0x0F)

ADDRESS:	0x0	0x0F											
MODE:	Clea	Clear On Read											
BIT	7	6 5 4 3 2 1 0											
NAME	-	ChgThrmRegCurl ChgThrmRegVltl ChgThrn											
ChgThrmRegCurl	0 = 3	ChgThrmRegCur status change interrupt. 0 = Status of ChgThrmRegCur has NOT changed since the last time ChgThrmRegCurl was read 1 = Status of ChgThrmRegCur has changed since the last time ChgThrmRegCurl was read											
ChgThrmRegVItI	0 = 8	Status of C	hgThrmRe	ange interrupt. gVlt has NOT changed s gVlt has changed since									
ChgThrmStatl	0 = 8	Status of C	hgThrmSta	change interrupt. at[2:0] has NOT changed at[2:0] has changed since	_								

Table 20. BCInt Register (0x10)

ADDRESS:	0x10								
MODE:	Clear On R	ead							
BIT	7	6	5	4	3	0			
NAME	VBUSDetI	-	-	ChgTypRunFl	ChgTypRunRI	PrChgTypl	DCDTmol	ChgTypl	
VBUSDetl	0 = Status o	BUSDet status change interrupt. = Status of VBUSDet has NOT changed since the last time VBUSDetI was read = Status of VBUSDet has changed since the last time VBUSDetI was read							
ChgTypRunFI	0 = ChgTyp	ChgTypRun Falling Edge interrupt. = ChgTypRun bit falling edge has NOT occurred since the last time ChgTypRunFl was read = ChgTypRun bit falling edge has occurred since the last time ChgTypRunFl was read							
ChgTypRunRl	0 71	Run bit ris	ing edge l	pt. nas NOT occurred nas occurred since		0 71			
PrChgTypl		f PrChgTy	p has NO	pt. T changed since thanged since than	_				
DCDTmol	0 = Status o	DCDTmo status change interrupt. 0 = Status of DCDTmo has NOT changed since the last time DCDTmol was read 1 = Status of DCDTmo has changed since the last time DCDTmol was read							
ChgTypl	ChgTyp status change interrupt. 0 = Status of ChgTyp has NOT changed since the last time ChgTypl was read 1 = Status of ChgTyp has changed since the last time ChgTypl was read								

Table 21. CCInt Register (0x11)

ADDRESS:	0x11									
MODE:	Clear On Rea	d								
BIT	7	6	5	4	3	2	1	0		
NAME	-	VSAFE0VI	DetAbrtl	-	CCPinStatl	CCIStatl	CCVcnStatl	CCStatl		
VSAFE0VI	0 = Status of \	VSAFE0V status change interrupt. 0 = Status of VSAFE0V has NOT changed since the last time VSAFE0VI was read 1 = Status of VSAFE0V has changed since the last time VSAFE0VI was read								
DetAbrtl	0 = Status of [T changed si		ne DetAbrtI was etAbrtI was read	read				
CCPinStatl	0 = Status of 0		NOT changed		t time CCPinStat CCPinStatI was					
CCIStatl	0 = Status of 0		OT changed si		me CCIStatI was CIStatI was read					
CCVcnStatl	0 = Status of 0	CCVcnStat status change interrupt. 0 = Status of CCVcnStat has NOT changed since the last time CCVcnStatl was read 1 = Status of CCVcnStat has changed since the last time CCVcnStatl was read								
CCStatl	0 = Status of 0	CCStat status change interrupt. 0 = Status of CCStat has NOT changed since the last time CCStatl was read 1 = Status of CCStat has changed since the last time CCStatl was read								

Table 22. DevInt1Mask Register (0x12)

ADDRESS:	0x12										
MODE:	Read/Write										
BIT	7	6	5	4	3	2	1	0			
NAME	SysFltIM	ChglnOVPIM	ILimIM	VSysRegIM	ThrmSd150IM	ThrmSd120IM	BatDetIM	WbChgIM			
SysFitIM	SysFltI Interru 1 = Mask 0 = Unmask										
ChglnOVPIM	ChglnOVPI In 1 = Mask 0 = Unmask										
ILimIM	ILiml Interrupt 1 = Mask 0 = Unmask										
VSysRegIM	VSysRegI Inte 1 = Mask 0 = Unmask	errupt Mask									
ThrmSd150IM	ThrmSd150I II 1 = Mask 0 = Unmask	nterrupt Mask									
ThrmSd120IM	ThrmSd120I II 1 = Mask 0 = Unmask	nterrupt Mask									
BatDetIM	BatDetl Interru 1 = Mask 0 = Unmask	upt Mask									
WbChgIM	WbChgl Interr 1 = Mask 0 = Unmask	upt Mask									

Table 23. AICLIntMask Register (0x13)

ADDRESS:	0x13										
MODE:	Read/Write	Read/Write									
BIT	7	6	5	4	3	2	1	0			
NAME	-	AICLIM	-	-	-	-	-	-			
AICLIM	AICLI Interru 1 = Mask 0 = Unmask	pt Mask									

Table 24. DevInt2Mask Register (0x14)

ADDRESS:	0x14	0x14											
MODE:	Read/V	Vrite											
BIT	7	6	5	4	3	2	1	0					
NAME	-	BattPREQIM	-	BypUVLOIM	SysUVLOIM	DCDCILimIM	DCDCRunAwayIM	DCDCPGoodIM					
BattPREQIM	1 = Ma	attPREQI Interrupt Mask = Mask = Unmask											
BypUVLOIM	1 = Ma	sypUVLOI Interrupt Mask = Mask = Unmask											
SysUVLOIM	SysUVI 1 = Mas 0 = Unr		1ask										
DCDCILimIM	DCDCI 1 = Mas 0 = Unr		Mask										
DCDCRunAwayIM	1 = Ma	DCDCRunAwayl Interrupt Mask 1 = Mask 0 = Unmask											
DCDCPGoodIM	DCDCF 1 = Mas 0 = Unr		pt Mask										

Table 25. ChgIntMask Register (0x15)

ADDRESS:	0x15	0x15											
MODE:	Read/Write												
BIT	7	7 6 5 4 3 2 1 0											
NAME	DirChgFaultIM	LowPowRIM	LowPowFIM	-	-	-	-	ChgStatIM					
DirChgFaultIM	DirChgFaultl Intel 1 = Mask 0 = Unmask												
LowPowRIM	LowPowRI Interru 1 = Mask 0 = Unmask												
LowPowFIM	LowPowFl Interru 1 = Mask 0 = Unmask	pt Mask											
ChgStatIM	ChgStatl Interrup 1 = Mask 0 = Unmask	t Mask											

Table 26. JEITAIntMask Register (0x16)

ADDRESS:	0x16	0x16										
MODE:	Read/Wr	Read/Write										
BIT	7	7 6 5 4 3 2 1 0										
NAME	-	ChgThrmRegCurIM ChgThrmRegVltIM ChgThrmStatIM										
ChgThrmRegCurlM	1 = Mask	ChgThrmRegCurl Interrupt Mask 1 = Mask 0 = Unmask										
ChgThrmRegVltIM	ChgTHrm 1 = Mask 0 = Unma		terrupt	Mask								
ChgThrmIM	ChgThrm 1 = Mask 0 = Unma	-	t Mask									

Table 27. BCIntMask Register (0x17)

ADDRESS:	0x17									
MODE:	Read/Write									
BIT	7	6	5	4	3	2	1	0		
NAME	VBUSDetIM	-	-	ChgTypRunFIM	ChgTypRunRIM	PrChgTypIM	DCDTmolM	ChgTypIM		
VBUSDetIM	VBUSDetl Inter 1 = Mask 0 = Unmask									
ChgTypRunFIM	ChgTypRunFI I 1 = Mask 0 = Unmask									
ChgTypRunRIM	ChgTypRunRI I 1 = Mask 0 = Unmask	nterrup	t Mask							
PrChgTypIM	PrChgTypel Into 1 = Mask 0 = Unmask	errupt N	1ask							
DCDTmoIM	DCDTmrl Interr 1 = Mask 0 = Unmask	upt Ma	sk							
ChgTypIM	ChgTypI Interru 1 = Mask 0 = Unmask	pt Masl	<							

Table 28. CCIntMask Register (0x18)

ADDRESS:	0x18									
MODE:	Read/Wr	ite								
BIT	7	6	5	4	3	2	1	0		
NAME	-	VSAFE0VIM	DetAbrtIM	-	CCPinStatIM	CCIStatIM	CCVcnStatIM	CCStatIM		
VSAFE0VIM	1 = Mask	VSAFE0VI Interrupt Mask 1 = Mask 0 = Unmask								
DetAbrtIM	DetAbrtl 1 = Mask 0 = Unma									
CCPinStatIM	CCPinSta 1 = Mask 0 = Unma									
CCIStatIM	CCIStatl 1 = Mask 0 = Unma									
CCVcnStatIM	CCVcnSt 1 = Mask 0 = Unma									
CCStatIM	CCStatl I 1 = Mask 0 = Unma									

Table 29. LED_CTRL Register (0x19)

ADDRESS:	0x19	0x19									
MODE:	Read/Write										
BIT	7	6	5	4	3	2	1	0			
NAME	-	-	-	-	-	-	LEDCtrl	LEDManual			
LEDCtrl	0 = LED is O	LED Manual Control 0 = LED is OFF 1 = LED is ON									
LEDManual	0 = LED is co		ation narger state ma controlled by								

Table 30. ThermaCfg1 Register (0x1A)

ADDRESS:	0x1A							
MODE:	Read/Write							
BIT	7	6	5	4	3	2	1	0
NAME		T1T2IFchg[2:0)]		T2T3IFchg[2:0)]	JeitaC	fgR[1:0]
T1T2lFchg[2:0]	Fast Charge 000 = 0.2 x I 001 = 0.3 x I 010 = 0.4 x I 011 = 0.5 x II 100 = 0.6 x I 101 = 0.7 x I 110 = 0.8 x II 111 = 1.0 x II	FChg FChg FChg FChg FChg FChg FChg	-T2 temperatu	re zone				
T2T3lFchg[2:0]	Fast Charge 000 = 0.2 x I 001 = 0.3 x I 010 = 0.4 x I 011 = 0.5 x II 100 = 0.6 x I 101 = 0.7 x I 110 = 0.8 x II 111 = 1.0 x II	FChg FChg FChg FChg FChg FChg FChg	2-T3 temperatu	re zone				
JeitaCfgR[1:0]	01 = JEITA N 10 = JEITA N	Nonitoring and Nonitoring and Nonitoring and	TPU SW disal TPU SW Enal TPU SW Enal bled and TPU	oled if V _{CHGIN} oled	N > V _{BDET} (10m	ns Debounce)		

Table 31. ThermaCfg2 Register (0x1B)

ADDRESS:	0x1B						,	,
MODE:	Read/Write							
BIT	7	6	5	4	3	2	1	0
NAME	-	T3T4IFchg[2:0]	-	T3T4ENset	T1T2ENset	T3T4VFset	T1T2VFset
T3T4IFchg[2:0]	Fast Charge 000 = 0.2 x II 001 = 0.3 x II 010 = 0.4 x II 011 = 0.5 x IF 100 = 0.6 x II 101 = 0.7 x II 110 = 0.8 x IF 111 = 1.0 x IF	FChg FChg =Chg FChg FChg =Chg	-T4 temperatu	ure zone				
T3T4ENset	0 = JEITA tur	er On/Off in T3 ns charger off esn't turn char	in T3-T4 zone		ACtrSet = 1)			
T1T2ENset	0 = JEITA tur	er On/Off in T1 ns charger off esn't turn char	in T1-T2 zone		ACtrSet = 1)			
T3T4VFset	JEITA voltage 1 = Enabled 0 = Disabled	e scaling enab	le in T3-T4. (0	Only valid if JEI	TACtrSet = 1)			
T1T2VFset	JEITA voltage 1 = Enabled 0 = Disabled	e scaling enab	led in T1-T2.	(Only valid if JE	EITACtrSet = 1)			

Table 32. ThermaCfg3 Register (0x1C)

ADDRESS:	0x1C	0x1C										
MODE:	Read/Write Unless Otherwise Noted											
BIT	7	7 6 5 4 3 2 1 0										
NAME	-	-	-	-	-	-	JEITACtrSet	WarmCoolSel				
JEITACtrSet	0 = JEITA sta	JEITA Control Enable 0 = JEITA status Not affect charger 1 = JEITA status affects charger settings (See register ThermaCfg2)										
WarmCoolSel	0 = 45°C Wa	EITA Zone The rm, 10°C Cool rm, 10°C Cool		t (Read Only)								

Table 33. ChargerCtrl1 Register (0x1D)

ADDRESS:	0x1D								
MODE:	Read/Write or	Read-Only	if AppWrtP	rtct = "(1) Protec	ted" (See Table	e 61)			
BIT	7	6	5	4	3	2	1	0	
NAME	ChgAutoStp	BatRe0	Chg[1:0]	FreshBatDis (MAX14748B)	-	BatR	BatReg[1:0] Ch		
ChgAutoStp	Charger Auto-Stop. Controls the transition from maintain charge to maintain charge done. See <i>Battery Charger State</i> diagram. 0 = Auto-Stop disabled. 1 = Auto-Stop enabled.								
BatReChg[1:0]	BAT Recharge 00 = 200mV 01 = 300mV 10 = 400mV 11 = 500mV	Threshold.	If ChgAutoSi	ta = 1, charger re	starts charging i	f V _{BAT} falls below	v V _{BATREG} by	this amount.	
FreshBatDis (MAX14748B)	Enable/Disable 0 = Fresh Batte 1 = Fresh Batte Note, this bit sl	ery Feature l ery Feature l	Enabled Disabled						
BatReg[1:0]	Battery Regula 00 = 8.3V 01 = 8.4V 10 = 8.5V 11 = 8.6V	ition Thresho	old						
ChgEn	On/Off Control 0 = Charger dis 1 = Charger er	sabled	(does not in	npact SYS node).					

Table 34. ChargerCtrl2 Register (0x1E)

ADDRESS:	0x1E							
MODE:	Read/Write of	or Read-Only	if AppWrtPrtct	= "(1) Prote	cted" (See Tal	ole 61)		
BIT	7	6	5	4	3	2	1	0
NAME	-		VPchg[2:0]		IPCh	g[1:0]	ChgDo	ne[1:0]
VPchg[2:0]	Pre-charge V 000 = 5.7V 001 = 5.8V 010 = 5.9V 111 = 6.0V 100 = 6.1V 101 = 6.2V 110 = 6.3V 111 = 6.4V	oltage Thresi	nold Setting					
IPChg[1:0]	Pre-charge C 00 = 0.05 x IF 01 = 0.1 x IFC 10 = 0.2 x IFC 11 = 0.3 x IFC	FChg Chg Chg	9					
ChgDone[1:0]	Charge Done 00 = 0.05 x IF 01 = 0.1 x IF 10 = 0.2 x IF 11 = Reserve	FChg Chg Chg	etting					

Table 35. ChargerCtrl3 Register (0x1F)

ADDRESS:	0x1F										
MODE:	Read/Wr	rite or Read-Only	if AppWrtPrto	t = "(1) Protec	ted" (See Tal	ble 61)					
BIT	7	6	5	4	3	2	1	0			
NAME	-	ChgAutoSta	MtChg ⁻	Γmr[1:0]	FChgT	mr[1:0]	PChgT	mr[1:0]			
ChgAutoSta	0 = Char	Charger Auto-Restart Control Charger remains in maintain charge done even when VBAT is less than BAT recharge threshold. Charger automatically restarts when VBAT drops below BAT recharge threshold.									
MtChgTmr[1:0]	00 = 0mi 01 = 15m 10 = 30m	Maintain Charge Timer Setting 00 = 0min 01 = 15min 10 = 30min 11 = 60min									
FChgTmr[1:0]	Fast- Cha 00 = 75m 01 = 150 10 = 300 11 = 600	min min									
PChgTmr[1:0]	Pre-char 00 = 30m 01 = 60m 10 = 120 11 = 240	nin min									

Table 36. ChargerCtrl4 Register (0x20)

ADDRESS:	0x20	0x20										
MODE:	Read-Onl	у				Read/Write or Read-Only if AppWrtPrtct "(1) Protected" (See Table 61)						
BIT	7	6	5	4	3	2	1	0				
NAME	WeakBatStat[2:0] WeakBatEn -						-					
WeakBatStat[2:0]	000 = Idle 001 = Batt 010 = Wea 011 = Goo	od Battery. ak Battery 2	not SDP									
WeakBatEna	Weak Batt 0 = Disabl 1 = Enable		nable									

Table 37. CurLimCtrl Register (0x21)

ADDRESS:	0x21										
MODE:	Read/Write										
BIT	7	6	5	4	3	2	1	0			
NAME	CurLim1Frc	FSUSMsk	-		(CurLim1Set[4:0	0]				
CurLim1Frc		Forced Input Current Limit Enable. When CurLim1Frc is 1, the input current limit is by the CurLim1Set[4:0]. 0 = Not forced 1 = Forced									
FSUSMsk	0 = FSUS pin	FSUS pin function mask. If FSUSMsk is 1, FSUS pin status is ignored. 0 = FSUS pin function enabled 1 = FSUS pin function disabled									
CurLim1Set[4:0]	Forced Input (00000 = 0.104 00001 = 0.204 11101 = 3.004 11110 = Reser 11111 = Reser	A A ved	/alue. The in	put current lim	it is forced to t	this value if Cu	rLim1Frc is se	t to 1.			

Table 38. CurLimStatus Register (0x22)

ADDRESS:	0x22									
MODE:	Read Only									
BIT	7	6	5	4	3	2	1	0		
NAME	C	CurLim2Rb[2:0] SpvChgllim[4:0]								
CurLim2Rb[2:0]	Active Char 0 = 20% 1 = 30% 2 = 40% 3 = 50% 4 = 60% 5 = 70% 6 = 80% 7 = 100%	rger/Boost cu	rrent as perce	ent of the valu	e set by R _{SET} .					
SpvChgllim[4:0]	SpvChgllim 00000 = 0.1 00001 = 0.2 11101 = 3.0 11110 = Res	10A 20A 00A served	ne actual inpi	ut current limit	currently set.					

Table 39. BBCFG1 Register (0x23)

ADDRESS:	0x23	0x23 Read/Write or Read-Only if AppWrtPrtct = "(1) Protected" (See Table 61) 7 6 5 4 3 2 1 0										
MODE:	Read/Write											
BIT	7											
NAME		BoostRC	omp[3:0]	-	-	-	-					
BoostRComp[3:0]	Sets the inte 0000 = 9.5ks 0001 = 17.3k 0010 = 25.3k 0011 = 33.2k 0100 = 41.4k 0101 = 49.2k 0110 = 57.3k 0111 = 65.1k 1000 = 73.6k 1001 = 81.4k 1010 = 89.4k 1011 = 97.2k 1100 = 105.5 1101 = 113.3 1110 = 121.4 1111 = 129.2	CACACACACACACACACACACACACACACACACACACA	sation resistor	for the boos	t mode							

Table 40. BBCFG2 Register (0x24)

ADDRESS:	0x24									
MODE:	Read/Write	or Read-Only	if AppWrtPr	rtct = "(1) Protec	ted" (See Tal	ole 61)				
BIT	7	6	5	4	3	2	1	0		
NAME	-	-	-	BBFrcZX	BuckVSet[3:0]					
BBFrcZX	BBFrcZX set 0 = Forced P 1 = Forced Z		forced ZX mo	ode.						
BuckVSet[3:0]	Buck Regula 0000 = 4.0V 0001 = 4.1V 0010 = 4.2V 0011 = 4.3V 0100 = 4.4V 0101 = 4.5V 0110 = 4.6V 0111 = 4.7V 1000 = 4.8V 1001 = 4.9V 1010 = 5.0V 1011 = 5.1V 1100 = 5.2V 1110 = 5.4V 1111 = 5.5V									

Table 41. BCCtrl1 Register (0x25)

ADDRESS:	0x25					,					
MODE:	Read/Write										
BIT	7	6	5	4	3	2	1	0			
NAME	DCD2s	SfOutLvI	-	ADC3PDet SfOutCtrl[1:0] ChgDetMan ChgE							
DCD2s	DCD2s sets to 0 = standard 1 = 2s	the timing of D	CD in BC1.2								
SfOutLvI	SFOUT Volta 0 = 5V 1 = 3.3V	ige Level Sele	ct								
ADC3PDet	3A DCP Dete 0 = Not Enab 1 = Enabled		adds detectio	n step after BC1	1.2 completes	s to detect pro	esence of 3A DCI	?)			
SfOutCtrl[1:0]	00 = Always 01 = On if a v 10 = Turns on a. ChgD b. ChgD 11: RFU Note: CHGIN SRC_CCx m According to	valid CHGIN von under followin etEn = 1, CHO etEn = 0, and N valid can be ode. A system	oltage is presong conditions. GIN is valid, a CHGIN is vale external CHG that supports ification, CHG	nd BC1.2 FSM [id ilN voltage or Ch power swap mu GIN will collapse	HGIN voltage ust not use S	e generated b	y reverse buck in o supply USB trai urns off SFOUT I	nsceiver.			
ChgDetMan	0 = Not enab		· ·	er detection. (Bit	auto-resets t	to 0)					
ChgDetEn	Charger Dete 0 = Not enab 1 = Enabled	led	tion runs eve	ry time V _{CHGIN}	> V _{BDET} and	d DetAbrt = 0))				

Table 42. Reserved Register (0x26)

ADDRESS:	0x26							
MODE:	Read Only							
BIT	7	6	5	4	3	2	1	0
NAME	-	-	-	-	-	-	-	-

Table 43. CCCtrl1 Register (0x27)

ADDRESS:	0x27							
MODE:	Read/Write							
BIT	7	6	5	4	3	2	1	0
NAME	-	-	-	CCSrcSnk	CCSnkSrc	CCDbgEn	CCAudEn	CCDetEn
CCSrcSnk	Allow State ma mode. 0 = Disable 1 = Enable	chine to ente	er Sink Mode (DFP) detectior	n. Note USB P	D role swap is	allowed to ent	ter Source
CCSnkSrc	Allow State ma mode. 0 = Disable 1 = Enabled	chine to ente	er Source Mod	le (DFP) detect	tion. Note USE	3 PD role swap	o is allowed to	enter Source
CCDbgEn	Enable Detection 0 = Disabled 1 = Enabled	on of Type-C	Debug Adapt	er				
CCAudEn	Enable Detection 0 = Disabled 1 = Enabled	on of Type-C	Audio Adapte	r				
CCDetEn	Enable CC Pin 0 = Disabled 1 = Enabled	Detection –	Force State M	lachine to Disa	bled State.			

Table 44. CCCtrl2 Register (0x28)

ADDRESS:	0x28							
MODE:	Read/Write							
BIT	7	6	5	4	3	2	1	0
NAME	CCForceError	SnkAttachedLock	CCSnkSrcSwp	CCSrcSnkSwp	CCVcnSwp	CCVcnEn	CCSrcRst	CCSnkRst
CCForceError	0 = No action	after a write (This		utomatically whe	en action is do	one)		
SnkAttachedLock	0 = Exit Attach	after a minimum c ed.SNK* state wh Attached.SNK* sta	en V _{CHGIN} < V _E					
CCSnkSrcSwp		•		This bit must be	written to 0 o	nce the US	3 PD contro	ller
CCSrcSnkSwp		•		This bit must be	written to 0 o	nce the US	3 PD contro	ller
CCVcnSwp	automatically v	lachine to Swap V when action is dor in V _{CONN} role ge in V _{CONN}		resets to 0 after	a write (Note	this bit will	reset to 0	
CCVcnEn		V _{CONN} _{ONN} off (both exter operation based c			switch)			
CCSrcRst	Force a reset of 0 = No reset 1 = Request re	of the State Machir	ne – Immediate ti	ransition to Unatt	ached.SRC*	state. Bit res	ets to 0 afte	r a write.
CCSnkRst	Force a reset of 0 = No reset 1 = Request re	of the State Machir	ne – Immediate ti	ransition to Unatt	ached.SNK* s	state. Bit res	ets to 0 afte	r a write.

^{*} Attached.SNK, Unattached.SRC, and Unattached.SNK are defined in USB Type-C Specificaiton Release 1.1.

Table 45. CCCtrl3 Register (0x29)

ADDRESS:	0x29									
MODE:	Read/Wi	rite								
BIT	7	6	5	4	3	2	1	0		
NAME	-	-	-	-	CCTrySnk	CCPreferSnk	CCDRPF	Phase[1:0]		
CCTrySnk	that stror 0 = Disal	Enable transition from AttachWait.SRC* to Try.SNK* then to Attach.SNK_CCx* or to TryWait.SRC* for DRP that strongly prefers the SNK role. CCTrySnk has higher priority than CCPreferSnk. 0 = Disabled 1 = Enabled								
CCPreferSnk	Enable to the SNK 0 = Disal 1 = Enab	role. oled	Jnattached.SF	RC* to Try.S	NK* then to Un	attached.SNK* fo	or DRP that str	ongly prefers		
CCDRPPhase[1:0]	Percent 6 00 = 35% 01 = 40% 10 = 45% 11 = 50%	6 6	is acting as Ur	nattached.S	RC* when CCS	NKSRC = 1				

^{*} AttachWait.SRC, Try.SNK, Attached.SNK, TryWait.SRC, Unattached.SNK, and Unattached SRC are defined in USB Type-C Specificaiton Release 1.1.

Table 46. CHGINILim1 Register (0x2A)

ADDRESS:	0x2A								
MODE:	Read Only								
BIT	7	6	5	4	3	2	1	0	
NAME	- CHGINILim[6:0]								
CHGINILim[6:0]	Status of cha all 100mA. 0000000 = 1 0000001 = 1 0000010 = 1 0000010 = 1 0000011 = 1 1111111 = 40	00mA 00mA 00mA 00mA 33mA 66mA	urrent limit se	et by charger o	detection (in 33	mA step). Note	e that the first 4	4 codes are	

Table 47. CHGINILim2 Register (0x2B)

ADDRESS:	0x2B							
MODE:	Read/Writ	e						
BIT	7	6	5	4	3	2	1	0
NAME	CHGINILimGate SDPMaxCur[1:0]					(Cur[1:0]	CDPMaxCur	
CHGINILimGate	0 = No gat	n Control o ing of CHG hanges in 0	INILim set		SC1.2 FSM C1.2 FSM completes -	- ChgTypRur	n = 0	
SDPMaxCur[1:0]	indicating 00 = No m 01 = Limit 10 = Limit	1.5A or 3A. odification of SDP to 500 SDP to 1.0.	Requires of CHGIN mA. Chg A. ChgTyp	CHGINIL _LIM Typ = 01 o = 01 (SI	I. USB-C to USB-A ca LimGate = 1. (SDP) and PrChgTyp DP) and PrChgTyp = 0 DP) and PrChgTyp = 0	= 000 (unknow	own) set CHG n) set CHGIN	GINILim[6:0] to 0x0F IILim[6:0] to 0x1E
CDPMaxCur	3A. Requir 0 = No mo	es CHGIN_ dification of	_LIM_Gate f CHGIN_I	e = 1. LIM	USB-C to USB-A ca	•		

Table 48. AICLCFG1 Register (0x2C)

ADDRESS:	0x2C											
MODE:	Read/Write or Re	ead-Only if	AppWrtPrtct	= "(1) Protect	ted" (See Tabl	e 61)						
BIT	7	6	5	4	3	2	1	0				
NAME	AICLEn	AICLEn - - - - - AICLAbort										
AICLEn	AICL Enable. Writing 1 to AICLEn enables AICL operation. Note that if AICLAbort is 1, AICL operation is not allowed. This bit auto-resets to 0. 0 = No Action 1 = AICL enabled											
AICLAbort	High Priority AICL 0 = Device is allo 1 = Device is NO	wed to run	,	-		aborted if it's a	already runni	ng.				

Table 49. AICLCFG2 Register (0x2D)

ADDRESS:	0x2D								
MODE:	Read/Write	or Read-Only	if AppWrtPrtc	t = "(1) Prote	cted" (See Tal	ble 61)			
BIT	7	6	5	4	3	2	1	0	
NAME	ı	BYPUVLO[2:0]				AICLMaxI[4:0]			
BYPUVLO[2:0]	VBUS Thesh 000 = 3.8V 001 = 3.9V 010 = 4.0V 011 = 4.1V 100 = 4.2V 101 = 4.3V 110 = 4.4V 111 = 4.5V	001 = 3.9V 010 = 4.0V 011 = 4.1V 100 = 4.2V 101 = 4.3V 110 = 4.4V							
AICLMaxI[4:0]	AICL Stop Ct 00000 = 1000 00001 = 2000 11111 = 3.2A	mA	A step)						

Table 50. AICLCFG3 Register (0x2E)

ADDRESS:	0x2E											
MODE:	Read/Write	or Read-Only	if AppWrtPrt	ct = "(1) Protect	ted" (See Ta	ble 61)						
BIT	7	6	5	4	3	2	1	0				
NAME	-	BYPDeb AICLTBlk[1:0] AICLTStep[1:0]										
BYPDeb	AICL BYPU 0 = 500μs 1 = 200μs	= 200µs										
AICLTBIk[1:0]	TBLANK Tir 00 = 500ms 01 = 1s 10 = 1.5s 11 = 5s	Ū										
AICLTStep[1:0]	TSTEP Time 00 = 100ms 01 = 200ms 10 = 300ms 11 = 500ms											

Table 51. DPDNSw Register (0x2F)

ADDRESS:	0x2F									
MODE:	Read/Write									
BIT	7	6	5	4	3	2	1	0		
NAME	-	-	-	-	-	-	AnSw(Ontl[1:0]		
AnSwCntl[1:0]	00 = Auto. 9 01 = Auto ir 10 = Switch		during adapte and Buck mod	er detection. Sv de is detected.		SDP or CDP is	detected.			

Table 52. Others Register (0x30)

ADDRESS:	0x30	0x30							
MODE:	Read/Write	Read/Write							
BIT	7	6	5	4	3	2	1	0	
NAME	-	-	-	-	-	-	-	USBCRSet	
USBCRSet	this operation	on opens the in Table 59 and T on	put limiter and	turns off the bo	registers assoc oost converter bit auto-resets	temporarily.) Re		`	

Table 53. Reserved Register (0x31)

ADDRESS:	0x31							
MODE:	Read Only							
BIT	7	6	5	4	3	2	1	0
NAME	-	-	-	-	-	-	-	-

Table 54. Reserved Register (0x32)

ADDRESS:	0x32							
MODE:	Read Only							
BIT	7	6	5	4	3	2	1	0
NAME	-	-	-	-	-	-	-	-

Table 55. LowPow Register (0x33)

ADDRESS:	0x33	0x33								
MODE:	Read/Write	Read/Write								
BIT	7	6	5	4	3	2	1	0		
NAME	LowPowEn	-	-	-	-	-	-	LowPowAbort		
LowPowEn		is not allowed	d. This bit auto		ow Power mod	de. Note that	if LowPo	owAbort is 1, Low		
LowPowAbort		allowed to er	nter Low Powe	r mode by writir Power Mode. Lo	•		ed if dev	ice has already		

Table 56. Reserved Register (0x34)

ADDRESS:	0x34							
MODE:	Read Only	/						
BIT	7	6	5	4	3	2	1	0
NAME	-	-	-	-	-	-	-	-

Table 57. FLTSel Register (0x35)

ADDRESS:	0x35	0x35							
MODE:	Read/Writ	Read/Write							
BIT	7	7 6 5 4 3 2 1 0							
NAME	FLTS	elect[1:0]	-	-	-	-	-	-	
FLTSelect[10]	00 = No ef 01 = Low o (ChgStat[3 1x = Fallin	arger-Faulting an fect and interna on FLTIN pin (60 t:0] = 1000). g edge on FLTII or more details.	lly ignored)μs debounce) _) places the ch	arger in Batter	-			

Applications Information

Component Selection

The correct selection of external components ensures high efficiency, low output ripple, and fast transient response.

Inductor Selection

The MAX14748 is designed to use a 1.5 μ H or 2.2 μ H inductor. See <u>Table 58</u> for suggested inductors and manufacturers.

BAT Capacitor Selection

BAT capacitor is required to keep the BAT voltage ripple small and to ensure regulation loop stability. The BAT capacitor must have low impedance at the switching frequency. Ceramic capacitors with X5R or X7R dielectric are highly recommended due to their small size, low ESR, and small temperature coefficients.

BAT requires careful bypassing. In the PCB layout, place BAT capacitor as close as possible to BAT to minimize parasitic inductance. If making connections to BAT capacitor through vias, ensure that the vias are rated for the expected input current to avoid excess inductance and resistance between the capacitor and BAT.

The recommended nominal BAT capacitance is $22\mu F$, however, after initial tolerance, bias voltage, aging, and temperature derating, the effective capacitance must be greater than $10\mu F$. To ensure regulation loop stability, the effective BAT capacitance should be chosen within the range of $10\mu F$ to $30\mu F$.

SYS Capacitor Selection

SYS capacitor acts as the output capacitor for the boost converter when charging, and the input capacitor for the reverse buck converter when the device is acting as power source in DRP mode. SYS capacitor is required to keep the SYS voltage ripple small and to ensure regulation loop stability. It must have low impedance at the switching frequency. Ceramic capacitors with X5R or X7R dielectric are highly recommended due to their small size, low ESR, and small temperature coefficients.

Place SYS capacitor as close as possible to SYS to minimize parasitic inductance. If making connections to SYS capacitor through vias, ensure that the vias are rated for the expected input current to avoid excess inductance and resistance between the capacitor and SYS.

The recommended nominal SYS capacitance is $40\mu F$, however, after initial tolerance, bias voltage, aging, and temperature derating, the effective capacitance must be greater than $15\mu F$.

BYP Capacitor Selection

BYP capacitor acts as the input capacitor for the boost converter, and the output capacitor for the reverse buck converter. BYP capacitor reduces the current peaks drawn from the input power source when charging while reducing the output voltage ripple of the reverse buck converter when it is acting as power source in DRP mode. The impedance of the input capacitor at the switching frequency should be very low. Ceramic capacitors with X5R or X7R dielectric are highly recommended due to their small size, low ESR, and small temperature coefficients.

Table 58. Suggested Inductors

APPLICATION	INDUCTANCE (µH)	R _{DC} (MΩ)	SATURATION CURRENT (A)	CURRENT RATING (A)	SUGGESTED PARTS
3A Type-C	2.2µH	26	4.2	3.7	Taiyo Yuden NRS6028T2R2NMGJ
Adapters	2.2µH	80	3.5	2.8	BOURNS SRP4012TA-2R2M

Table 59. Reset Types

RESET TYPE	RESET CONDITION
RST	1. V _{CCINT} Power-On Reset
RST1	1. V _{CCINT} Power-On Reset or 2. FLTIN falling edge (only if FLTSelect[1] = 1)
RST2	1. V _{CCINT} Power-On Reset or 2. FLTIN falling edge (only if FLTSelect[1] = 1)
RST3	V _{CCINT} Power-On Reset or FLTIN falling edge (only if FLTSelect[1] = 1) or USB-C reset through USBCRSet (0x30[0])

BYP requires careful bypassing. In the PCB layout, place BYP capacitor as close as possible to the BYP to minimize parasitic inductance. If making connections to BYP capacitor through vias, ensure that the vias are rated for the expected input current to avoid excess inductance and resistance between the capacitor and BYP.

The recommended nominal BYP capacitance is $22\mu F$, however, after initial tolerance, bias voltage, aging, and temperature derating, the effective capacitance must be greater than $10\mu F$.

CHGIN Capacitor Selection

CHGIN capacitor decouples a charge source and its parasitic impedance. Typically, the charger source at CHGIN is a USB connector's VBUS. The recommended nominal CHGIN capacitance is $1\mu F$. Larger capacitance at CHGIN improves the decoupling; however, take care not to exceed the maximum capacitance allowed by the USB specification.

The impedance of the CHGIN at the DC-DC switching frequency should be very low. Ceramic capacitors with X5R or X7R dielectric are highly recommended due to their small size, low ESR, and small temperature coefficients.

To fully utilize the +30V input capability of the, choose a capacitor with a 35V or greater rating; many applications don't need to utilize the full input capability of the device and find that a 16V or 10V rated input capacitor is sufficient.

BST Capacitor Selection

Choose the nominal BST capacitance to be $0.1\mu F$. BST capacitor is part of a charge pump that creates the high-side gate drive for the DC-DC. It is recommended that the BST capacitor has at least 10V rating.

PCB Layout and Routing

High switching frequencies and large peak currents make PCB layout a very important part of design. Good design minimizes excessive EMI on the feedback paths and voltage gradients in the ground plane, both of which can result in instability or regulation errors. Connect the inductor, input capacitors, and output capacitors as close together as possible, and keep their traces short, direct, and wide. Keep noisy traces, such as the LX node, as short as possible.

Table 60. Register Reset Types and Default Values

REGISTER ADDRESS	REGISTER NAME	RESET TYPE	MAX14748
0x00	ChipID	RST1	0x3E
0x01	ChipRev	RST1	0x33
0x01 (MAX14748B)	ChipRev	RST1	0x44
0x02	DevStatus1	RST1	STATUS*
0x03	AICLStatus	RST1	STATUS
0x04	DevStatus2	RST1	STATUS
0x05	ChgStatus	RST1	STATUS
0x06	JEITAStatus	RST1	STATUS
0x07	BCStatus	RST3	STATUS
80x0	Reserved	_	0x00
0x09	CCStatus1	RST3	STATUS
0x0A	CCStatus2	RST3	STATUS
0x0B	DevInt1	RST1	INT*
0x0C	AICLInt	RST1	INT
0x0D	DevInt2	RST1	INT
0x0E	ChgInt	RST1	INT
0x0F	JEITAInt	RST1	INT
0x10	BCInt	RST3	INT
0x11	CCInt	RST3	INT
0x12	DevInt1Mask	RST1	0xFF
0x13	AICLIntMask	RST1	0x40
0x14	DevInt2Mask	RST1	0x7F
0x15	ChgIntMask	RST1	0xF1
0x16	JEITAIntMask	RST1	0x19
0x17	BCIntMask	RST3	0xFF
0x18	CCIntMask	RST3	0x7F
0x19	LED CTRL	RST1	0x00
0x1A	ThermaCfq1	RST2	0x7D
0x1B	ThermaCfg2	RST2	0xEF

REGISTER ADDRESS	REGISTER NAME	RESET TYPE	MAX14748
0x1C	ThermaCfg3	RST2	0x02
0x1D	ChargerCtrl1	RST2	0x80
0x1E	ChargerCtrl2	RST2	0x10
0x1F	ChargerCtrl3	RST2	0x49
0x20	ChargerCtrl4**	RST2	0x06
0x21	CurLimCtrl	RST2	0x00
0x22	CurLimStatus	RST1	STATUS
0x23	BBCFG1	RST1	0x20
0x24	BBCFG2	RST1	0x8A
0x25	BCCtrl1	RST3	0x05
0x26	Reserved	_	0x00
0x27	CCCtrl1	RST3	0x19
0x27 (MAX14748B)	CCCtrl1	RST3	0x11
0x28	CCCtrl2	RST3	0x04
0x29	CCCtrl3	RST3	0x08
0x2A	CHGINILim1	RST3	STATUS
0x2B	CHGINILim2	RST3	0x0B
0x2C	AICLCFG1	RST1	0x01
0x2D	AICLCFG2	RST1	0x44
0x2E	AICLCFG3	RST1	0x05
0x2F	DPDNSw	RST2	0x01
0x30	Others	RST1	0x00
0x31	Reserved	_	0x00
0x32	Reserved	_	0x00
0x33	LowPow	RST1	0x01
0x34	Reserved	_	0x01
0x35	FLTSel	RST	0x80

^{*}INT and STATUS: status and interrupt register values vary based on device operating condition.

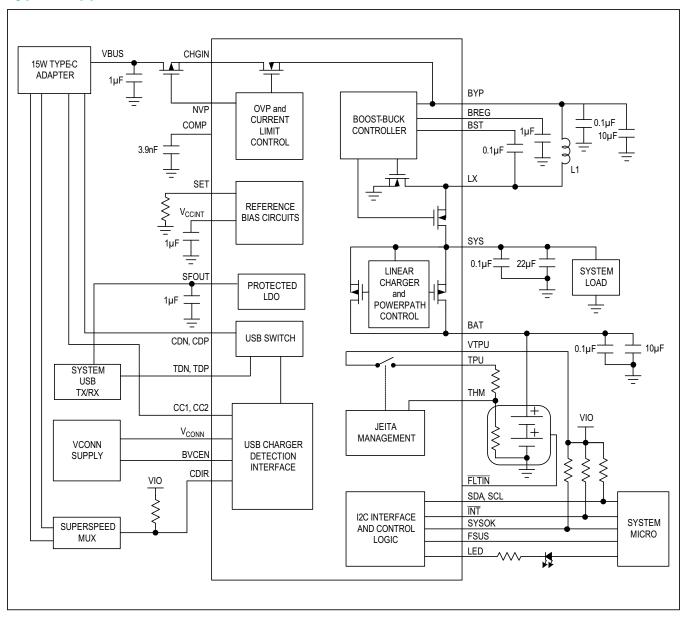
^{**} ChargerCtrl4 register value depends on the status of WeakBatStat[2:0] bits.

Table 61. Register Bit Default Values

REGISTER BITS	VALUES			
CDPMaxCur	1500mA			
SDPMaxCur[1:0]	500mA			
CHGINILimGate	Gating			
CCAudEn	Disabled			
CCDbgEn	Disabled			
CCSnkSrc	Disabled			
CCSrcSnk	Enabled			
JeitaCfgR[1:0]	"01"			
CCDRPPhase[1]	35% or 40%			
CCTrySnk	Enabled			
SfOutCtrl[1:0]	"01"			
ADC3PDet	Disabled			
DCD2s	Standard			
WarmCoolSel	45°C/10°C			
T1T2IFchg[2:0]	0.5 x IFChg			
T3T4IFchg[2:0]	1.0 x IFChg			
BatReg[1:0]	8.3V			
ChgEn	Disabled			
JETIACtrSet	(1) Control			
IPChg[1:0]	0.05 x IFChg			
ChgDone[1:0]	0.05 x IFChg			
ChgAutoStp	Enabled			
BatReChg[1:0]	200mV			

REGISTER BITS	VALUES		
FreshBatDis	Done		
ChgAutoSta	Enabled		
MtChgTmr[1:0]	0min		
FChgTmr[1:0]	300min		
PChgTmr[1:0]	60min		
ChipRevH[3:0]	3		
AppWrtPrtct	(0) Writable		
VPchg[2:0]	5.8V		
T3T4ENset	Enabled		
T1T2ENset	Enabled		
T3T4VFset	Enabled		
T1T2VFset	Enabled		
T2T3lFchg[2:0]	1.0 x IFChg		
BoostRComp[3:0]	2		
FLTSelect[1:0]	(10) Reset		
BuckVSet[3:0]	5.0V		
AnSwCntl[1:0]	(01) Auto		
AICLTStep[1:0]	200ms		
WeakBatEna	Enabled		
BYPUVLO[2:0]	4.0V		
AICLMax[4:0]	500mA		
BYPDeb	500µs		
AICLTBlk[1:0]	1000ms		

Typical Application Circuit



Note: All capacitance values listed in this document refer to effective capacitance. Be sure to specify capacitors that will meet these requirements under typical system operating conditions taking into consideration the effects of voltage and temperature.

Ordering Information

•		
PART	TEMP RANGE	PIN-PACKAGE
MAX14748EWW+	-40°C to +85°C	54 WLP
MAX14748EWW+T	-40°C to +85°C	54 WLP
MAX14748BEWW+	-40°C to +85°C	54 WLP
MAX14748BEWW+T	-40°C to +85°C	54 WLP

⁺Denotes a lead(Pb)-free package/RoHS-compliant package. See <u>Table 61</u> for the device differences.

Chip Information PROCESS: BiCMOS

Maxim Integrated | 70 www.maximintegrated.com

 $T = \overline{Tape and reel}$.

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	6/17	Initial release	_
1	12/17	Added MAX14748C as future product	1, 6, 27, 29, 35, 36, 52, 58, 59, 67, 68, 70
2	3/18	Updated Bump Configuration, Figure 4, Register Map, Table 33, Table 60, and Ordering Information table	15, 27, 35, 52,
3	4/18	Updated the <i>Electrical Characteristics</i> table, <i>Register Map</i> , Tables 8, 17, 24, 33	3, 35, 38, 43, 47, 52
3.1	5/18	Corrected Bump Configuration diagram	15
4	5/18	Corrected Bump Configuration diagram	15
5	9/18	Updated the <i>Electrical Characteristics</i> table, <i>Typical Operating Characteristics</i> global conditions, and Table 60.	2–14, 67
6	10/18	Updated Table 59 and Table 61; corrected footnote and formatting for Table 3, and corrected typos in Register Tables to say "Read-Only"	36, 52–56, 61–62, 65, 68
7	3/19	Updated the Electrical Characteristics table and Figure 4	8, 27
8	7/19	Added the Deeply Discharged Battery section	30

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Офис по работе с юридическими лицами:

105318, г. Москва, ул. Щербаковская д. 3, офис 1107, 1118, ДЦ «Щербаковский»

Телефон: +7 495 668-12-70 (многоканальный)

Факс: +7 495 668-12-70 (доб.304)

E-mail: info@moschip.ru

Skype отдела продаж:

moschip.ru moschip.ru_6 moschip.ru_4 moschip.ru_9