

## ISL8483E, ISL8485E

ESD Protected to  $\pm 15\text{kV}$ , 5V, Low Power, High Speed or Slew Rate Limited  
RS-485/RS-422 Transceivers

FN6048  
Rev.13.00  
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The [ISL8483E](#) and [ISL8485E](#) are ESD protected, BiCMOS 5V powered, single transceivers that meet both the RS-485 and RS-422 standards for balanced communication. Each driver output/receiver input is protected against  $\pm 15\text{kV}$  ESD strikes without latch-up. Unlike competitive devices, this Renesas family is specified for 10% tolerance supplies (4.5V to 5.5V).

The ISL8483E uses slew rate limited drivers that reduce EMI and minimize reflections from improperly terminated transmission lines or unterminated stubs in multidrop and multipoint applications.

Data rates up to 10Mbps are achievable by using the ISL8485E, which features higher slew rates.

Both devices present a “single unit load” to the RS-485 bus, which allows up to 32 transceivers on the network.

Receiver (Rx) inputs feature a “fail-safe if open” design, which ensures a logic high Rx output if Rx inputs are floating.

Driver (Tx) outputs are short-circuit protected even for voltages exceeding the power supply voltage. Additionally, on-chip thermal shutdown circuitry disables the Tx outputs to prevent damage if power dissipation becomes excessive.

These half duplex configurations multiplex the Rx inputs and Tx outputs to allow transceivers with Rx and Tx disable functions in 8 Ld packages.

### Related Literature

For a full list of related documents, visit our website:

- [ISL8483E](#) and [ISL8485E](#) product pages

### Features

- Pb-Free (RoHS compliant)
- Extended industrial temperature options (+125°C)
- RS-485 I/O pin ESD protection .....  $\pm 15\text{kV}$  HBM
  - Class 3 ESD level on all other pins.....  $> 7\text{kV}$  HBM
- Specified for 10% tolerance supplies
- High data rate version (ISL8485E). . . . . up to 10Mbps
- Slew rate limited version for error free data transmission (ISL8483E) . . . . . up to 250kbps
- Single unit load allows up to 32 devices on the bus
- 1nA low current Shutdown mode (ISL8483E)
- Low quiescent current:
  - 160 $\mu\text{A}$  (ISL8483E)
  - 500 $\mu\text{A}$  (ISL8485E)
- -7V to +12V common-mode input voltage range
- Three-state Rx and Tx outputs
- 30ns propagation delays, 5ns skew (ISL8485E)
- Operate from a single +5V supply (10% tolerance)
- Current limiting and thermal shutdown for driver overload protection

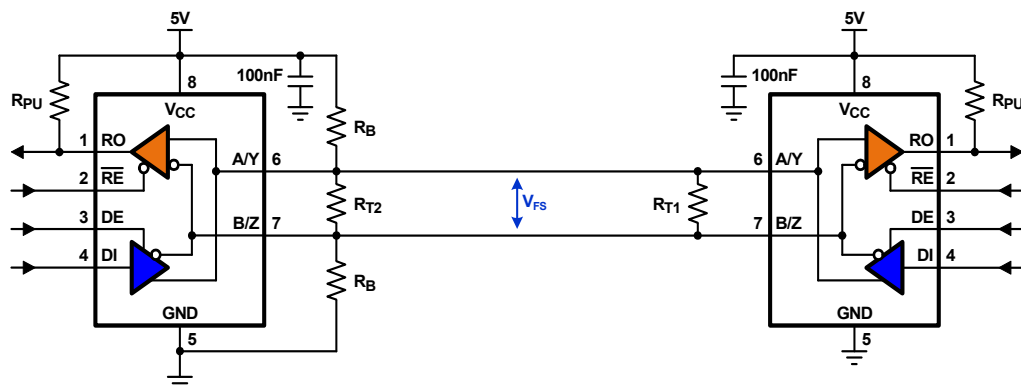
### Applications

- Factory automation
- Security networks
- Building environmental control systems
- Industrial/process control networks
- Level translators (such as RS-232 to RS-422)
- RS-232 “extension cords”

TABLE 1. SUMMARY OF FEATURES

PART NUMBER	HALF/FULL DUPLEX	NO. OF DEVICES ALLOWED ON BUS	DATA RATE (Mbps)	SLEW-RATE LIMITED?	RECEIVER/DRIVER ENABLE?	QUIESCENT $I_{CC}$ ( $\mu\text{A}$ )	LOW POWER SHUTDOWN?	PIN COUNT
ISL8483E	Half	32	0.25	Yes	Yes	160	Yes	8
ISL8485E	Half	32	10	No	Yes	500	No	8

## Typical Operating Circuit



To calculate the resistor values, refer to [TB509](#)

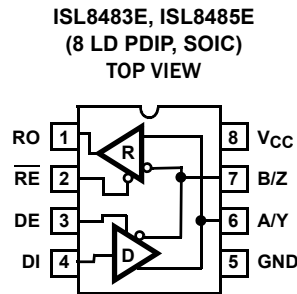
## Ordering Information

PART NUMBER (Notes 3, 4)	PART MARKING	TEMP. RANGE (°C)	TAPE AND REEL (UNITS) (Note 2)	PACKAGE (RoHS COMPLIANT)	PKG. DWG. #
ISL8483EIBZ	8483 EIBZ	-40 to +85	-	8 Ld SOIC	M8.15
ISL8483EIBZ-T	8483 EIBZ	-40 to +85	2.5k	8 Ld SOIC	M8.15
ISL8485EABZ	8485 EABZ	-40 to +125	-	8 Ld SOIC	M8.15
ISL8485EABZ-T	8485 EABZ	-40 to +125	2.5k	8 Ld SOIC	M8.15
ISL8485ECBZ	8485 ECBZ	0 to +70	-	8 Ld SOIC	M8.15
ISL8485ECBZ-T	8485 ECBZ	0 to +70	2.5k	8 Ld SOIC	M8.15
ISL8485EIBZ	8485 EIBZ	-40 to +85	-	8 Ld SOIC	M8.15
ISL8485EIBZ-T	8485 EIBZ	-40 to +85	2.5k	8 Ld SOIC	M8.15
ISL8485EIPZ	ISL 8485EIPZ	-40 to +85	-	8 Ld PDIP (Note 1)	E8.3

### NOTES:

- Pb-free PDIPs can be used for through hole wave solder processing only. They are not intended for use in reflow solder processing applications.
- Refer to [TB347](#) for details about reel specifications.
- These Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
- For Moisture Sensitivity Level (MSL), refer to the product information pages for the [ISL8483E](#) and the [ISL8485E](#). For more information on MSL, refer to [TB363](#).

## Pin Configuration



## Pin Descriptions

PIN	FUNCTION
RO	Receiver output: RO is high if A > B by at least 0.2V; RO is low if A < B by 0.2V or more; RO is high if A and B are unconnected (floating).
$\overline{RE}$	Receiver output enable. RO is enabled when $\overline{RE}$ is low; RO is high impedance when $\overline{RE}$ is high.
DE	Driver output enable. The driver outputs Y and Z are enabled by bringing DE high. They are high impedance when DE is low.
DI	Driver input. A low on DI forces output Y low and output Z high. Similarly, a high on DI forces output Y high and output Z low.
GND	Ground connection.
A/Y	$\pm 15\text{kV}$ HBM ESD protected, RS-485, RS-422 level noninverting receiver input and noninverting driver output. Pin is an input (A) if DE = 0; pin is an output (Y) if DE = 1.
$\overline{B/Z}$	$\pm 15\text{kV}$ HBM ESD protected, RS-485, RS-422 level inverting receiver input and inverting driver output. Pin is an input (B) if DE = 0; pin is an output (Z) if DE = 1.
VCC	System power supply input (4.5V to 5.5V).

## Truth Tables

TRANSMITTING				
INPUTS			OUTPUTS	
$\overline{RE}$	DE	DI	Z	Y
X	1	1	0	1
X	1	0	1	0
0	0	X	High-Z	High-Z
1	0	X	High-Z *	High-Z *

\*Shutdown mode for ISL8483E (see [Note 11](#))

RECEIVING			
INPUTS			OUTPUT
$\overline{RE}$	DE	A-B	RO
0	0	$V_{AB} \geq 0.2V$	1
0	0	$0.2V > V_{AB} > -0.2V$	Undetermined
0	0	$V_{AB} \leq -0.2V$	0
0	0	Inputs Open	1
1	0	X	High-Z *
1	1	X	High-Z

\*Shutdown mode for ISL8483E (see [Note 11](#))

## Absolute Maximum Ratings

V <sub>CC</sub> to Ground	7V
Input Voltages	
DI, DE, $\overline{RE}$	-0.5V to (V <sub>CC</sub> +0.5V)
Input/Output Voltages	
A/Y, B/Z	-8V to +12.5V
RO	-0.5V to (V <sub>CC</sub> +0.5V)
Short-Circuit Duration	
Y, Z	Continuous
ESD Rating	.See "ESD PERFORMANCE"

## Thermal Information

Thermal Resistance (Typical, <a href="#">Note 5</a> )	$\theta_{JA}$ (°C/W)
8 Ld SOIC Package	170
8 Ld PDIP Package*	140
Maximum Junction Temperature (Plastic Package)	+150°C
Maximum Storage Temperature Range	-65°C to +150°C
Pb-free reflow profile	see <a href="#">TB493</a>
*Pb-free PDIPs can be used for through hole wave solder processing only. They are not intended for use in reflow solder processing applications.	

## Operating Conditions

Temperature Range	
ISL8485ECx	0°C to +70°C
ISL848xEIx	-40°C to +85°C
ISL8485EAX	-40°C to +125°C

**CAUTION:** Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions can adversely impact product reliability and result in failures not covered by warranty.

### NOTE:

- $\theta_{JA}$  is measured with the component mounted on a low-effective thermal conductivity test board in free air. Refer to [TB379](#) for details.

**Electrical Specifications** Test Conditions: V<sub>CC</sub> = 4.5V to 5.5V; unless otherwise specified. Typical values are at V<sub>CC</sub> = 5V, T<sub>A</sub> = +25°C, ([Note 6](#))

PARAMETER	SYMBOL	TEST CONDITIONS	TEMP (°C)	MIN ( <a href="#">Note 16</a> )	TYP	MAX ( <a href="#">Note 16</a> )	UNIT	
<b>DC CHARACTERISTICS</b>								
Driver Differential V <sub>OUT</sub> (No Load)	V <sub>OD1</sub>		Full	-	-	V <sub>CC</sub>	V	
Driver Differential V <sub>OUT</sub> (With Load)	V <sub>OD2</sub>	R = 50Ω (RS-422), ( <a href="#">Figure 1 on page 6</a> )	Full	2	3	-	V	
		R = 27Ω (RS-485), ( <a href="#">Figure 1 on page 6</a> )	Full	1.5	2.3	5	V	
Change in Magnitude of Driver Differential V <sub>OUT</sub> for Complementary Output States	$\Delta V_{OD}$	R = 27Ω or 50Ω, ( <a href="#">Figure 1 on page 6</a> )	Full	-	0.01	0.2	V	
Driver Common-Mode V <sub>OUT</sub>	V <sub>OC</sub>	R = 27Ω or 50Ω, ( <a href="#">Figure 1 on page 6</a> )	Full	-	-	3	V	
Change in Magnitude of Driver Common-Mode V <sub>OUT</sub> for Complementary Output States	$\Delta V_{OC}$	R = 27Ω or 50Ω, ( <a href="#">Figure 1 on page 6</a> )	Full	-	0.01	0.2	V	
Logic Input High Voltage	V <sub>IH</sub>	DE, DI, $\overline{RE}$	Full	2	-	-	V	
Logic Input Low Voltage	V <sub>IL</sub>	DE, DI, $\overline{RE}$	Full	-	-	0.8	V	
Logic Input Current	I <sub>IN1</sub>	DE, DI, $\overline{RE}$ (ISL8483E)	Full	-2	-	2	μA	
	I <sub>IN1</sub>	DI (ISL8485E)	Full	-2	-	2	μA	
	I <sub>IN1</sub>	DE, $\overline{RE}$ (ISL8485E)	Full	-25	-	25	μA	
Input Current (A, B), ( <a href="#">Note 14</a> )	I <sub>IN2</sub>	DE = 0V, V <sub>CC</sub> = 0V or 4.5 to 5.5V	V <sub>IN</sub> = 12V	Full	-	-	1	mA
			V <sub>IN</sub> = -7V	Full	-	-	-0.8	mA
Receiver Differential Threshold Voltage	V <sub>TH</sub>	-7V ≤ V <sub>CM</sub> ≤ 12V	Full	-0.2	-	0.2	V	
Receiver Input Hysteresis	$\Delta V_{TH}$	V <sub>CM</sub> = 0V	+25	-	70	-	mV	
Receiver Output High Voltage	V <sub>OH</sub>	I <sub>O</sub> = -4mA, V <sub>ID</sub> = 200mV	Full	3.5	-	-	V	
Receiver Output Low Voltage	V <sub>OL</sub>	I <sub>O</sub> = -4mA, V <sub>ID</sub> = 200mV	Full	-	-	0.4	V	
Three-State (High Impedance) Receiver Output Current	I <sub>OZR</sub>	0.4V ≤ V <sub>O</sub> ≤ 2.4V	Full	-	-	±1	μA	

**Electrical Specifications** Test Conditions:  $V_{CC} = 4.5V$  to  $5.5V$ ; unless otherwise specified. Typical values are at  $V_{CC} = 5V$ ,  $T_A = +25^\circ C$ , (Note 6) (Continued)

PARAMETER	SYMBOL	TEST CONDITIONS	TEMP (°C)	MIN (Note 16)	TYP	MAX (Note 16)	UNIT	
Receiver Input Resistance	$R_{IN}$	$-7V \leq V_{CM} \leq 12V$	Full	12	-	-	k $\Omega$	
No-Load Supply Current, (Note 7)	$I_{CC}$	ISL8485E, DI, $\overline{RE} = 0V$ or $V_{CC}$	DE = $V_{CC}$	Full	-	700	900	$\mu A$
			DE = 0V	Full	-	500	565	$\mu A$
		ISL8483E, DI, $\overline{RE} = 0V$ or $V_{CC}$	DE = $V_{CC}$	Full	-	470	650	$\mu A$
			DE = 0V	Full	-	160	250	$\mu A$
Shutdown Supply Current	$I_{SHDN}$	ISL8483E, DE = 0V, $\overline{RE} = V_{CC}$ , DI = 0V or $V_{CC}$	Full	-	1	50	nA	
Driver Short-Circuit Current, $V_O = \text{High or Low}$	$I_{OSD1}$	DE = $V_{CC}$ , $-7V \leq V_Y$ or $V_Z \leq 12V$ , (Note 8)	Full	35	-	250	mA	
Receiver Short-Circuit Current	$I_{OSR}$	$0V \leq V_O \leq V_{CC}$	Full	7	-	85	mA	
<b>SWITCHING CHARACTERISTICS (ISL8485E)</b>								
Driver Input to Output Delay	$t_{PLH}, t_{PHL}$	$R_{DIFF} = 54\Omega$ , $C_L = 100pF$ , (Figure 2 on page 7)	Full	18	30	50	ns	
Driver Output Skew	$t_{SKEW}$	$R_{DIFF} = 54\Omega$ , $C_L = 100pF$ , (Figure 2 on page 7)	Full	-	2	10	ns	
Driver Differential Rise or Fall Time	$t_R, t_F$	$R_{DIFF} = 54\Omega$ , $C_L = 100pF$ , (Figure 2 on page 7)	Full	3	11	25	ns	
Driver Enable to Output High	$t_{ZH}$	$C_L = 100pF$ , SW = GND, (Figure 3 on page 7)	Full	-	17	70	ns	
Driver Enable to Output Low	$t_{ZL}$	$C_L = 100pF$ , SW = $V_{CC}$ , (Figure 3 on page 7)	Full	-	14	70	ns	
Driver Disable from Output High	$t_{HZ}$	$C_L = 15pF$ , SW = GND, (Figure 3 on page 7)	Full	-	19	70	ns	
Driver Disable from Output Low	$t_{LZ}$	$C_L = 15pF$ , SW = $V_{CC}$ , (Figure 3 on page 7)	Full	-	13	70	ns	
Receiver Input to Output Delay	$t_{PLH}, t_{PHL}$	(Figure 4 on page 7)	Full	30	40	150	ns	
Receiver Skew   $t_{PLH} - t_{PHL}$	$t_{SKD}$	(Figure 4 on page 7)	+25	-	5	-	ns	
Receiver Enable to Output High	$t_{ZH}$	$C_L = 15pF$ , SW = GND, (Figure 5 on page 8)	Full	-	9	50	ns	
Receiver Enable to Output Low	$t_{ZL}$	$C_L = 15pF$ , SW = $V_{CC}$ , (Figure 5 on page 8)	Full	-	9	50	ns	
Receiver Disable from Output High	$t_{HZ}$	$C_L = 15pF$ , SW = GND, (Figure 5 on page 8)	Full	-	9	50	ns	
Receiver Disable from Output Low	$t_{LZ}$	$C_L = 15pF$ , SW = $V_{CC}$ , (Figure 5 on page 8)	Full	-	9	50	ns	
Maximum Data Rate	$f_{MAX}$	(Note 15)	Full	10	-	-	Mbps	
<b>SWITCHING CHARACTERISTICS (ISL8483E)</b>								
Driver Input to Output Delay	$t_{PLH}, t_{PHL}$	$R_{DIFF} = 54\Omega$ , $C_L = 100pF$ , (Figure 2 on page 7)	Full	250	800	2000	ns	
Driver Output Skew	$t_{SKEW}$	$R_{DIFF} = 54\Omega$ , $C_L = 100pF$ , (Figure 2 on page 7)	Full	-	160	800	ns	
Driver Differential Rise or Fall Time	$t_R, t_F$	$R_{DIFF} = 54\Omega$ , $C_L = 100pF$ , (Figure 2 on page 7)	Full	250	800	2000	ns	
Driver Enable to Output High	$t_{ZH}$	$C_L = 100pF$ , SW = GND, (Figure 3 on page 7), (Note 9)	Full	250	-	2000	ns	
Driver Enable to Output Low	$t_{ZL}$	$C_L = 100pF$ , SW = $V_{CC}$ , (Figure 3 on page 7), (Note 9)	Full	250	-	2000	ns	
Driver Disable from Output High	$t_{HZ}$	$C_L = 15pF$ , SW = GND, (Figure 3 on page 7)	Full	300	-	3000	ns	
Driver Disable from Output Low	$t_{LZ}$	$C_L = 15pF$ , SW = $V_{CC}$ , (Figure 3 on page 7)	Full	300	-	3000	ns	
Receiver Input to Output Delay	$t_{PLH}, t_{PHL}$	(Figure 4 on page 7)	Full	250	350	2000	ns	
Receiver Skew   $t_{PLH} - t_{PHL}$	$t_{SKD}$	(Figure 4 on page 7)	+25	-	25	-	ns	
Receiver Enable to Output High	$t_{ZH}$	$C_L = 15pF$ , SW = GND, (Figure 5 on page 8), (Note 10)	Full	-	10	50	ns	
Receiver Enable to Output Low	$t_{ZL}$	$C_L = 15pF$ , SW = $V_{CC}$ , (Figure 5 on page 8), (Note 10)	Full	-	10	50	ns	

**Electrical Specifications** Test Conditions:  $V_{CC} = 4.5V$  to  $5.5V$ ; unless otherwise specified. Typical values are at  $V_{CC} = 5V$ ,  $T_A = +25^\circ C$ , (Note 6) (Continued)

PARAMETER	SYMBOL	TEST CONDITIONS	TEMP (°C)	MIN (Note 16)	TYP	MAX (Note 16)	UNIT
Receiver Disable from Output High	$t_{HZ}$	$C_L = 15pF$ , SW = GND, (Figure 5 on page 8)	Full	-	10	50	ns
Receiver Disable from Output Low	$t_{LZ}$	$C_L = 15pF$ , SW = $V_{CC}$ , (Figure 5 on page 8)	Full	-	10	50	ns
Maximum Data Rate	$f_{MAX}$	(Note 15)	Full	250	-	-	kbps
Time to Shutdown	$t_{SHDN}$	(Note 11)	Full	50	200	600	ns
Driver Enable from Shutdown to Output High	$t_{ZH(SHDN)}$	$C_L = 100pF$ , SW = GND, (Figure 3 on page 7), (Notes 11, 12)	Full	-	-	2000	$\mu s$
Driver Enable from Shutdown to Output Low	$t_{ZL(SHDN)}$	$C_L = 100pF$ , SW = $V_{CC}$ , (Figure 5 on page 8), (Notes 11, 12)	Full	-	-	2000	$\mu s$
Receiver Enable from Shutdown to Output High	$t_{ZH(SHDN)}$	$C_L = 15pF$ , SW = GND, (Figure 5 on page 8), (Notes 11, 13)	Full	-	-	2500	ns
Receiver Enable from Shutdown to Output Low	$t_{ZL(SHDN)}$	$C_L = 15pF$ , SW = $V_{CC}$ , (Figure 5 on page 8), (Notes 11, 13)	Full	-	-	2500	ns
<b>ESD PERFORMANCE</b>							
RS-485 Pins (A/Y, B/Z)		Human Body Model	+25	-	$\pm 15$	-	kV
All Other Pins			+25	-	$>\pm 7$	-	kV

**NOTES:**

- All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to device ground unless otherwise specified.
- Supply current specification is valid for loaded drivers when DE = 0V.
- Applies to peak current. See "Typical Performance Curves" on page 10 for more information.
- When testing the ISL8483E, keep  $\overline{RE} = 0$  to prevent the device from entering SHDN.
- When testing the ISL8483E, the  $\overline{RE}$  signal high time must be short enough (typically <200ns) to prevent the device from entering SHDN.
- The ISL8483E is put into shutdown by bringing  $\overline{RE}$  high and DE low. If the inputs are in this state for less than 50ns, the parts are ensured not to enter shutdown. If the inputs are in this state for at least 600ns, the parts are ensured to have entered shutdown. See "Low Power Shutdown Mode (ISL8483E Only)" on page 9.
- Keep  $\overline{RE} = V_{CC}$ , and set the DE signal low time >600ns to ensure that the device enters SHDN.
- Set the  $\overline{RE}$  signal high time >600ns to ensure that the device enters SHDN.
- Devices meeting these limits are denoted as "single unit load (1 UL)" transceivers. The RS-485 standard allows up to 32 Unit Loads on the bus.
- Limits established by characterization and are not production tested.
- Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.

## Test Circuits and Waveforms

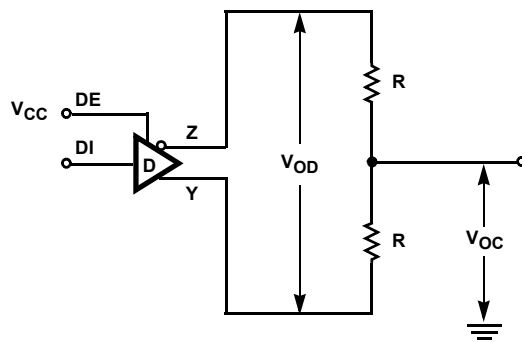


FIGURE 1. DRIVER  $V_{OD}$  AND  $V_{OC}$

## Test Circuits and Waveforms (Continued)

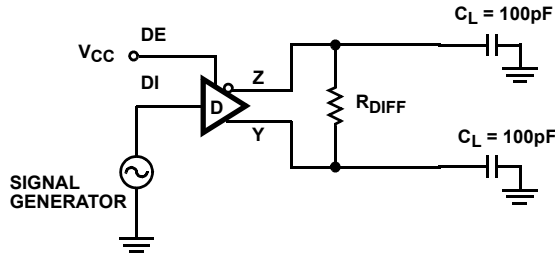
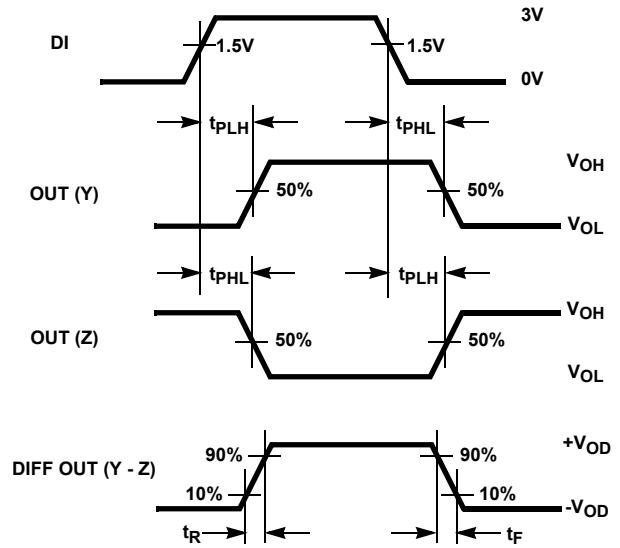


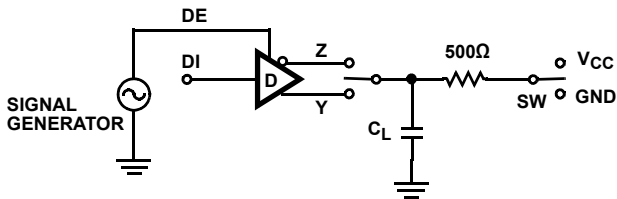
FIGURE 2A. TEST CIRCUIT

FIGURE 2. DRIVER PROPAGATION DELAY AND DIFFERENTIAL TRANSITION TIMES



$$\text{SKEW} = |t_{pLH}(\text{Y or Z}) - t_{pHL}(\text{Z or Y})|$$

FIGURE 2B. MEASUREMENT POINTS



(SHDN) FOR ISL8483E ONLY

PARAMETER	OUTPUT	$\overline{\text{RE}}$	DI	SW	$C_L$ (pF)
$t_{HZ}$	Y/Z	X	1 / 0	GND	15
$t_{LZ}$	Y/Z	X	0 / 1	$V_{CC}$	15
$t_{ZH}$	Y/Z	0 (Note 9)	1 / 0	GND	100
$t_{ZL}$	Y/Z	0 (Note 9)	0 / 1	$V_{CC}$	100
$t_{ZH}(\text{SHDN})$	Y/Z	1 (Note 12)	1 / 0	GND	100
$t_{ZL}(\text{SHDN})$	Y/Z	1 (Note 12)	0 / 1	$V_{CC}$	100

FIGURE 3A. TEST CIRCUIT

FIGURE 3. DRIVER ENABLE AND DISABLE TIMES

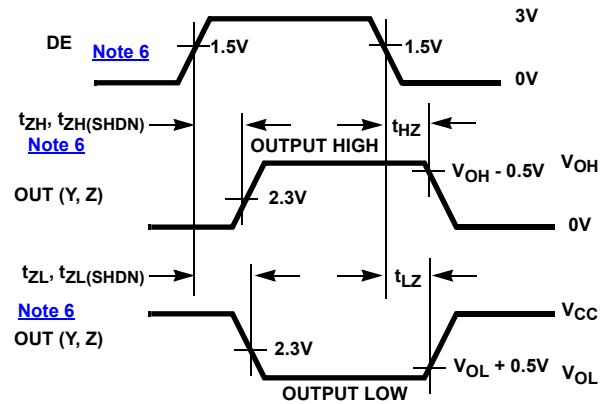


FIGURE 3B. MEASUREMENT POINTS

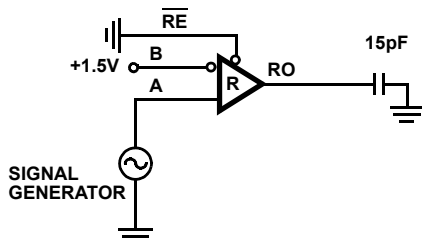


FIGURE 4A. TEST CIRCUIT

FIGURE 4. RECEIVER PROPAGATION DELAY

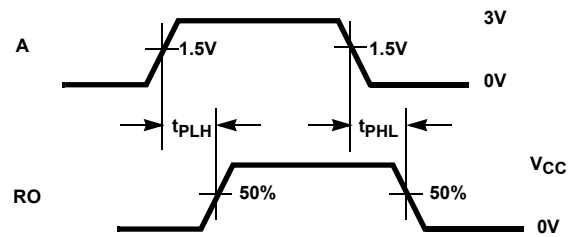
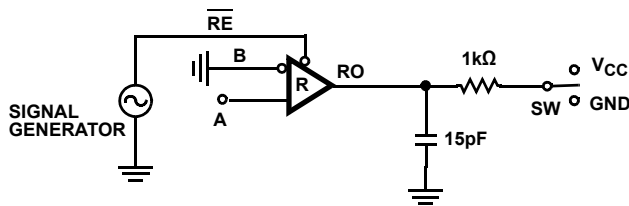


FIGURE 4B. MEASUREMENT POINTS

## Test Circuits and Waveforms (Continued)



(SHDN) FOR ISL8483E ONLY

PARAMETER	DE	A	SW
$t_{HZ}$	0	+1.5V	GND
$t_{LZ}$	0	-1.5V	$V_{CC}$
$t_{ZH}$ (Note 10)	0	+1.5V	GND
$t_{ZL}$ (Note 10)	0	-1.5V	$V_{CC}$
$t_{ZH(SHDN)}$ (Note 13)	0	+1.5V	GND
$t_{ZL(SHDN)}$ (Note 13)	0	-1.5V	$V_{CC}$

FIGURE 5A. TEST CIRCUIT

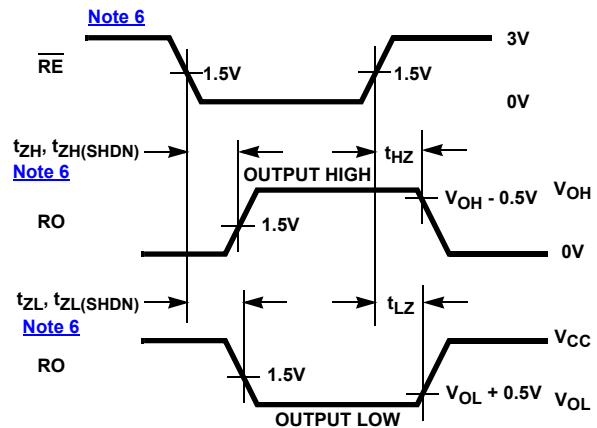


FIGURE 5B. MEASUREMENT POINTS

FIGURE 5. RECEIVER ENABLE AND DISABLE TIMES

## Application Information

RS-485 and RS-422 are differential (balanced) data transmission standards for use in long haul or noisy environments. RS-422 is a subset of RS-485, so RS-485 transceivers are also RS-422 compliant. RS-422 is a point-to-multipoint (multidrop) standard that allows only one driver and up to 10 receivers on each bus, assuming one unit load devices. RS-485 is a true multipoint standard that allows up to 32 one unit load devices (any combination of drivers and receivers) on each bus. To allow for multipoint operation, the RS-485 specification requires that drivers handle bus contention without sustaining any damage.

Another important advantage of RS-485 is the extended Common-Mode Range (CMR). The CMR specifies that the driver outputs and receiver inputs withstand signals that range from +12V to -7V. RS-422 and RS-485 are intended for runs as long as 4000 ft, so the wide CMR is necessary to handle ground potential differences and voltages induced in the cable by external fields.

### Receiver Features

The devices use a differential input receiver for maximum noise immunity and common-mode rejection. Input sensitivity is  $\pm 200\text{mV}$  as required by the RS-422 and RS-485 specifications.

Receiver input impedance surpasses the RS-422 spec of  $4\text{k}\Omega$  and meets the RS-485 "Unit Load" requirement of  $12\text{k}\Omega$  minimum.

Receiver inputs function with common-mode voltages as high as  $\pm 7\text{V}$  outside the power supplies (for example, +12V and -7V), making them ideal for long networks where induced voltages are a realistic concern.

All the receivers include a "fail-safe if open" function that ensures a high level receiver output if the receiver inputs are unconnected (floating).

Receivers easily meet the data rates supported by the corresponding driver.

ISL8483E and ISL8485E receiver outputs are tri-statable through the active low  $\overline{\text{RE}}$  input.

### Driver Features

The RS-485 and RS-422 drivers are differential output devices that deliver at least 1.5V across a  $54\Omega$  load (RS-485) and at least 2V across a  $100\Omega$  load (RS-422). The drivers feature low propagation delay skew to maximize bit width and to minimize EMI.

The ISL8483E and ISL8485E drivers are tri-statable using the active high DE input.

The ISL8483E driver outputs are slew rate limited to minimize EMI and to minimize reflections in unterminated or improperly terminated networks. The data rate on these slew rate limited versions is a maximum of 250kbps. The ISL8485E driver outputs are not limited, so faster output transition times allow data rates of at least 10Mbps.



## Data Rate, Cables, and Terminations

RS-485 and RS-422 are intended for network lengths up to 4000 ft, but the maximum system data rate decreases as the transmission length increases. Devices operating at 10Mbps are limited to lengths less than 100 feet, and the 250kbps versions can operate at full data rates with lengths in excess of 1000 ft.

Twisted pair cable is the cable of choice for the RS-485 and RS-422 networks. Twisted pair cables tend to pick up noise and other electromagnetically induced voltages as common-mode signals, which are effectively rejected by the differential receivers in these ICs.

Proper termination is imperative when using the 10Mbps devices to minimize reflections. Short networks using the 250kbps versions do not need to be terminated, but terminations are recommended unless power dissipation is an overriding concern.

In point-to-point or point-to-multipoint (single driver on bus) networks, terminate the main cable in its characteristic impedance (typically 120Ω) at the end farthest from the driver. In multi-receiver applications, keep stubs connecting receivers to the main cable as short as possible. In multipoint (multi-driver) systems, terminate the main cable in its characteristic impedance at both ends. Keep stubs that are connecting a transceiver to the main cable as short as possible.

## Built-In Driver Overload Protection

The RS-485 specification requires that drivers survive worst case bus contentions undamaged. The ISL848xE devices meet this requirement through driver output short-circuit current limits and on-chip thermal shutdown circuitry.

The driver output stages incorporate short-circuit current limiting circuitry that ensures that the output current never exceeds the RS-485 specification, even at the common-mode voltage range extremes. Also, these devices use a foldback circuit that reduces the short-circuit current and consequently the power dissipation when the contending voltage exceeds either supply.

In the event of a major short-circuit condition, the ISL848xE devices perform a thermal shutdown that disables the drivers whenever the die temperature becomes excessive. This eliminates the power dissipation allowing the die to cool. The drivers automatically re-enable after the die temperature drops about 15°. If the contention persists, the thermal shutdown/re-enable cycle repeats until the fault is cleared. Receivers stay operational during thermal shutdown.

## Low Power Shutdown Mode (ISL8483E Only)

These CMOS transceivers all use a fraction of the power required by their bipolar counterparts, but the ISL8483E includes a shutdown feature that reduces the already low quiescent  $I_{CC}$  to a 1nA trickle. The ISL8483E enters shutdown whenever the receiver and driver are *simultaneously* disabled ( $\overline{RE} = V_{CC}$  and  $DE = GND$ ) for a period of at least 600ns. Disabling both the driver and the receiver for fewer than 50ns ensures that the ISL8483E does not enter shutdown.

Note that receiver and driver enable times increase when the ISL8483E enables from shutdown. Refer to [Notes 9](#) through [Notes 12](#) on [page 6](#) at the end of the [“Electrical Specifications”](#) table for more information.

## ESD Protection

All pins on these interface devices include Class 3 Human Body Model (HBM) ESD protection structures, but the RS-485 pins (driver outputs and receiver inputs) incorporate advanced structures allowing them to survive ESD events in excess of ±15kV HBM. The RS-485 pins are particularly vulnerable to ESD damage because they typically connect to an exposed port on the exterior of the finished product. Simply touching the port pins or connecting a cable can cause an ESD event that might destroy unprotected ICs. These new ESD structures protect the device whether or not it is powered up without either allowing any latchup mechanism to activate and without degrading the RS-485 common-mode range of -7V to +12V. The built-in ESD protection eliminates the need for board level protection structures (such as transient suppression diodes) and the associated, undesirable capacitive load that they present.

## Human Body Model Testing

As the name implies, the HBM test method emulates the ESD event delivered to an IC during human handling. The tester delivers the charge stored on a 100pF capacitor through a 1.5kΩ current limiting resistor into the pin under test. The HBM method determines an IC's ability to withstand the ESD events typically present during handling and manufacturing.

The RS-485 pin survivability on this high ESD family has been characterized to be in excess of ±15kV for discharges to GND.

## Die Characteristics

### SUBSTRATE POTENTIAL (POWERED UP):

GND

### TRANSISTOR COUNT:

518

### PROCESS:

Si Gate CMOS

**Typical Performance Curves**  $V_{CC} = 5V$ ,  $T_A = +25^\circ C$ , ISL8483E and ISL8485E; unless otherwise specified.

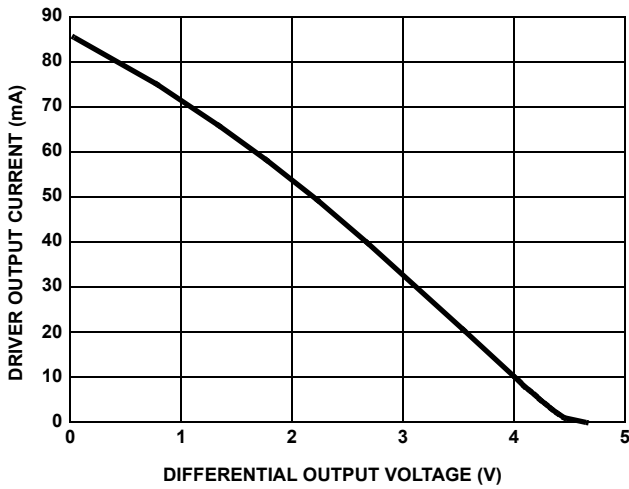


FIGURE 6. DRIVER OUTPUT CURRENT vs DIFFERENTIAL OUTPUT VOLTAGE

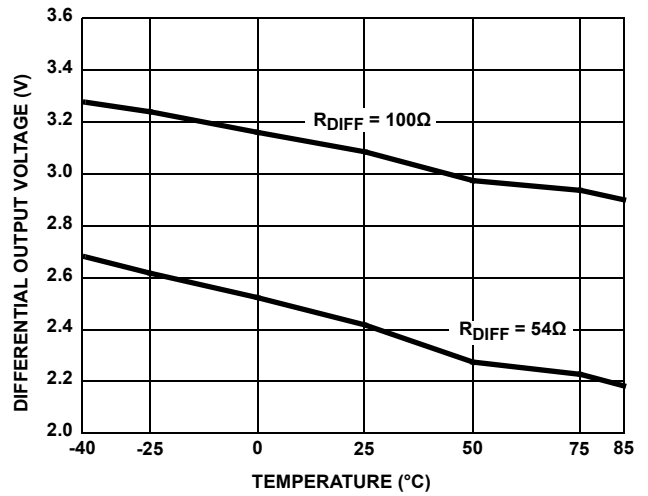


FIGURE 7. DRIVER DIFFERENTIAL OUTPUT VOLTAGE vs TEMPERATURE

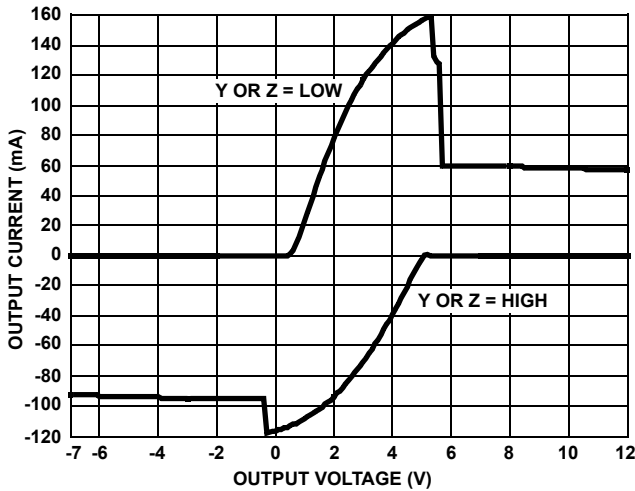


FIGURE 8. DRIVER OUTPUT CURRENT vs SHORT-CIRCUIT VOLTAGE

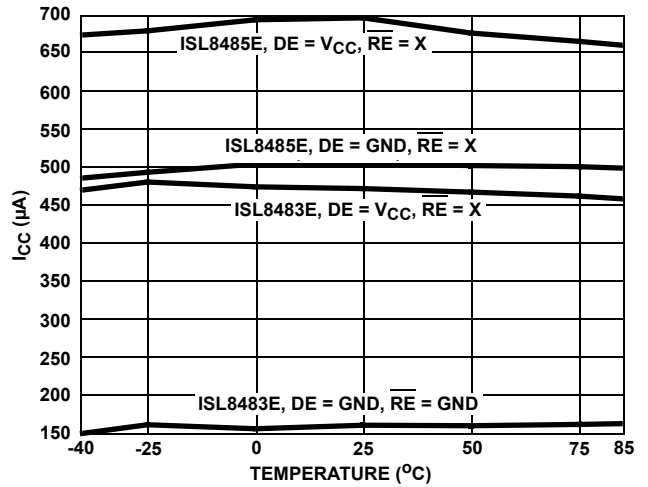


FIGURE 9. SUPPLY CURRENT vs TEMPERATURE

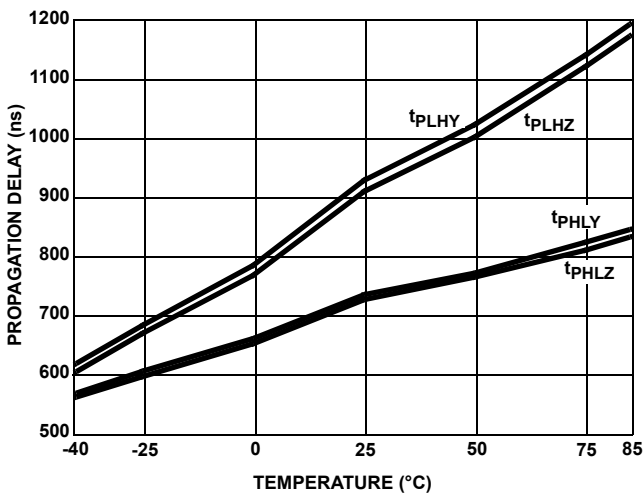


FIGURE 10. DRIVER PROPAGATION DELAY vs TEMPERATURE (ISL8483E)

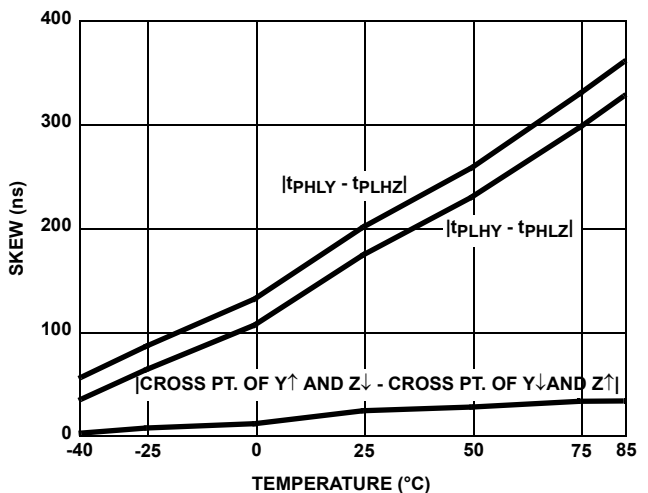


FIGURE 11. DRIVER SKEW vs TEMPERATURE (ISL8483E)

**Typical Performance Curves**  $V_{CC} = 5V, T_A = +25^\circ C$ , ISL8483E and ISL8485E; unless otherwise specified. (Continued)

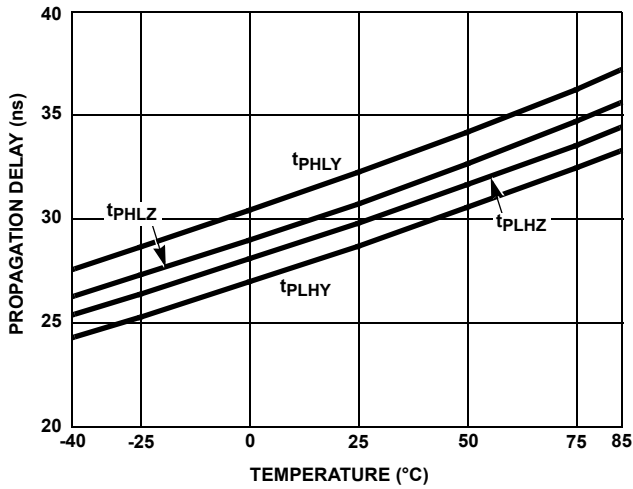


FIGURE 12. DRIVER PROPAGATION DELAY vs TEMPERATURE (ISL8485E)

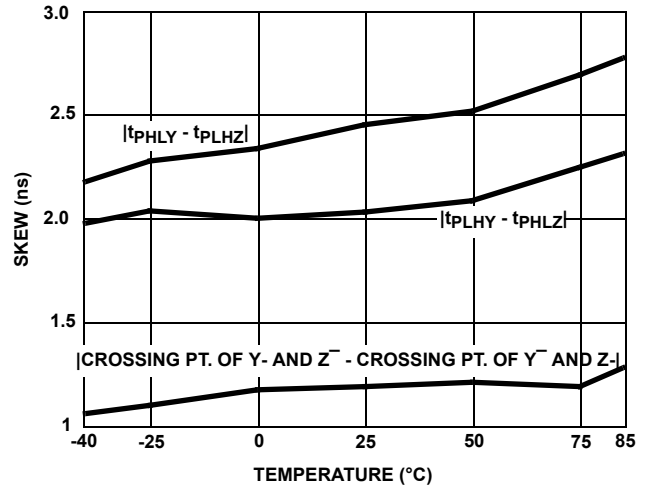


FIGURE 13. DRIVER SKEW vs TEMPERATURE (ISL8485E)

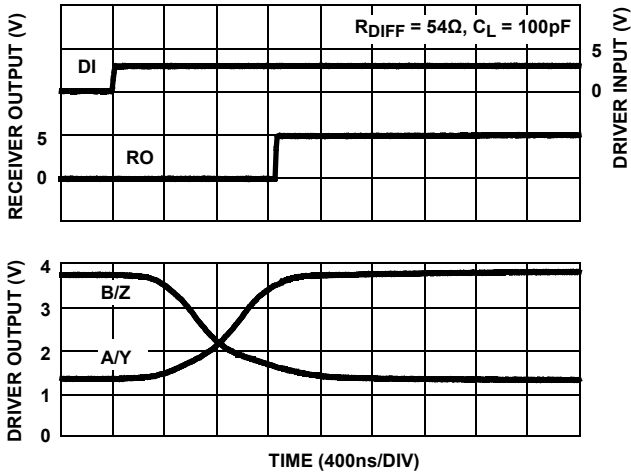


FIGURE 14. DRIVER AND RECEIVER WAVEFORMS, LOW TO HIGH (ISL8483E)

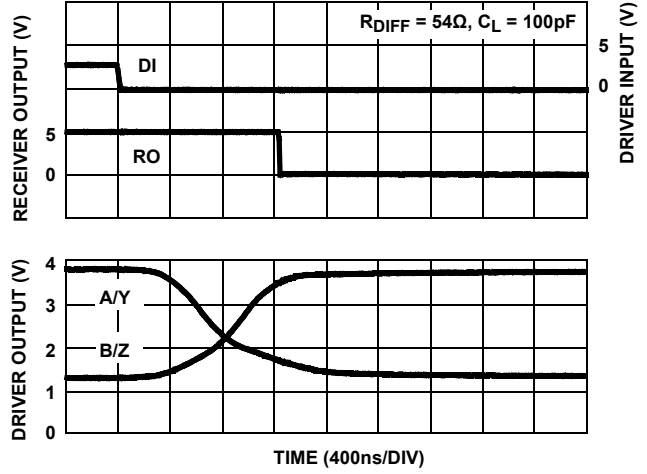


FIGURE 15. DRIVER AND RECEIVER WAVEFORMS, HIGH TO LOW (ISL8483E)

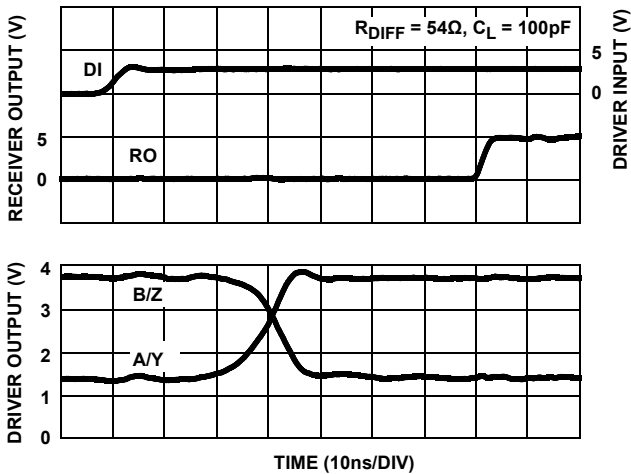


FIGURE 16. DRIVER AND RECEIVER WAVEFORMS, LOW TO HIGH (ISL8485E)

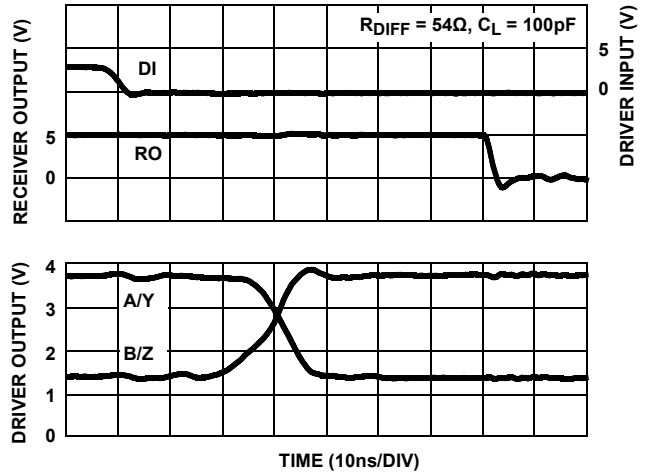


FIGURE 17. DRIVER AND RECEIVER WAVEFORMS, HIGH TO LOW (ISL8485E)

## Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please visit our website to make sure that you have the latest revision.

DATE	REVISION	CHANGE
Sept 24, 2018	FN6048.13	Updated the Ordering Information table by adding tape and reel information, removing part, and updating notes. Updated Typical Operating Circuits on page 2. Removed About Intersil section and updated disclaimer.
Aug 31, 2017	FN6048.12	Updated Receiving Truth table on page 2. Applied Intersil A Renesas Company template.
May 8, 2017	FN6048.11	Applied new header/footer Removed any mention of military version. Updated ordering information table on page 2 as follows: Updated Note 2, added Notes 3, and 5.
Sept 3, 2015	FN6048.10	- Ordering Information Table on page 2. - Added Revision History. - Added About Intersil Verbiage. -Updated POD M8.15 to most current revision with changes as follows: -Revision 1 to Revision 2 Changes: Updated to new POD format by removing table and moving dimensions onto drawing and adding land pattern -Revision 2 to Revision 3 Changes: Changed Note 1 "1982" to "1994" Changed in Typical Recommended Land Pattern the following: 2.41(0.095) to 2.20(0.087) 0.76 (0.030) to 0.60(0.023) 0.200 to 5.20(0.205) -Revision 3 to Revision 4 Changes: Changed Note 1 "1982" to "1994"

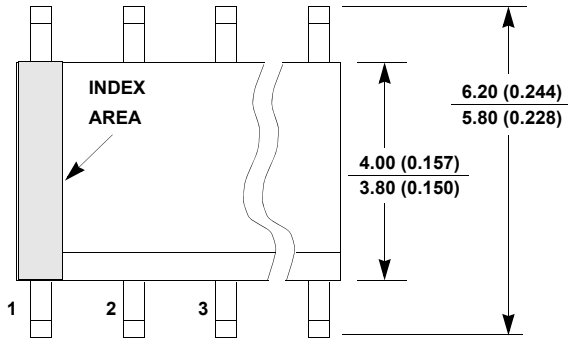
# Package Outline Drawings

For the most recent package outline drawing, see [M8.15](#).

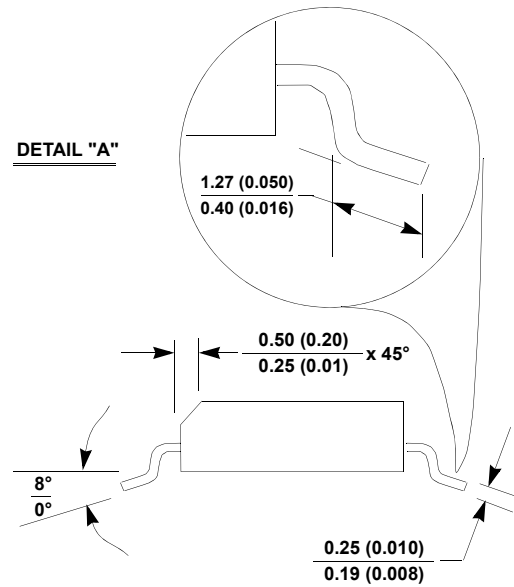
## M8.15

8 lead narrow body small outline plastic package

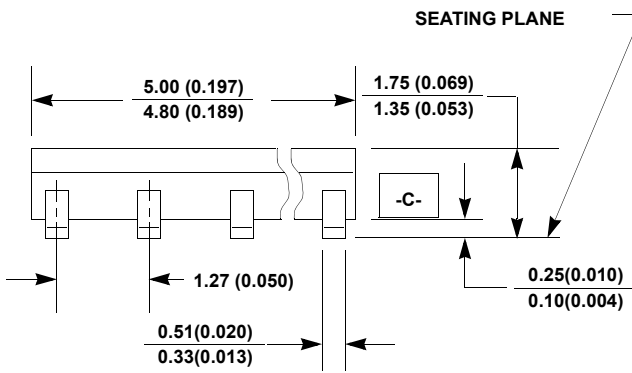
Rev 4, 1/12



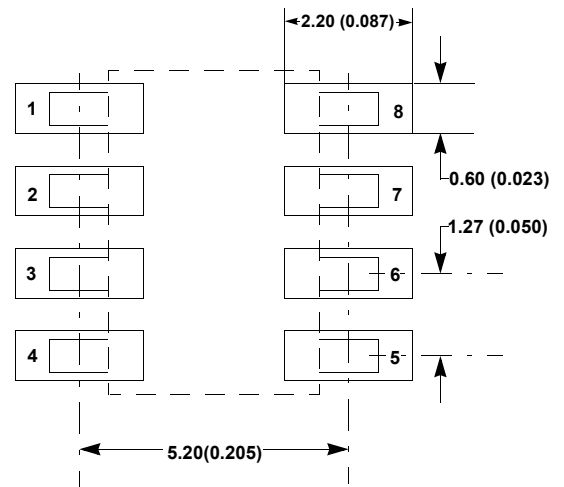
TOP VIEW



SIDE VIEW "B"



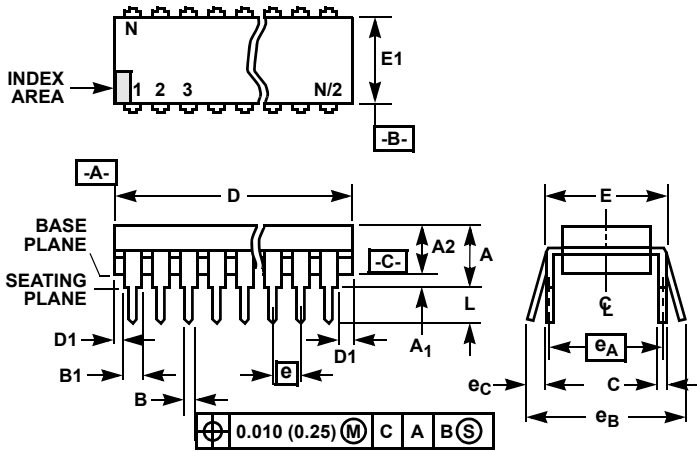
SIDE VIEW "A"



TYPICAL RECOMMENDED LAND PATTERN

**NOTES:**

17. Dimensioning and tolerancing per ANSI Y14.5M-1994.
18. Package length does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
19. Package width does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
20. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
21. Terminal numbers are shown for reference only.
22. The lead width as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch).
23. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.
24. This outline conforms to JEDEC publication MS-012-AA ISSUE C.



### E8.3 (JEDEC MS-001-BA ISSUE D)

#### 8 LEAD DUAL-IN-LINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.210	-	5.33	4
A1	0.015	-	0.39	-	4
A2	0.115	0.195	2.93	4.95	-
B	0.014	0.022	0.356	0.558	-
B1	0.045	0.070	1.15	1.77	8, 10
C	0.008	0.014	0.204	0.355	-
D	0.355	0.400	9.01	10.16	5
D1	0.005	-	0.13	-	5
E	0.300	0.325	7.62	8.25	6
E1	0.240	0.280	6.10	7.11	5
e	0.100 BSC		2.54 BSC		-
eA	0.300 BSC		7.62 BSC		6
eB	-	0.430	-	10.92	7
L	0.115	0.150	2.93	3.81	4
N	8		8		9

Rev. 0 12/93

**NOTES:**

- Controlling Dimensions: INCH. In case of conflict between English and Metric dimensions, the inch dimensions control.
- Dimensioning and tolerancing per ANSI Y14.5M-1982.
- Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication No. 95.
- Dimensions A, A1 and L are measured with the package seated in JEDEC seating plane gauge GS-3.
- D, D1, and E1 dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 inch (0.25mm).
- E and e<sub>A</sub> are measured with the leads constrained to be perpendicular to datum -C-.
- e<sub>B</sub> and e<sub>C</sub> are measured at the lead tips with the leads unconstrained. e<sub>C</sub> must be zero or greater.
- B1 maximum dimensions do not include dambar protrusions. Dambar protrusions shall not exceed 0.010 inch (0.25mm).
- N is the maximum number of terminal positions.
- Corner leads (1, N, N/2 and N/2 + 1) for E8.3, E16.3, E18.3, E28.3, E42.6 will have a B1 dimension of 0.030 - 0.045 inch (0.76 - 1.14mm).

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(Rev.4.0-1 November 2017)



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