

54ABT/74ABT373

Octal Transparent Latch with TRI-STATE® Outputs

General Description

The 54ABT373 consists of eight latches with TRI-STATE outputs for bus organized system applications. The flip-flops appear transparent to the data when Latch Enable (LE) is HIGH. When LE is LOW, the data that meets the setup times is latched. Data appears on the bus when the Output Enable (\overline{OE}) is LOW. When \overline{OE} is HIGH the bus output is in the high impedance state.

Features

- TRI-STATE outputs for bus interfacing
- Output sink capability of 64 mA, source capability of 32 mA
- Guaranteed output skew
- Guaranteed multiple output switching specifications
- Output switching specified for both 50 pF and 250 pF loads
- Guaranteed simultaneous switching, noise level and dynamic threshold performance
- Guaranteed latchup protection
- High impedance glitch free bus loading during entire power up and power down
- Nondestructive hot insertion capability
- Standard Military Drawing (SMD) 5962-9321801

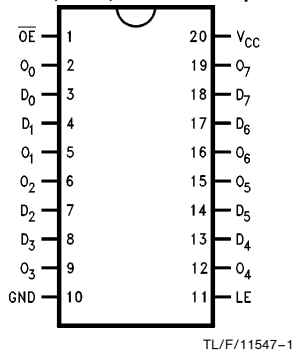
Commercial	Military	Package Number	Package Description
74ABT373CSC (Note 1)		M20B	20-Lead (0.300" Wide) Molded Small Outline, JEDEC
74ABT373CSJ (Note 1)		M20D	20-Lead (0.300" Wide) Molded Small Outline, EIAJ
74ABT373CPC		N20B	20-Lead (0.300" Wide) Molded Dual-In-Line
	54ABT373J/883	J20A	20-Lead Ceramic Dual-In-Line
74ABT373CMSA (Note 1)		MSA20	20-Lead Molded Shrink Small Outline, EIAJ Type II
	54ABT373W/883	W20A	20-Lead Cerpack
	54ABT373E/883	E20A	20-Lead Ceramic Leadless Chip Carrier, Type C
74ABT373CMTC (Notes 1, 2)		MTC20	20-Lead Molded Thin Shrink Small Outline, JEDEC

Note 1: Devices also available in 13" reel. Use suffix = SCX, SJX, MSAX, and MTCX.

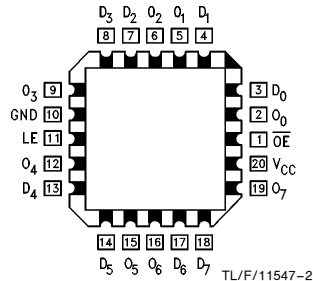
Note 2: Contact factory for package availability.

Connection Diagrams

Pin Assignment
for DIP, SOIC, SSOP and Flatpak



Pin Assignment
for LCC



Pin Names	Description
D ₀ –D ₇	Data Inputs
LE	Latch Enable Input (Active HIGH)
\overline{OE}	Output Enable Input (Active LOW)
O ₀ –O ₇	TRI-STATE Latch Outputs

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Functional Description

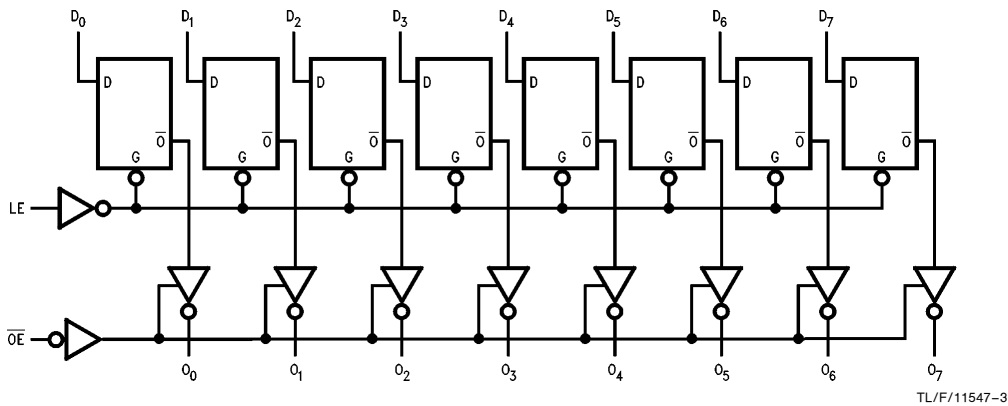
The 'ABT373 contains eight D-type latches with TRI-STATE output buffers. When the Latch Enable (LE) input is HIGH, data on the D_n inputs enters the latches. In this condition the latches are transparent, i.e., a latch output will change state each time its D input changes. When LE is LOW, the latches store the information that was present on the D inputs a setup time preceding the HIGH-to-LOW transition of LE. The TRI-STATE buffers are controlled by the Output Enable (\overline{OE}) input. When \overline{OE} is LOW, the buffers are in the bi-state mode. When \overline{OE} is HIGH the buffers are in the high impedance mode but this does not interfere with entering new data into the latches.

Truth Table

Inputs			Output
LE	\overline{OE}	D_n	O_n
H	L	H	H
H	L	L	L
L	L	X	O_n (no change)
X	H	X	Z

H = HIGH Voltage Level
 L = LOW Voltage Level
 X = Immaterial
 Z = High Impedance State

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
Ambient Temperature under Bias	−55°C to +125°C
Junction Temperature under Bias	
Ceramic	−55°C to +175°C
Plastic	−55°C to +150°C
V _{CC} Pin Potential to Ground Pin	−0.5V to +7.0V
Input Voltage (Note 2)	−0.5V to +7.0V
Input Current (Note 2)	−30 mA to +5.0 mA
Voltage Applied to Any Output in the Disabled or Power-Off State in the HIGH State	−0.5V to +5.5V −0.5V to V _{CC}
Current Applied to Output in LOW State (Max)	twice the rated I _{OL} (mA)

DC Latchup Source Current: \overline{OE} Pin −150 mA
(Across Comm Operating Range) Other Pins −500 mA

Over Voltage Latchup (I/O) 10V

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

Recommended Operating Conditions

Free Air Ambient Temperature	
Military	−55°C to +125°C
Commercial	−40°C to +85°C
Supply Voltage	
Military	+4.5V to +5.5V
Commercial	+4.5V to +5.5V
Minimum Input Edge Rate	($\Delta V/\Delta t$)
Data Input	50 mV/ns
Enable Input	20 mV/ns

DC Electrical Characteristics

Symbol	Parameter	ABT373			Units	V _{CC}	Conditions
		Min	Typ	Max			
V _{IH}	Input HIGH Voltage	2.0			V		Recognized HIGH Signal
V _{IL}	Input LOW Voltage			0.8	V		Recognized LOW Signal
V _{CD}	Input Clamp Diode Voltage			−1.2	V	Min	I _{IN} = −18 mA
V _{OH}	Output HIGH Voltage	54ABT/74ABT 54ABT 74ABT	2.5 2.0 2.0		V	Min	I _{OH} = −3 mA I _{OH} = −24 mA I _{OH} = −32 mA
V _{OL}	Output LOW Voltage	54ABT 74ABT		0.55 0.55	V	Min	I _{OL} = 48 mA I _{OL} = 64 mA
I _{IH}	Input HIGH Current			5 5	μA	Max	V _{IN} = 2.7V (Note 2) V _{IN} = V _{CC}
I _{BVI}	Input HIGH Current Breakdown Test			7	μA	Max	V _{IN} = 7.0V
I _{IL}	Input LOW Current			−5 −5	μA	Max	V _{IN} = 0.5V (Note 2) V _{IN} = 0.0V
V _{ID}	Input Leakage Test	4.75			V	0.0	I _{ID} = 1.9 μA All Other Pins Grounded
I _{OZH}	Output Leakage Current			50	μA	0 – 5.5V	V _{OUT} = 2.7V; \overline{OE} = 2.0V
I _{OZL}	Output Leakage Current			−50	μA	0 – 5.5V	V _{OUT} = 0.5V; \overline{OE} = 2.0V
I _{OS}	Output Short-Circuit Current	−100		−275	mA	Max	V _{OUT} = 0.0V
I _{CEX}	Output High Leakage Current			50	μA	Max	V _{OUT} = V _{CC}
I _{ZZ}	Bus Drainage Test			100	μA	0.0	V _{OUT} = 5.5V; All Others GND
I _{CCH}	Power Supply Current			50	μA	Max	All Outputs HIGH
I _{CCL}	Power Supply Current			30	mA	Max	All Outputs LOW
I _{CCZ}	Power Supply Current			50	μA	Max	\overline{OE} = V _{CC} All Others at V _{CC} or GND
I _{CC1}	Additional I _{CC} /Input	Outputs Enabled Outputs TRI-STATE Outputs TRI-STATE		2.5 2.5 2.5	mA mA mA	Max	V _I = V _{CC} − 2.1V Enable Input V _I = V _{CC} − 2.1V Data Input V _I = V _{CC} − 2.1V All Others at V _{CC} or GND
I _{CCD}	Dynamic I _{CC} (Note 2)	No Load		0.12	mA/ MHz	Max	Outputs Open, LE = V _{CC} \overline{OE} = GND, (Note 1) One Bit Toggling, 50% Duty Cycle

Note 1: For 8 bits toggling, I_{CCD} < 0.8 mA/MHz.

Note 2: Guaranteed, but not tested.

DC Electrical Characteristics (SOIC Package) (Continued)

Symbol	Parameter	Min	Typ	Max	Units	V _{CC}	Conditions C _L = 50 pF, R _L = 500Ω
V _{OLP}	Quiet Output Maximum Dynamic V _{OL}		0.4	0.8	V	5.0	T _A = 25°C (Note 1)
V _{OLV}	Quiet Output Minimum Dynamic V _{OL}	-1.2	-0.8		V	5.0	T _A = 25°C (Note 1)
V _{OHV}	Minimum High Level Dynamic Output Voltage	2.5	3.0		V	5.0	T _A = 25°C (Note 3)
V _{IHD}	Minimum High Level Dynamic Input Voltage	2.0	1.7		V	5.0	T _A = 25°C (Note 2)
V _{ILD}	Maximum Low Level Dynamic Input Voltage		0.9	0.6	V	5.0	T _A = 25°C (Note 2)

Note 1: Max number of outputs defined as (n). n - 1 data inputs are driven 0V to 3V. One output at Low. Guaranteed, but not tested.

Note 2: Max number of data inputs (n) switching. n - 1 inputs switching 0V to 3V. Input-under-test switching: 3V to threshold (V_{ILD}), 0V to threshold (V_{IHD}). Guaranteed, but not tested.

Note 3: Max number of outputs defined as (n). n - 1 data inputs are driven 0V to 3V. One output HIGH. Guaranteed, but not tested.

AC Electrical Characteristics

Symbol	Parameter	74ABT			54ABT		74ABT		Units
		T _A = +25°C V _{CC} = +5.0V C _L = 50 pF			T _A = -55°C to +125°C V _{CC} = 4.5V to 5.5V C _L = 50 pF		T _A = -40°C to +85°C V _{CC} = 4.5V to 5.5V C _L = 50 pF		
		Min	Typ	Max	Min	Max	Min	Max	
t _{PLH} t _{PHL}	Propagation Delay D _n to O _n	1.9	2.7	4.5	1.0	6.8	1.9	4.5	ns
t _{PLH} t _{PHL}	Propagation Delay LE to O _n	2.0	3.1	5.0	1.0	7.7	2.0	5.0	ns
t _{PZH} t _{PZL}	Output Enable Time	1.5	3.1	5.3	1.0	6.7	1.5	5.3	ns
t _{PHZ} t _{PLZ}	Output Disable Time	2.0	3.6	5.4	1.7	8.0	2.0	5.4	ns

AC Operating Requirements

Symbol	Parameter	74ABT			54ABT		74ABT		Units
		T _A = +25°C V _{CC} = +5.0V C _L = 50 pF			T _A = -55°C to +125°C V _{CC} = 4.5V to 5.5V C _L = 50 pF		T _A = -40°C to +85°C V _{CC} = 4.5V to 5.5V C _L = 50 pF		
		Min	Typ	Max	Min	Max	Min	Max	
f _{toggle}	Max Toggle Frequency		100		100				MHz
t _s (H) t _s (L)	Setup Time, HIGH or LOW D _n to LE	1.5			2.5		1.5		ns
t _h (H) t _h (L)	Hold Time, HIGH or LOW D _n to LE	1.0			2.5		1.0		ns
t _w (H)	Pulse Width, LE HIGH	3.0			3.3		3.0		ns

Extended AC Electrical Characteristics

(SOIC package)

Symbol	Parameter	74ABT		74ABT		74ABT		Units
		T _A = -40°C to +85°C V _{CC} = 4.5V to 5.5V C _L = 50 pF 8 Outputs Switching (Note 4)		T _A = -40°C to +85°C V _{CC} = 4.5V to 5.5V C _L = 250 pF (Note 5)		T _A = -40°C to +85°C V _{CC} = 4.5V to 5.5V C _L = 250 pF 8 Outputs Switching (Note 6)		
		Min	Max	Min	Max	Min	Max	
t _{PLH}	Propagation Delay	1.5	5.2	2.0	6.8	2.0	9.0	ns
t _{PHL}	D _n to O _n	1.5	5.2	2.0	6.8	2.0	9.0	
t _{PLH}	Propagation Delay	1.5	5.5	2.0	7.5	2.0	9.5	ns
t _{PHL}	LE to O _n	1.5	5.5	2.0	7.5	2.0	9.5	
t _{PZH}	Output Enable Time	1.5	6.2	2.0	8.0	2.0	10.5	ns
t _{PZL}		1.5	6.2	2.0	8.0	2.0	10.5	
t _{PHZ}	Output Disable Time	1.0	5.5	(Note 7)		(Note 7)		ns
t _{PZL}		1.0	5.5	(Note 7)		(Note 7)		

Note 4: This specification is guaranteed but not tested. The limits apply to propagation delays for all paths described switching in phase (i.e., all LOW-to-HIGH, HIGH-to-LOW, etc.).

Note 5: This specification is guaranteed but not tested. The limits represent propagation delay with 250 pF load capacitors in place of the 50 pF load capacitors in the standard AC load. This specification pertains to single output switching only.

Note 6: This specification is guaranteed but not tested. The limits represent propagation delays for all paths described switching in phase (i.e., all LOW-to-HIGH, HIGH-to-LOW, etc.) with 250 pF load capacitors in place of the 50 pF load capacitors in the standard AC load.

Note 7: The TRI-STATE delay times are dominated by the RC network (500Ω, 250 pF) on the output and has been excluded from the datasheet.

Skew

Symbol	Parameter	74ABT		74ABT		Units
		T _A = -40°C to +85°C V _{CC} = 4.5V-5.5V C _L = 50 pF 8 Outputs Switching (Note 3)		T _A = -40°C to +85°C V _{CC} = 4.5V-5.5V C _L = 250 pF 8 Outputs Switching (Note 4)		
		Max		Max		
t _{OSHL} (Note 1)	Pin to Pin Skew HL Transitions	1.0		1.5		ns
t _{OSLH} (Note 1)	Pin to Pin Skew LH Transitions	1.0		1.5		ns
t _{PS} (Note 5)	Duty Cycle LH-HL Skew	1.4		3.5		ns
t _{OST} (Note 1)	Pin to Pin Skew LH/HL Transitions	1.5		3.9		ns
t _{PV} (Note 2)	Device to Device Skew LH/HL Transitions	2.0		4.0		ns

Note 1: Skew is defined as the absolute value of the difference between the actual propagation delays for any two separate outputs of the same device. The specification applies to any outputs switching HIGH to LOW (t_{OSHL}), LOW to HIGH (t_{OSLH}), or any combination switching LOW to HIGH and/or HIGH to LOW (t_{OST}). This specification is guaranteed but not tested.

Note 2: Propagation delay variation for a given set of conditions (i.e., temperature and V_{CC}) from device to device. This specification is guaranteed but not tested.

Note 3: This specification is guaranteed but not tested. The limits apply to propagation delays for all paths described switching in phase (i.e., all LOW-to-HIGH, HIGH-to-LOW, etc.).

Note 4: This specification is guaranteed but not tested. The limits represent propagation delays with 250 pF load capacitors in place of the 50 pF load capacitors in the standard AC load.

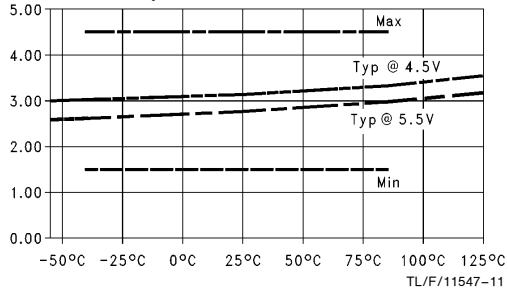
Note 5: This describes the difference between the delay of the LOW-to-HIGH and the HIGH-to-LOW transition on the same pin. It is measured across all the outputs (drivers) on the same chip, the worst (largest delta) number is the guaranteed specification. This specification is guaranteed but not tested.

Capacitance

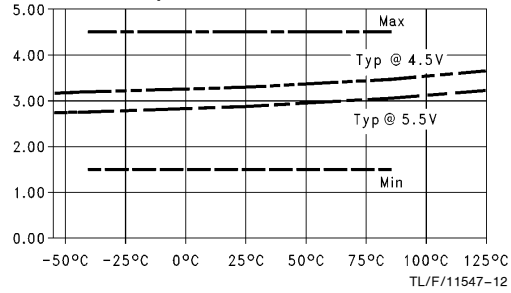
Symbol	Parameter	Typ	Units	Conditions ($T_A = 25^\circ\text{C}$)
C_{IN}	Input Capacitance	5	pF	$V_{CC} = 0\text{V}$
C_{OUT} (Note 1)	Output Capacitance	9	pF	$V_{CC} = 5.0\text{V}$

Note 1: C_{OUT} is measured at frequency $f = 1\text{ MHz}$, per MIL-STD-883B, Method 3012.

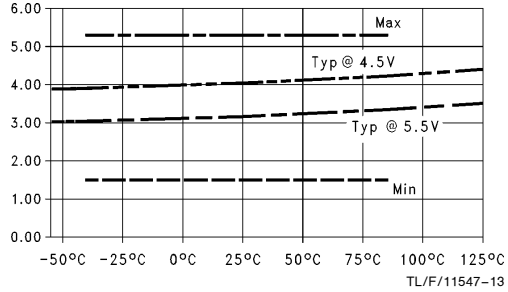
t_{PLH} vs Temperature (T_A)
 $C_L = 50\text{ pF}$, 1 Output Switching
 Data to Output



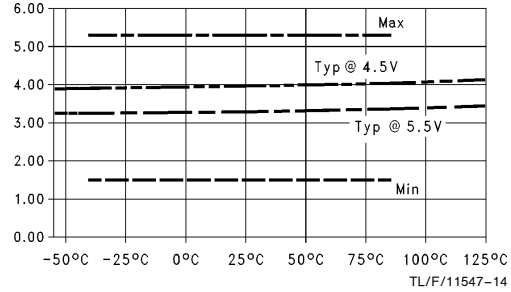
t_{PHL} vs Temperature (T_A)
 $C_L = 50\text{ pF}$, 1 Output Switching
 Data to Output



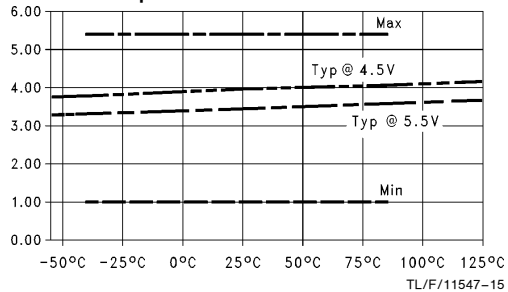
t_{pZH} vs Temperature (T_A)
 $C_L = 50\text{ pF}$, 1 Output Switching
 \overline{OE} to Output



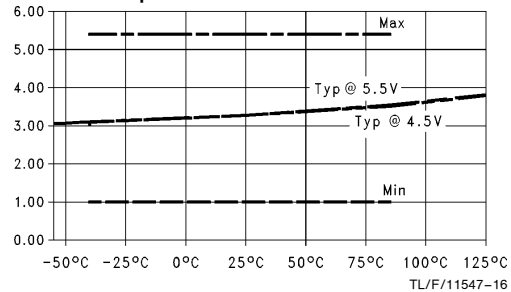
t_{pZL} vs Temperature (T_A)
 $C_L = 50\text{ pF}$, 1 Output Switching
 \overline{OE} to Output



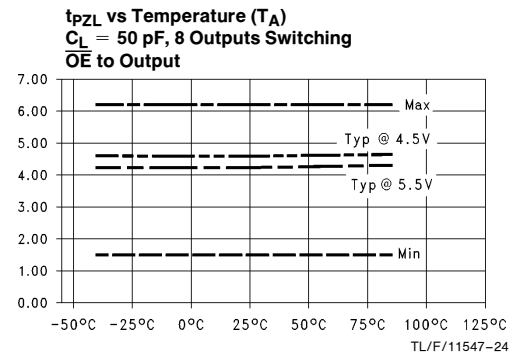
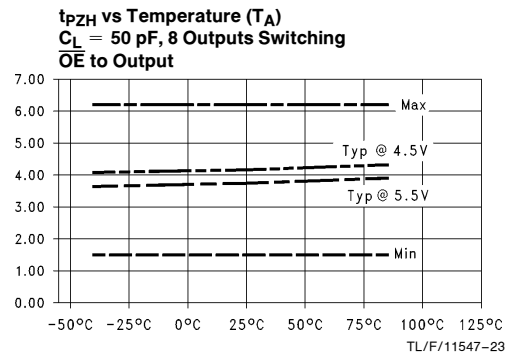
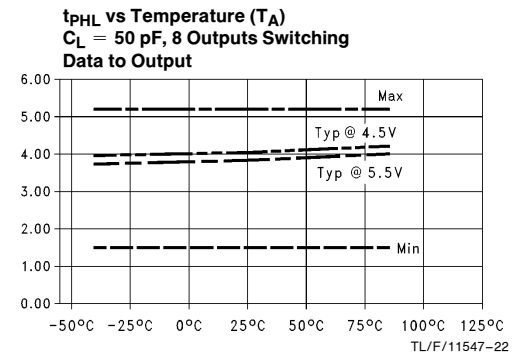
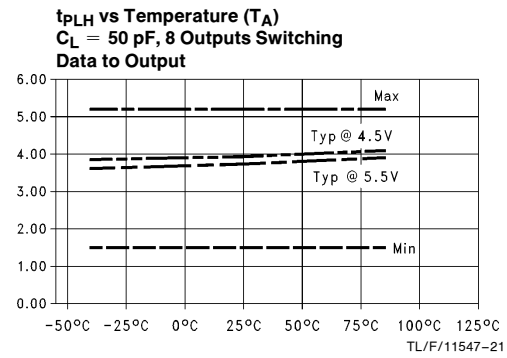
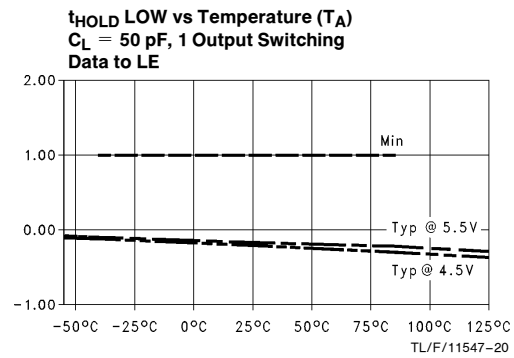
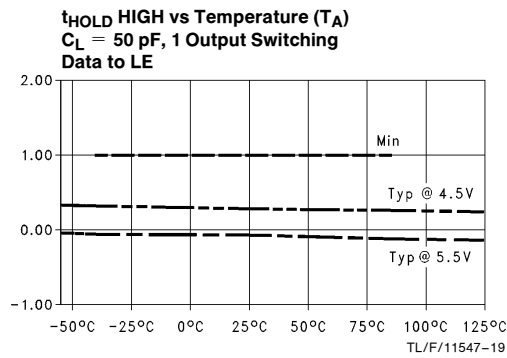
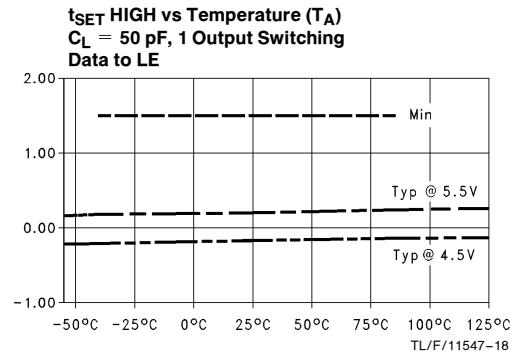
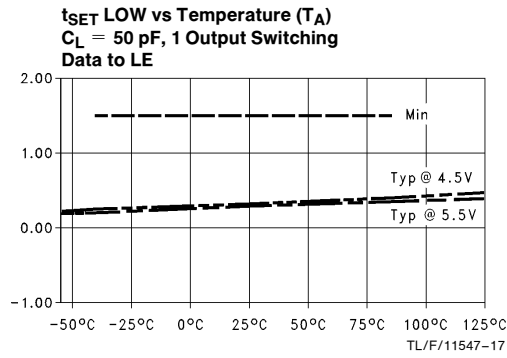
t_{pHZ} vs Temperature (T_A)
 $C_L = 50\text{ pF}$, 1 Output Switching
 \overline{OE} to Output



t_{pLZ} vs Temperature (T_A)
 $C_L = 50\text{ pF}$, 1 Output Switching
 \overline{OE} to Output

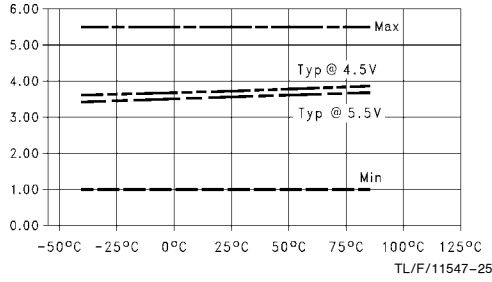


Dashed lines represent design characteristics; for specified guarantees, refer to AC Characteristics Tables.

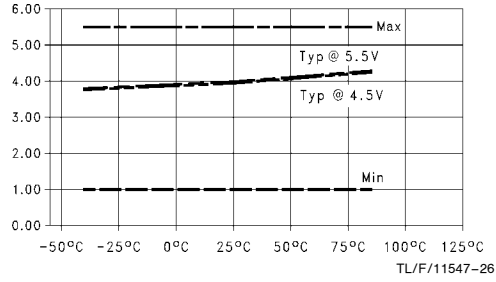


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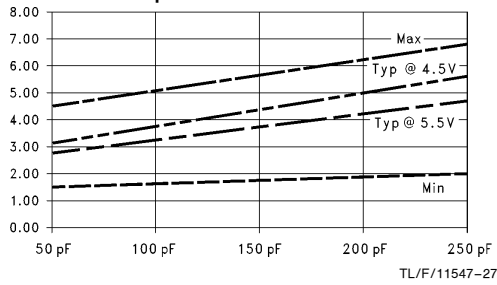
tpHZ vs Temperature (TA)
CL = 50 pF, 8 Outputs Switching
OE to Output



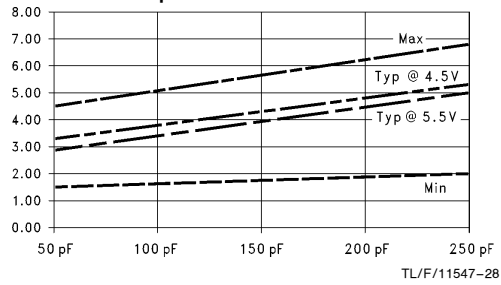
tpLZ vs Temperature (TA)
CL = 50 pF, 8 Outputs Switching
OE to Output



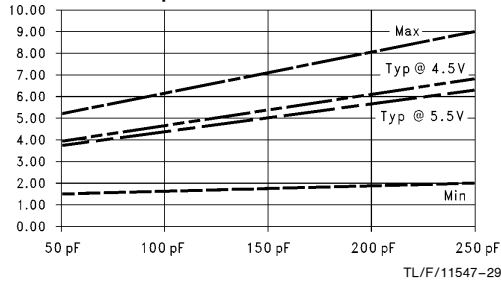
tpLH vs Load Capacitance
TA = 25°C, 1 Output Switching
Data to Output



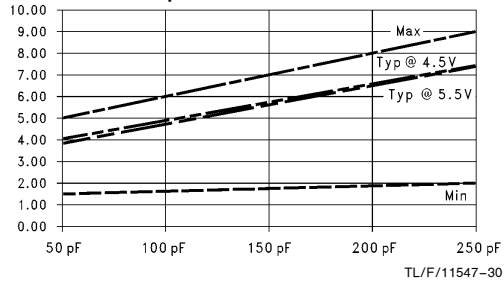
tpHL vs Load Capacitance
TA = 25°C, 1 Output Switching
Data to Output



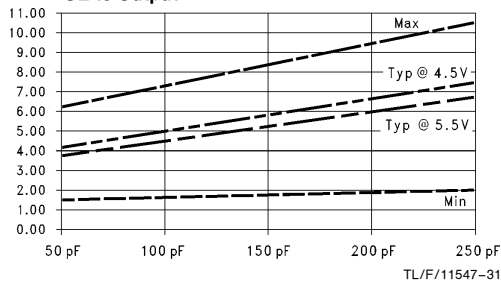
tpLH vs Load Capacitance
TA = 25°C, 8 Outputs Switching
Data to Output



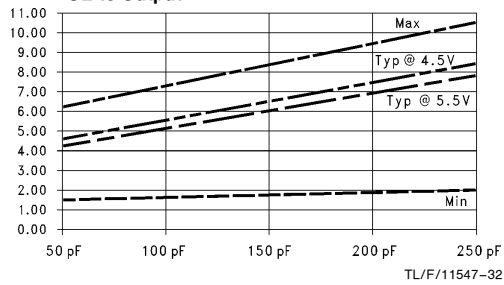
tpHL vs Load Capacitance
TA = 25°C, 8 Outputs Switching
Data to Output



tpZH vs Load Capacitance
TA = 25°C, 8 Outputs Switching
OE to Output

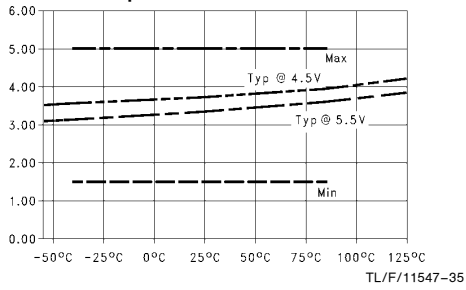


tpZL vs Load Capacitance
TA = 25°C, 8 Outputs Switching
OE to Output

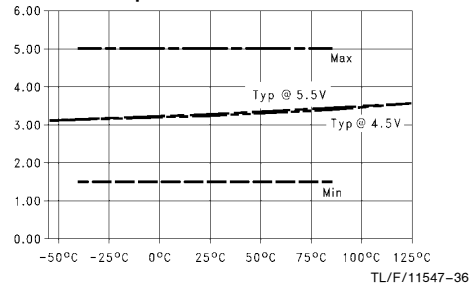


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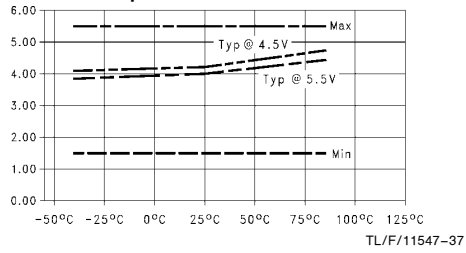
t_{PLH} vs Temperature (T_A)
 $C_L = 50$ pF, 1 Output Switching
 LE to Output



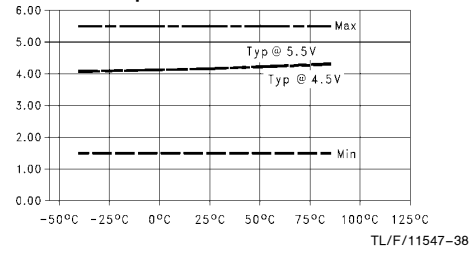
t_{PHL} vs Temperature (T_A)
 $C_L = 50$ pF, 1 Output Switching
 LE to Output



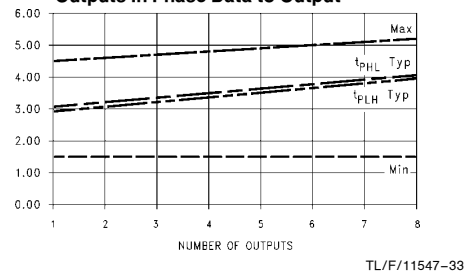
t_{PLH} vs Temperature (T_A)
 $C_L = 50$ pF, 8 Outputs Switching
 LE to Output



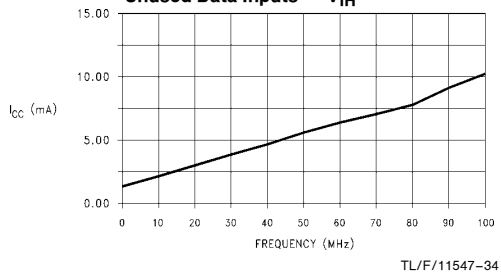
t_{PHL} vs Temperature (T_A)
 $C_L = 50$ pF, 8 Outputs Switching
 LE to Output



t_{PLH} and t_{PHL} vs Number Outputs Switching
 $C_L = 50$ pF, $T_A = 25^\circ\text{C}$, $V_{CC} = 5.0\text{V}$,
 Outputs In Phase Data to Output

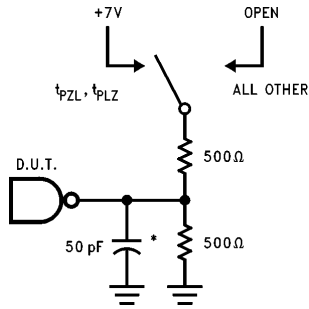


Typical I_{CC} vs Output Switching Frequency
 $C_L = 0$ pF, $V_{CC} = V_{IH} = 5.5\text{V}$, $LE = \text{GND}$,
 1 Output Switching at 50% Duty Cycle
 Data to Output, Transparent Mode with
 Unused Data Inputs = V_{IH}



Dashed lines represent design characteristics; for specified guarantees, refer to AC Characteristics Tables.

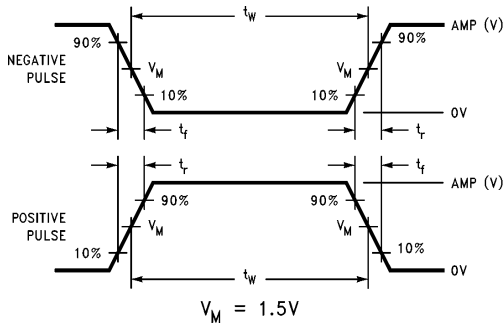
AC Loading



*Includes jig and probe capacitance

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FIGURE 1. Standard AC Test Load

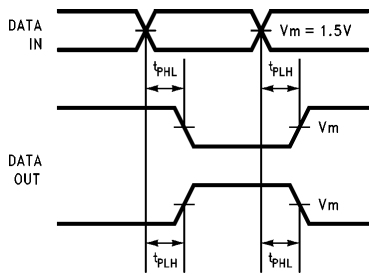


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FIGURE 2a. Test Input Signal Levels

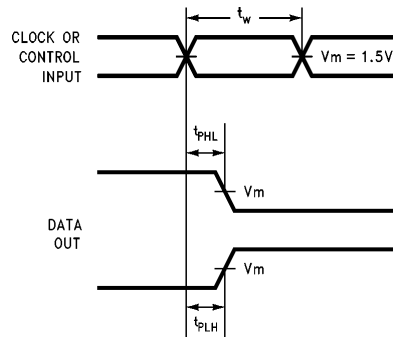
Amplitude	Rep. Rate	t_w	t_r	t_f
3.0V	1 MHz	500 ns	2.5 ns	2.5 ns

FIGURE 2b. Test Input Signal Requirements



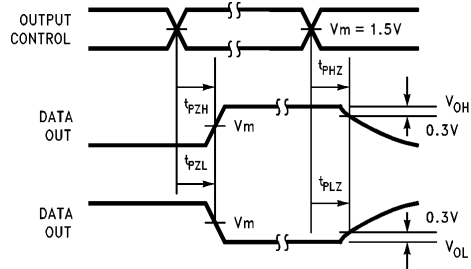
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FIGURE 3. Propagation Delay Waveforms for Inverting and Non-Inverting Functions



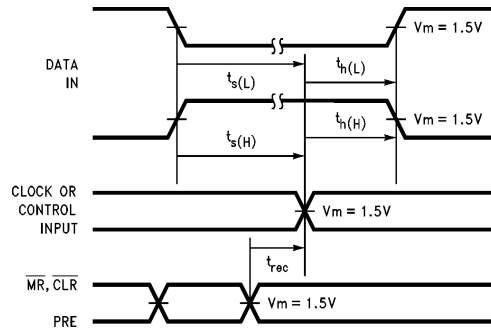
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FIGURE 4. Propagation Delay, Pulse Width Waveforms



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FIGURE 5. TRI-STATE Output HIGH and LOW Enable and Disable Times

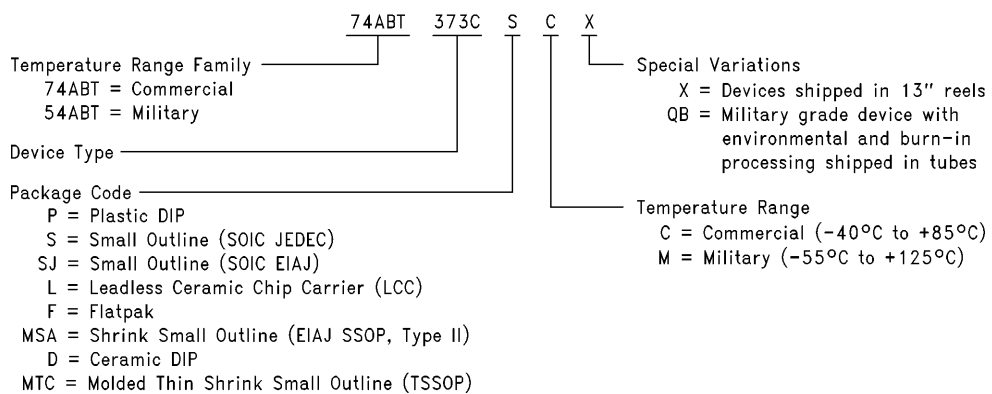


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FIGURE 6. Setup Time, Hold Time and Recovery Time Waveforms

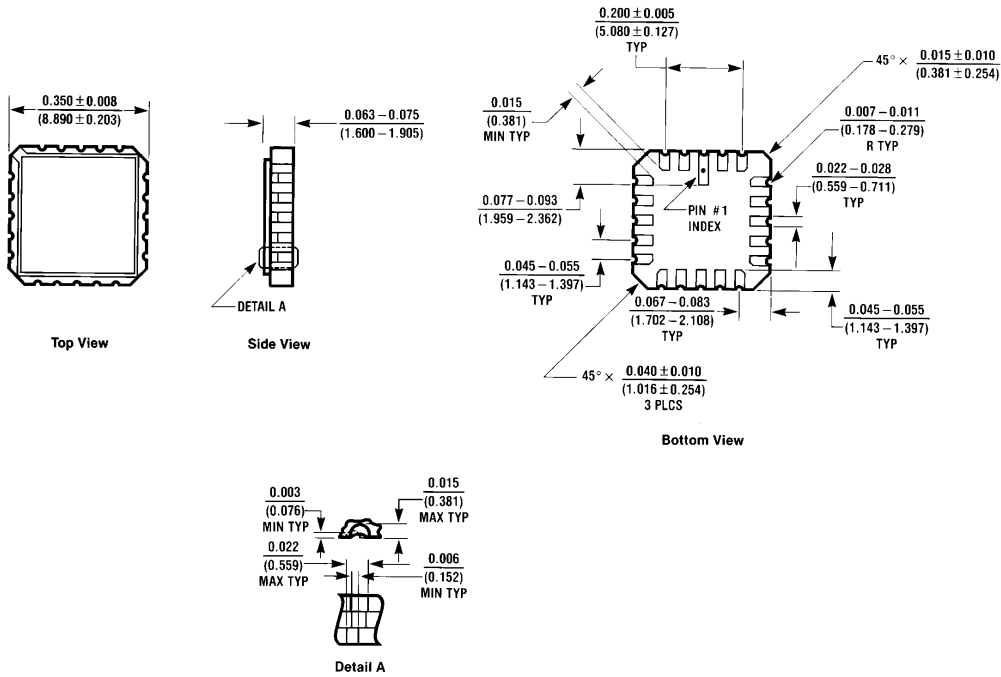
Ordering Information

The device number is used to form part of a simplified purchasing code where the package type and temperature range are defined as follows:



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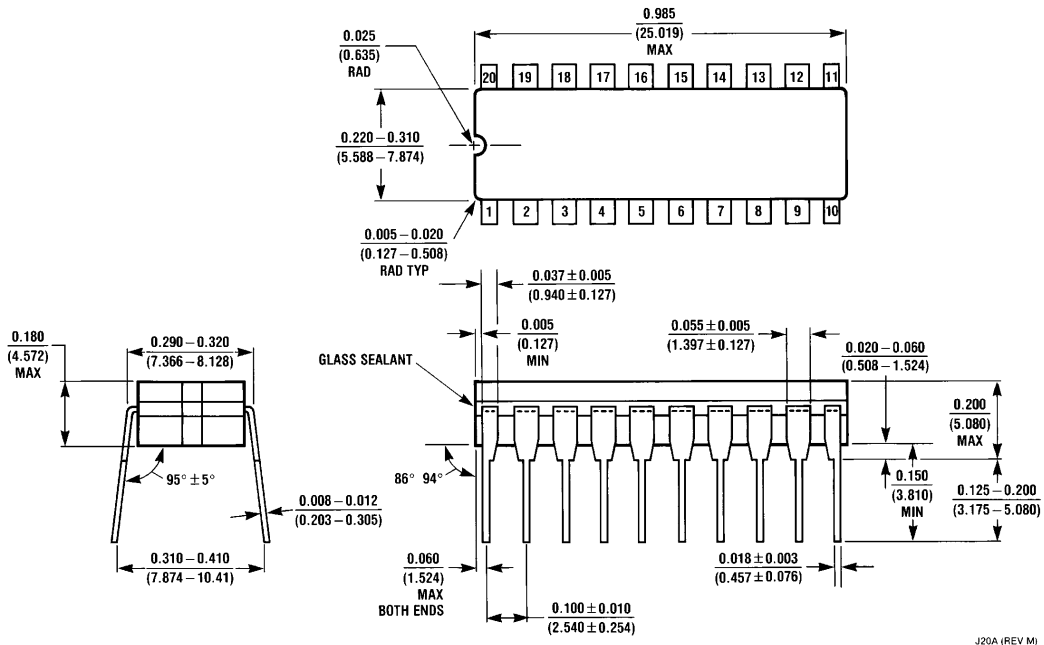
Physical Dimensions inches (millimeters)



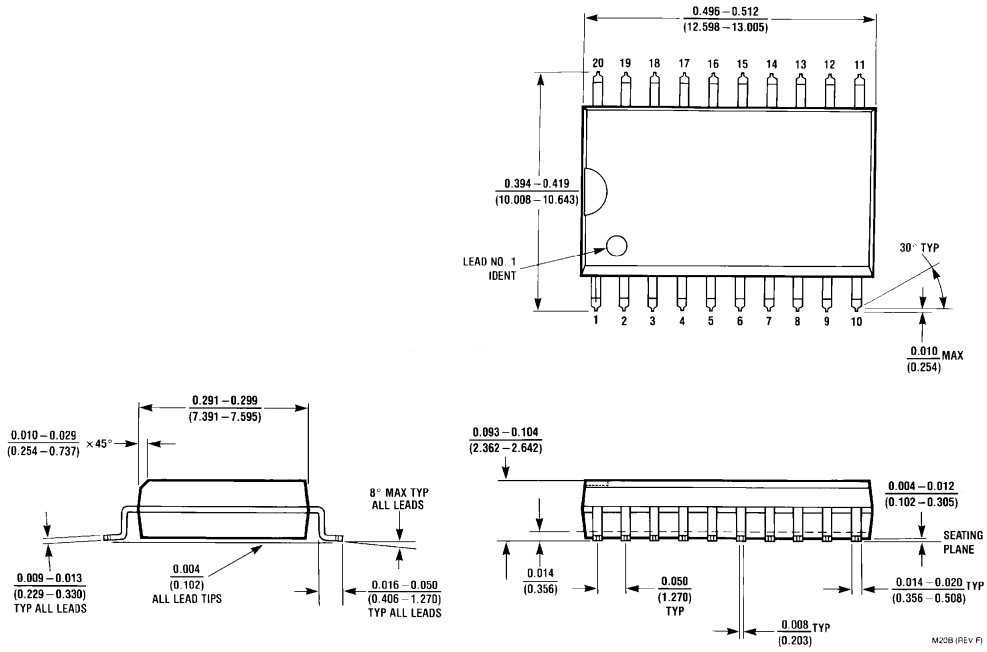
E20A (REV D)

**20-Terminal Ceramic Chip Carrier (L)
 NS Package Number E20A**

Physical Dimensions inches (millimeters) (Continued)

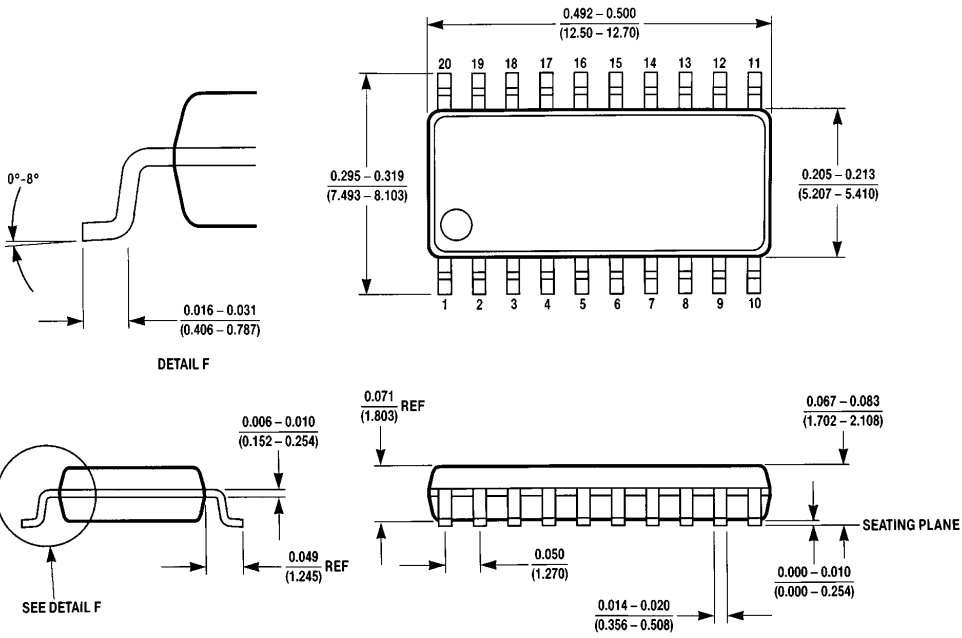


20-Lead Ceramic Dual-In-Line (D)
NS Package Number J20A

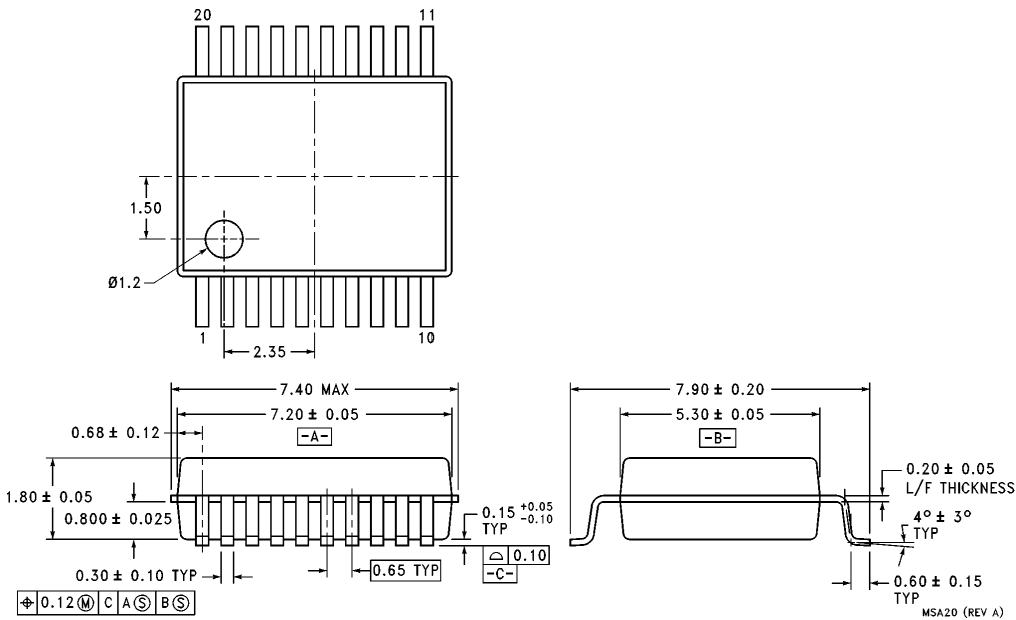


20-Lead Small Outline Integrated Circuit JEDEC (S)
NS Package Number M20B

Physical Dimensions inches (millimeters) (Continued)

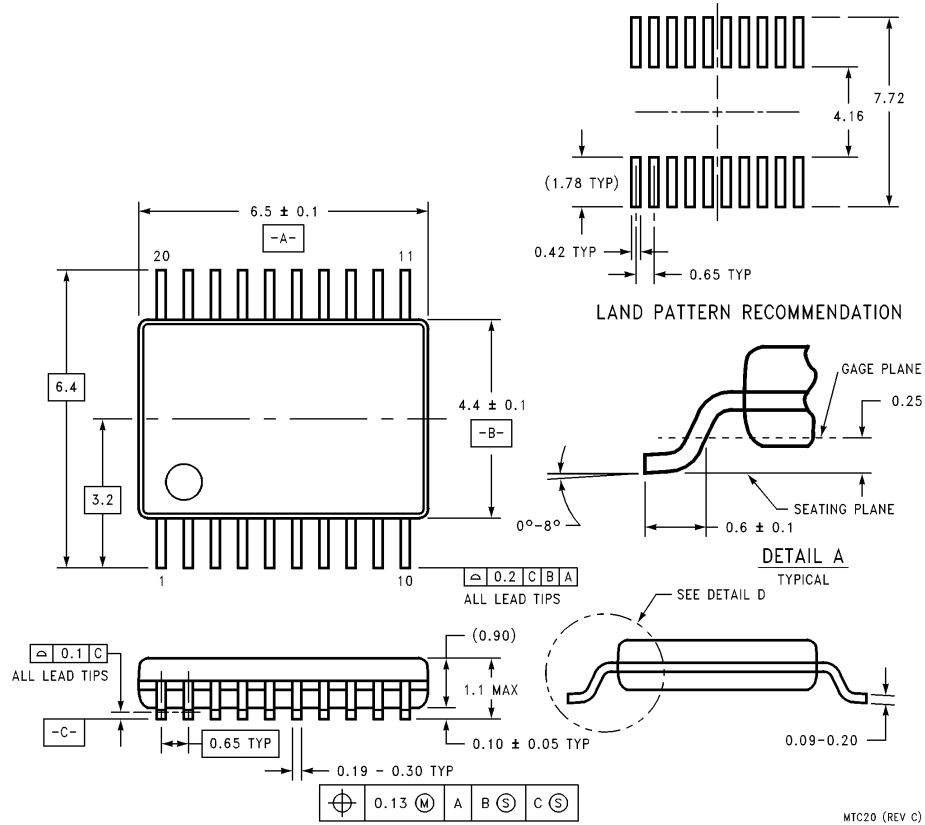


**20-Lead Small Outline Integrated Circuit EIAJ (SJ)
NS Package Number M20D**



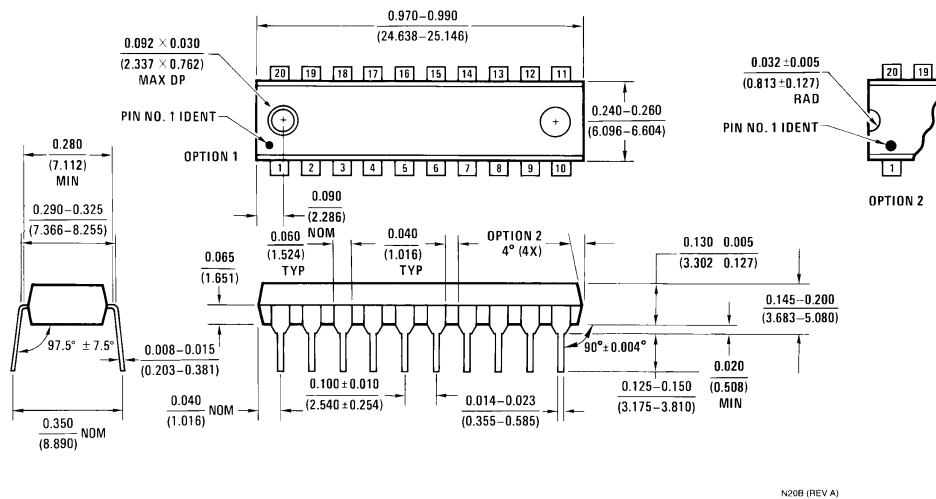
**20-Lead Plastic EIAJ SSOP (MSA)
NS Package Number MSA20**

Physical Dimensions inches (millimeters) (Continued)



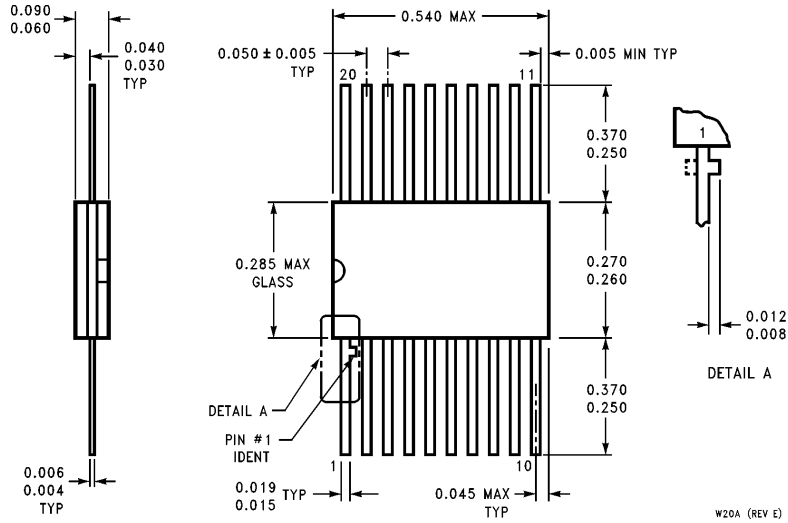
All dimensions are in millimeters.

20-Lead Molded Thin Shrink Small Outline Package JEDEC (MTC)
NS Package Number MTC20



20-Lead Plastic Dual-In-Line Package (P)
NS Package Number N20B

Physical Dimensions inches (millimeters) (Continued)



**20-Lead Ceramic Flatpak (F)
NS Package Number W20A**

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