# 1:4 Clock Driver for Intel PCIe® Chipsets

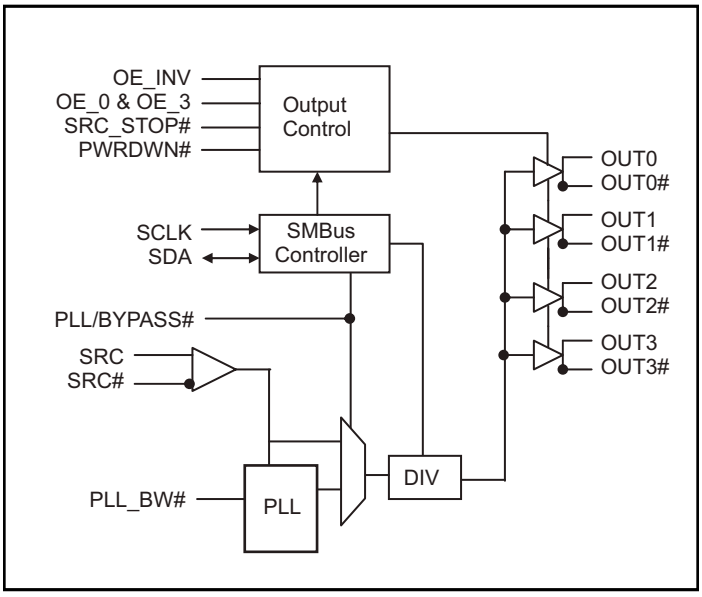
## Features

- Phase jitter filter for PCIe® 2.0 application
- Four Pairs of Differential Clocks
- Low skew < 50ps
- Low jitter < 50ps cycle-to-cycle
- < 1 ps additive RMS phase jitter
- Output Enable for all outputs
- Outputs tristate control via SMBus
- Programmable PLL Bandwidth
- 100 MHz PLL Mode operation
- 100 - 400 MHz Bypass Mode operation
- 3.3V Operation
- Packaging (Pb-free and Green):
  →28-Pin SSOP (H28)
  →28-Pin TSSOP (L28)

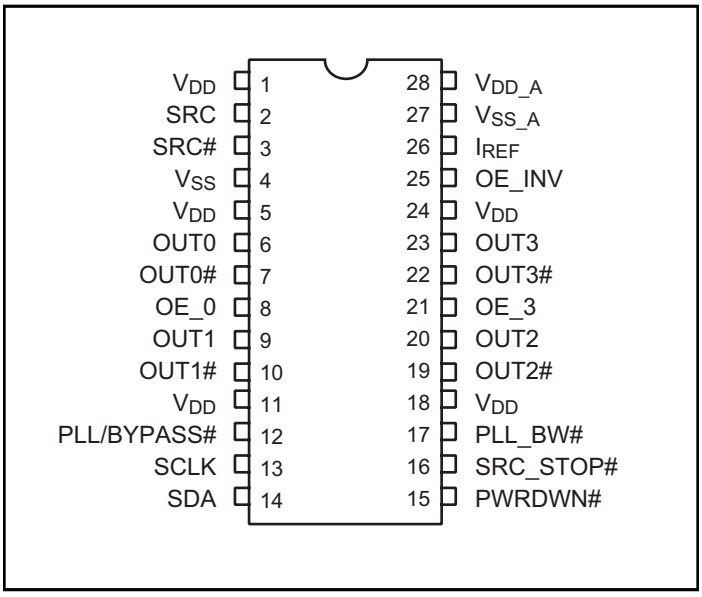
## Description

Pericom Semiconductor's PI6C20400A is a PCIe® 2.0 compliant high-speed, low-noise differential clock buffer designed to be companion to PI6C410BS. The device distributes the differential SRC clock from PI6C410BS to four differential pairs of clock outputs either with or without PLL. The clock outputs are controlled by input selection of SRC_STOP#, PWRDWN# and SMBus, SCLK and SDA. When input of either SRC_STOP# or PWRDWN# is low, the output clocks are Tristated. When PWRDWN# is low, the SDA and SCLK inputs must be Tri-stated.

## Block Diagram




## Pin Configuration



## Pin Descriptions

| Pin Name | Type | Pin No | Description |
|---|---|---|---|
| SRC & SRC# | Input | 2, 3 | 0.7V Differential SRC input from PI6C410 clock synthesizer |
| OE_0 & OE_3 | Input | 8, 21 | 3.3V LVTTL input for enabling outputs, active high.<br>OE_0 for OUT0 / OUT0#<br>OE_3 for OUT3 / OUT3# |
| OE_INV | Input | 25 | 3.3V LVTTL input for inverting the OE, SRC_STOP# and PWRDWN# pins.<br>When 0 = same stage<br>When 1 = OE_0, OE_3, SRC_STOP#, PWRDWN# inverted. |
| OUT[0:3] & OUT[0:3]# | Output | 6, 7, 9, 10, 19, 20, 22, 23 | 0.7V Differential outputs |
| PLL/BYPASS# | Input | 12 | 3.3V LVTTL input for selecting fan-out of PLL operation. |
| SCLK | Input | 13 | SMBus compatible SCLOCK input |
| SDA | I/O | 14 | SMBus compatible SDATA |
| IREF | Input | 26 | External resistor connection to set the differential output current |
| SRC_STOP# | Input | 16 | 3.3V LVTTL input for SRC stop, active low |
| PLL_BW# | Input | 17 | 3.3V LVTTL input for selecting the PLL bandwidth |
| PWRDWN# | Input | 15 | 3.3V LVTTL input for Power Down operation, active low |
| $V_{DD}$ | Power | 1, 5, 11, 18, 24 | 3.3V Power Supply for Outputs |
| VSS | Ground | 4 | Ground for Outputs |
| VSS_A | Ground | 27 | Ground for PLL |
| VDD_A | Power | 28 | 3.3V Power Supply for PLL |

## Serial Data Interface (SMBus)

This part is a slave only SMBus device that supports indexed block read and indexed block write protocol using a single 7-bit address and read/write bit as shown below.

## Address Assignment

| A6 | A5 | A4 | A3 | A2 | A1 | A0 | W/R |
|---|---|---|---|---|---|---|---|
| 1 | 1 | 0 | 1 | 1 | 1 | 0 | 0/1 |

## Data Protocol

| 1 bit | 7 bits | 1 | 1 | 8 bits | 1 | 8 bits | 1 | 8 bits | 1 | | 8 bits | 1 | 1 bit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Start bit | Slave Addr | R/W | Ack | Register offset | Ack | Byte Count = N | Ack | Data Byte 0 | Ack | … | Data Byte N - 1 | Ack | Stop bit |

**Notes:**

1. Register offset for indicating the starting register for indexed block write and indexed block read. Byte Count in write mode cannot be 0.

## Data Byte 0: Control Register

| Bit | Descriptions | Type | Power Up Condition | Output(s) Affected | Source Pin |
|---|---|---|---|---|---|
| 0 | Outputs Mode<br>0 = Divide by 2<br>1 = Normal | RW | 1 = Normal | OUT[0:3], OUT[0:3]# | NA |
| 1 | PLL/BYPASS#<br>0 = Fanout<br>1 = PLL | RW | 1 = PLL | OUT[0:3], OUT[0:3]# | NA |
| 2 | PLL Bandwidth<br>0 = High Bandwidth,<br>1 = Low Bandwidth | RW | 1 = Low | OUT[0:3], OUT[0:3]# | NA |
| 3 | Reserved | | | | NA |
| 4 | Reserved | | | | NA |
| 5 | Reserved | | | | NA |
| 6 | SRC_STOP#<br>0 = Driven when stopped<br>1 = Tristate | RW | 0 = Driven when stopped | OUT[0:3], OUT[0:3]# | NA |
| 7 | PWRDWN#<br>0 = Driven when stopped<br>1 = Tristate | RW | 0 = Driven when stopped | OUT[0:3], OUT[0:3]# | NA |

## Data Byte 1: Control Register

| Bit | Descriptions | Type | Power Up Condition | Output(s) Affected | Source Pin |
|---|---|---|---|---|---|
| 0 | Reserved | | | | NA |
| 1 | OUTPUTS enable<br>1 = Enabled<br>0 = Disabled | RW | 1 = Enabled | OUT0, OUT0# | NA |
| 2 | | RW | 1 = Enabled | OUT1, OUT1# | NA |
| 3 | Reserved | | | | NA |
| 4 | Reserved | | | | NA |
| 5 | OUTPUTS enable<br>1 = Enabled<br>0 = Disabled | RW | 1 = Enabled | OUT2, OUT2# | NA |
| 6 | | RW | 1 = Enabled | OUT3, OUT3# | NA |
| 7 | Reserved | | | | NA |

## Data Byte 2: Control Register

| Bit | Descriptions | Type | Power Up Condition | Output(s) Affected | Source Pin |
|---|---|---|---|---|---|
| 0 | Reserved | | | | NA |
| 1 | Allow control of OUTPUTS with assertion of SRC_STOP#<br>0 = Free running<br>1 = Stopped with SRC_Stop# | RW | 0 = Free running | OUT0, OUT0# | NA |
| 2 | | RW | 0 = Free running | OUT1, OUT1# | NA |
| 3 | Reserved | | | | NA |
| 4 | Reserved | | | | NA |
| 5 | Allow control of OUTPUTS with assertion of SRC_STOP#<br>0 = Free running<br>1 = Stopped with SRC_Stop# | RW | 0 = Free running | OUT2, OUT2# | NA |
| 6 | | RW | 0 = Free running | OUT3, OUT3# | NA |
| 7 | Reserved | | | | NA |

## Data Byte 3: Control Register

| Bit | Descriptions | Type | Power Up Condition | Output(s) Affected | Source Pin |
|---|---|---|---|---|---|
| 0 | Reserved | RW | | | |
| 1 | | RW | | | |
| 2 | | RW | | | |
| 3 | | RW | | | |
| 4 | | RW | | | |
| 5 | | RW | | | |
| 6 | | RW | | | |
| 7 | | RW | | | |

## Data Byte 4: Pericom ID Register

| Bit | Descriptions | Type | Power Up Condition | Output(s) Affected | Pin |
|---|---|---|---|---|---|
| 0 | Pericom ID | R | 0 | NA | NA |
| 1 | | R | 0 | NA | NA |
| 2 | | R | 0 | NA | NA |
| 3 | | R | 0 | NA | NA |
| 4 | | R | 0 | NA | NA |
| 5 | | R | 1 | NA | NA |
| 6 | | R | 0 | NA | NA |
| 7 | | R | 0 | NA | NA |

## Functionality

| PWRDWN# | OUT | OUT# | SRC_Stop# | OUT | OUT# |
|---|---|---|---|---|---|
| 1 | Normal | Normal | 1 | Normal | Normal |
| 0 | $I_{REF}$ × 2 or Float | Low | 0 | $I_{REF}$ × 6 or Float | Low |

## Power Down (PWRDWN# assertion)

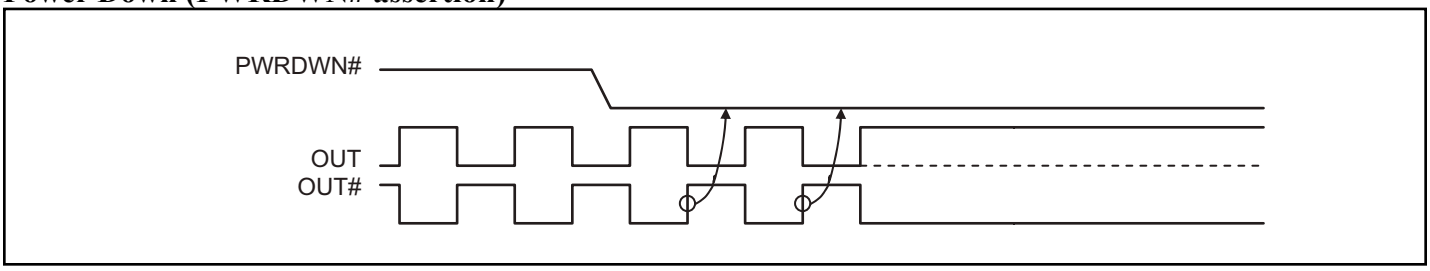



**Figure 1. Power down sequence**

## Power Down (PWRDWN# De-assertion)

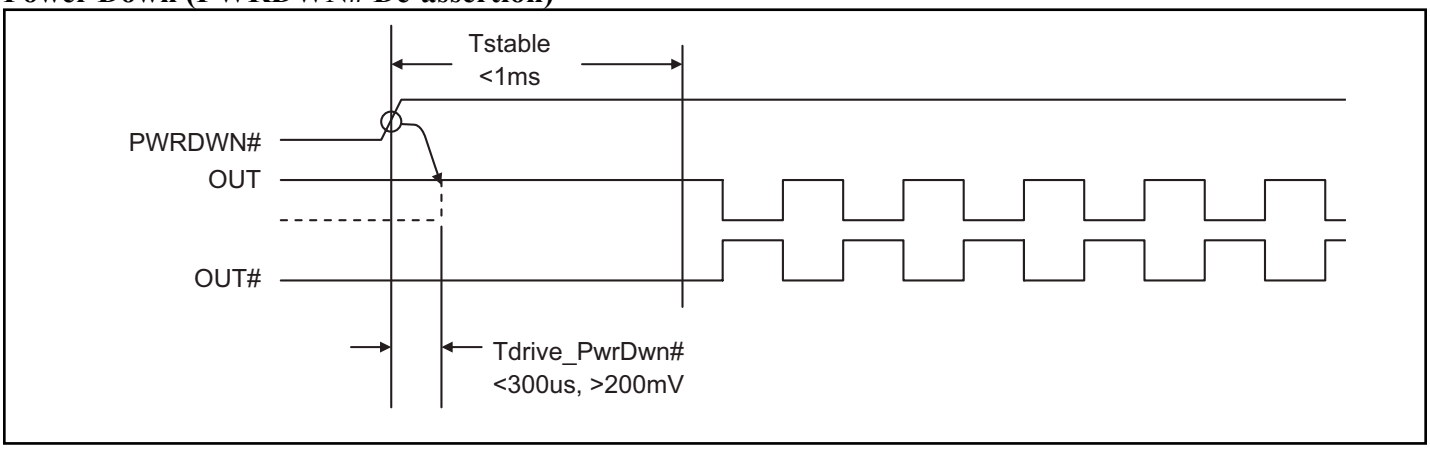



**Figure 2. Power down de-assert sequence**

## Current-mode output buffer characteristics of OUT[0:3], OUT[0:3]#

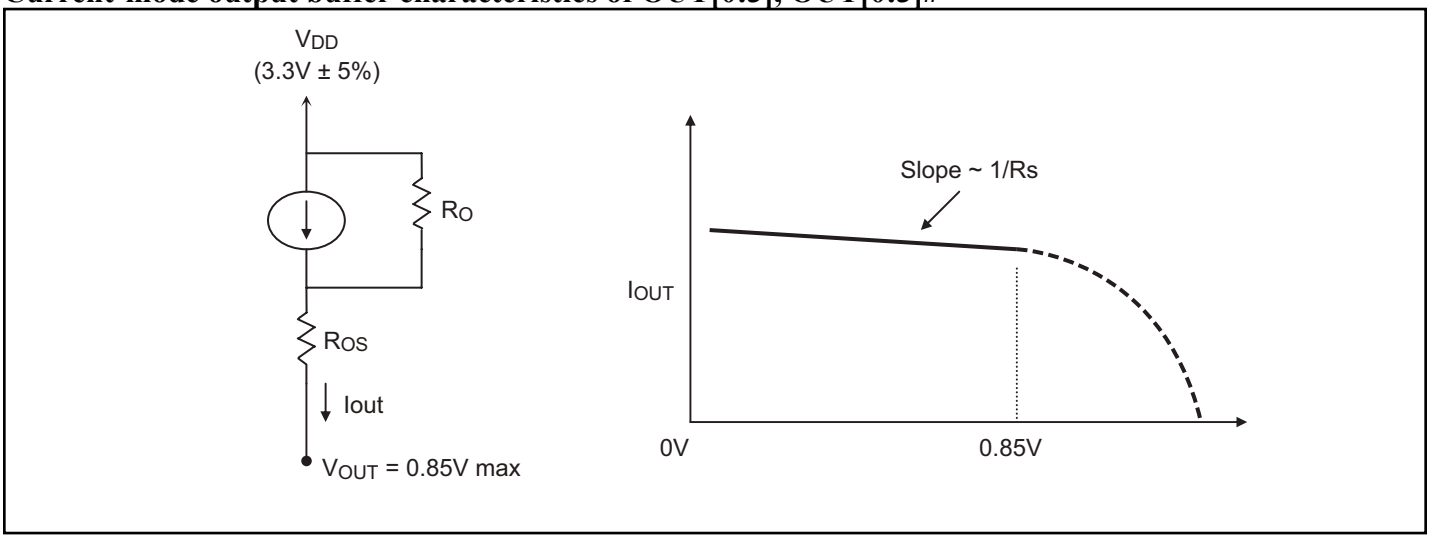



**Figure 9. Simplified diagram of current-mode output buffer**

## Differential Clock Buffer characteristics

| Symbol | Minimum | Maximum |
|---|---|---|
| $R_O$ | 3000Ω | N/A |
| $R_{OS}$ | unspecified | unspecified |
| $V_{OUT}$ | N/A | 850mV |

## Current Accuracy

| Symbol | Conditions | Configuration | Load | Min. | Max. |
|---|---|---|---|---|---|
| $I_{OUT}$ | $V_{DD}$ = 3.30 ±5% | $R_{REF}$ = 475Ω 1%<br>$I_{REF}$ = 2.32mA | Nominal test load for given configuration | -12%<br>$I_{NOMINAL}$ | +12%<br>$I_{NOMINAL}$ |

**Note:**
1. $I_{NOMINAL}$ refers to the expected current based on the configuration of the device.

## Differential Clock Output Current

| Board Target Trace/Term Z | Reference R, Iref = $V_{DD}$/(3xRr) | Output Current | $V_{OH}$ @ Z |
|---|---|---|---|
| 100Ω<br>(100Ω differential ≈ 15% coupling ratio) | $R_{REF}$ = 475Ω 1%,<br>$I_{REF}$ = 2.32mA | $I_{OH}$ = 6 x $I_{REF}$ | 0.7V @ 50 |

## Absolute Maximum Ratings (Over operating free-air temperature range)

| Symbol | Parameters | Min. | Max. | Units |
|---|---|---|---|---|
| $V_{DD_A}$ | 3.3V Core Supply Voltage | -0.5 | 4.6 | V |
| $V_{DD}$ | 3.3V I/O Supply Voltage | -0.5 | 4.6 | |
| $V_{IH}$ | Input High Voltage | | 4.6 | |
| $V_{IL}$ | Input Low Voltage | -0.5 | | |
| Ts | Storage Temperature | -65 | 150 | °C |
| $V_{ESD}$ | ESD Protection | 2000 | | V |

**Note:**
1. Stress beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.

## DC Electrical Characteristics ($V_{DD}$ = 3.3±5%, $V_{DD_A}$ = 3.3±5%)

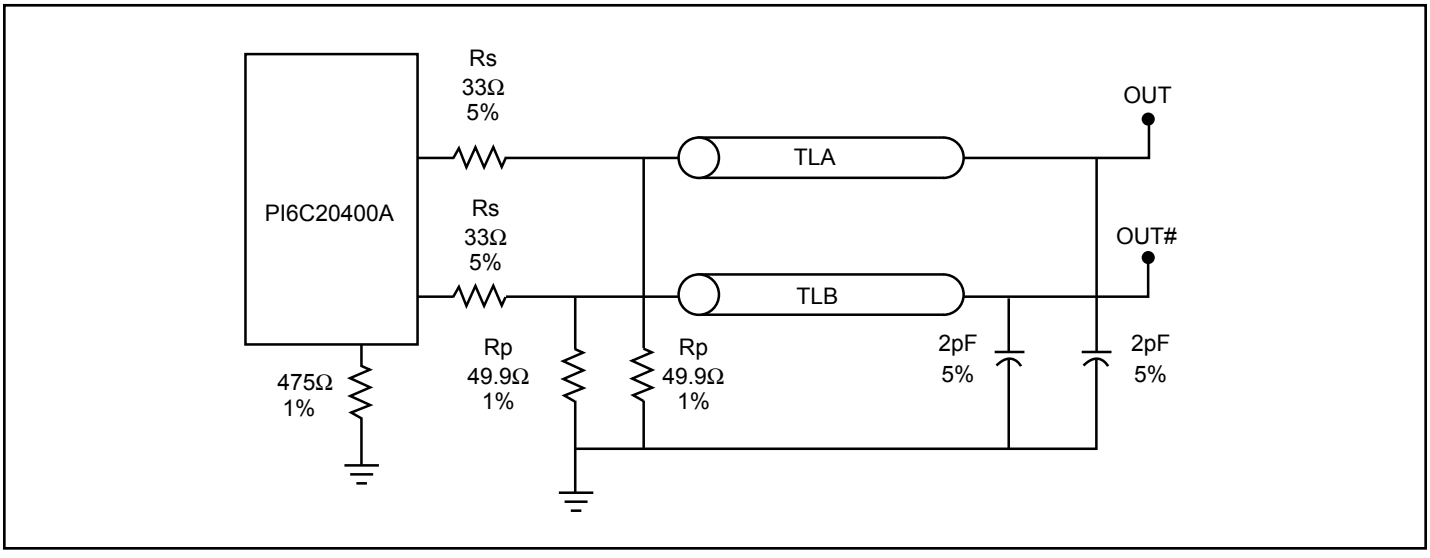
| Symbol | Parameters | Condition | Min. | Max. | Units |
|---|---|---|---|---|---|
| $V_{DD_A}$ | 3.3V Core Supply Voltage | | 3.135 | 3.465 | V |
| $V_{DD}$ | 3.3V I/O Supply Voltage | | 3.135 | 3.465 | |
| $V_{IH}$ | 3.3V Input High Voltage | $V_{DD}$ | 2.0 | $V_{DD}$ + 0.3 | |
| $V_{IL}$ | 3.3V Input Low Voltage | | $V_{SS}$ – 0.3 | 0.8 | |
| $I_{IL}$ | Input Leakage Current | $0 < V_{IN} < V_{DD}$ | -5 | +5 | µA |
| $V_{OH}$ | 3.3V Output High Voltage | $I_{OH}$ = -1mA | 2.4 | | V |
| $V_{OL}$ | 3.3V Output Low Voltage | $I_{OL}$ = 1mA | | 0.4 | |
| $I_{OH}$ | Output High Current | $I_{OH} = 6 \times I_{REF}$, $I_{REF}$ = 2.32mA | 12.2 | | mA |
| | | | | 15.6 | |
| $C_{IN}$ | Input Pin Capacitance | | 2 | 5 | pF |
| $C_{OUT}$ | Output Pin Capacitance | | | 6 | |
| $L_{PIN}$ | Pin Inductance | | | 7 | nH |
| $I_{DD(BYPASS)}$ | Power Supply Current (PLL Bypass) | $V_{DD}$ = 3.465V, $F_{CPU}$ = 100MHz | | 90 | mA |
| $I_{DD}$ | Power Supply Current | $V_{DD}$ = 3.465V | Bypass mode | 100 | |
| | | $F_{CPU}$ = 100MHz | PLL mode | 130 | |
| $I_{SS}$ | Power Down Current | Driven outputs | | 40 | |
| $I_{SS}$ | Power Down Current | Tristate outputs | | 12 | |
| $T_A$ | Ambient Temperature | | -40 | 85 | °C |

## AC Switching Characteristics ($V_{DD}$ = 3.3±5%, $V_{DD_A}$ = 3.3±5%)

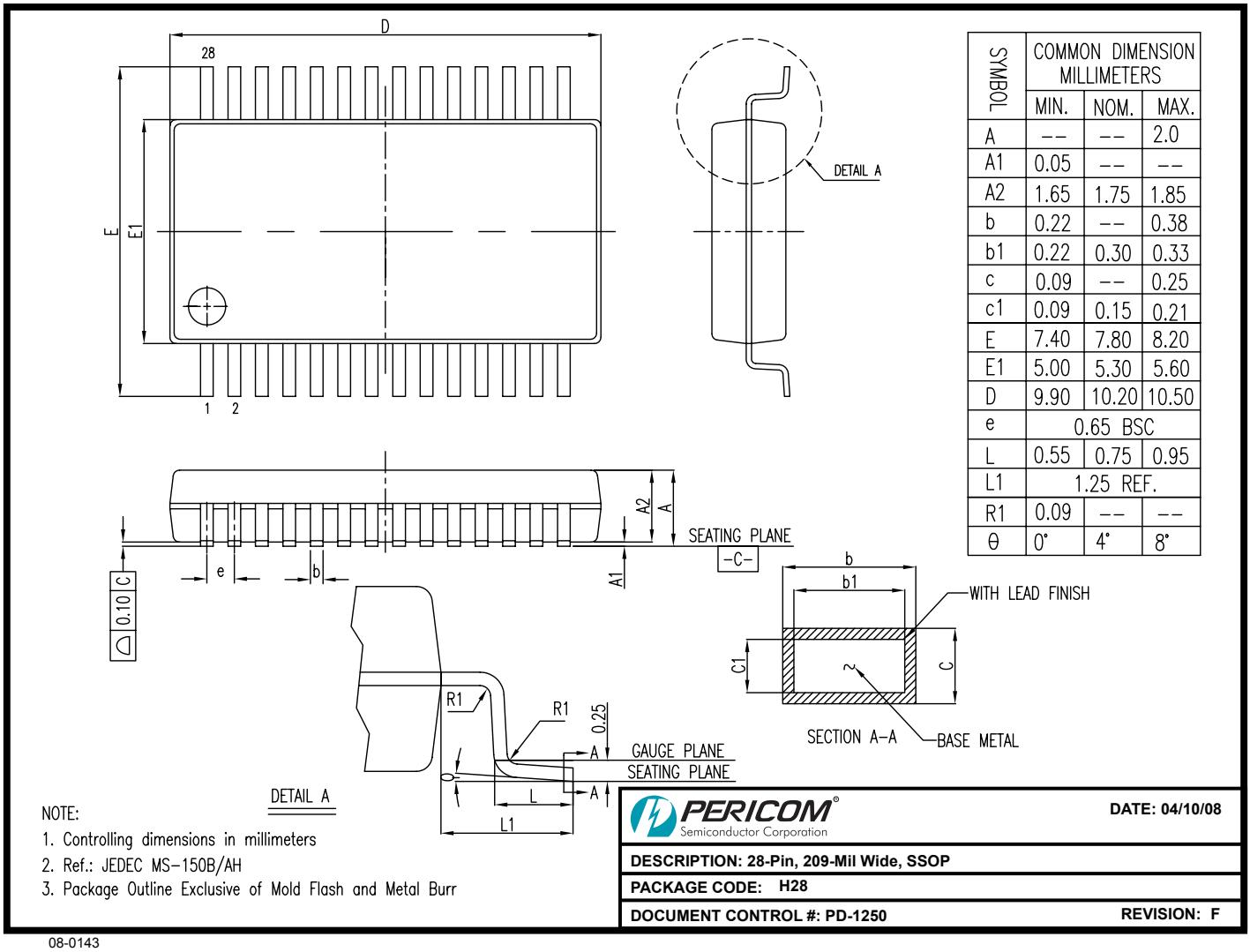
| Symbol | Parameters | Min | Max. | Units | Notes |
|---|---|---|---|---|---|
| $F_{IN}$ | PLL Mode | 95 | 105 | MHz | |
| | Bypass Mode | 100 | 400 | MHz | |
| $T_{rise}$ / $T_{fall}$ | Rise and Fall Time (measured between 0.175V to 0.525V) | 175 | 700 | ps | 2 |
| $DT_{rise}$ / $DT_{fall}$ | Rise and Fall Time Variation | | 125 | ps | 2 |
| $T_{pd}$ | PLL Mode | | ±250 | ps | |
| | Non-PLL Mode | 2.5 | 6.5 | ns | |
| $T_{jitter}$ | Cycle – Cycle Jitter | | 50 | ps | 3, 4 |
| $V_{HIGH}$ | Voltage High including overshoot | 660 | 1150 | mV | 2 |
| $V_{LOW}$ | Voltage Low including undershoot | -300 | | mV | 2 |
| $V_{cross}$ | Absolute crossing point voltages | 250 | 550 | mV | 2 |
| $DV_{cross}$ | Total Variation of Vcross over all edges | | 140 | mV | 2 |
| $T_{DC}$ | Duty Cycle | 45 | 55 | % | 3 |
| $T_{jadd}$ | Additive RMS phase jitter for PCIe 2.0 | <0 | 1 | ps | 5 |

**Notes:**
1. Test configuration is $R_s$ = 33.2Ω, Rp = 49.9Ω, and 2pF.
2. Measurement taken from Single Ended waveform.
3. Measurement taken from Differential waveform.
4. Measurement taken using M1 data capture analysis tool.
5. Additive jitter is calculated from input and output RMS phase jitter by using PCIe 2.0 filter. ($T_{jadd} = \sqrt{(\text{output jitter})^2 - (\text{input jitter})^2}$

## Configuration Test Load Board Termination



## Packaging Mechanical: 28-Pin SSOP (H)




| SYMBOL | COMMON DIMENSION MILLIMETERS | | |
|---|---|---|---|
| | MIN. | NOM. | MAX. |
| A | -- | -- | 2.0 |
| A1 | 0.05 | -- | -- |
| A2 | 1.65 | 1.75 | 1.85 |
| b | 0.22 | -- | 0.38 |
| b1 | 0.22 | 0.30 | 0.33 |
| c | 0.09 | -- | 0.25 |
| c1 | 0.09 | 0.15 | 0.21 |
| E | 7.40 | 7.80 | 8.20 |
| E1 | 5.00 | 5.30 | 5.60 |
| D | 9.90 | 10.20 | 10.50 |
| e | 0.65 BSC | | |
| L | 0.55 | 0.75 | 0.95 |
| L1 | 1.25 REF. | | |
| R1 | 0.09 | -- | -- |
| θ | 0° | 4° | 8° |

NOTE:
1. Controlling dimensions in millimeters
2. Ref.: JEDEC MS-150B/AH
3. Package Outline Exclusive of Mold Flash and Metal Burr

PERICOM Semiconductor Corporation

**DATE: 04/10/08**

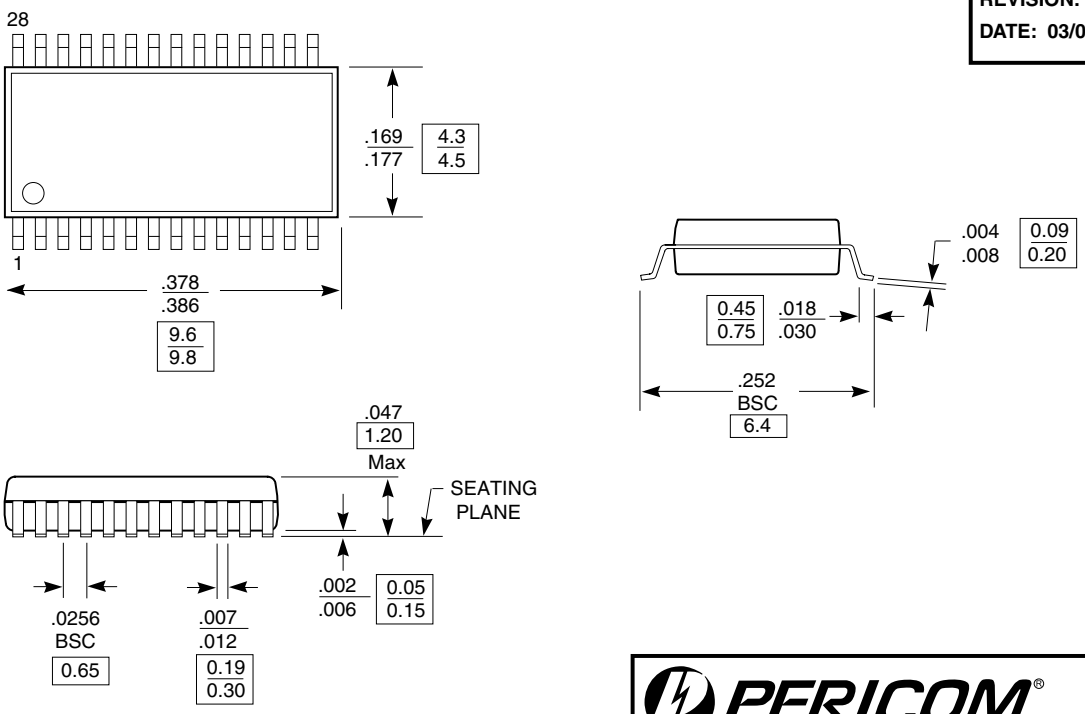
**DESCRIPTION: 28-Pin, 209-Mil Wide, SSOP**

**PACKAGE CODE: H28**

**DOCUMENT CONTROL #: PD-1250** **REVISION: F**

08-0143

## Packaging Mechanical: 28-Pin TSSOP (L)




DOCUMENT CONTROL NO.
PD - 1313

REVISION: D
DATE: 03/09/05

**Note**:
1. Package Outline Exclusive of Mold Flash and Metal Burr
2. Controlling dimentions in millimeters
3. Ref: JEDEC MO-153F/AE

PERICOM®
Pericom Semiconductor Corporation
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1-800-435-2335 • www.pericom.com

DESCRIPTION: 28-Pin, 173-Mil Wide, TSSOP

PACKAGE CODE: L

## Ordering Information(1-3)

| Ordering Code | Package Code | Package Description |
|---|---|---|
| PI6C20400AHE | HE | 28-pin, 209-mil wide, SSOP, Pb-Free and Green |
| PI6C20400ALE | LE | 28-pin, 173-mil wide, TSSOP, Pb-Free and Green |

**Notes:**
1. Thermal characteristics can be found on the company web site at www.pericom.com/packaging/
2. E = Pb-free and Green
3. Adding an X suffix = Tape/Reel



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