

SKYWORKS®

DATA SHEET

SE2432L: 2.4 GHz ZigBee®/Smart Energy Front-End Module

Applications

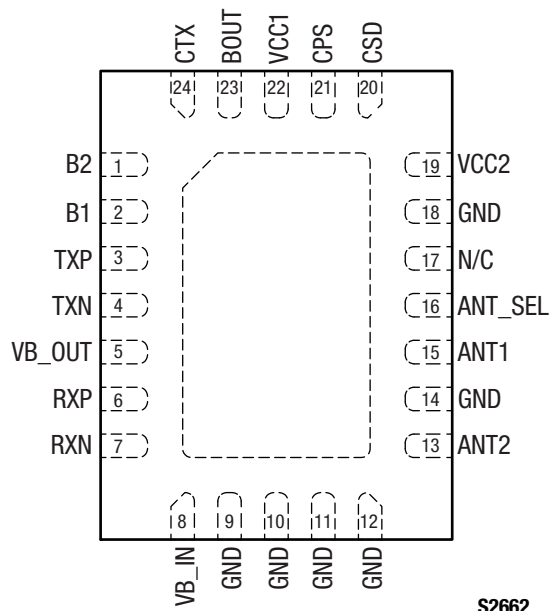
- Smart meters
- In-home appliances
- Smart thermostats

Features

- Integrated PA with up to +24 dBm output power
- Integrated LNA with programmable bypass
- Integrated antenna switching with transmit and receive diversity function
- Low NF: 2 dB typical
- Differential transmit/receive interface with integrated baluns
- Fast switch on/off time: <800 ns
- Supply range: 2.0 V to 3.6 V
- Sleep mode current: 0.05 μ A typical
- Small QFN (24-pin, 3 x 4 mm) package (MSL1, 260 °C per JEDEC-J-STD-020)



Skyworks Green™ products are compliant with all applicable legislation and are halogen-free. For additional information, refer to *Skyworks Definition of Green™*, document number SQ04-0074.



S2662

Figure 1. SE2432L Pinout – 24-Pin QFN (Top View)

Description

The SE2432L is a high performance, fully integrated RF Front-End Module (FEM) designed for ZigBee®/Smart Energy applications.

The SE2432L is designed for ease of use and maximum flexibility. The device provides integrated and fully matched input baluns, an integrated inter-stage matching and harmonic filter, and digital controls compatible with 1.6 to 3.6 V CMOS levels.

The RF blocks operate over a wide supply voltage range from 2.0 V to 3.6 V that allows the SE2432L to be used in battery powered applications over a wide spectrum of the battery discharge curve.

The SE2432L is provided in a small, 24-pin, 3 x 4 mm Quad Flat No-Lead (QFN) package. The pin configuration and package are shown in Figure 1. A functional block diagram is shown in Figure 2. Signal pin assignments and functional pin descriptions are provided in Table 1.

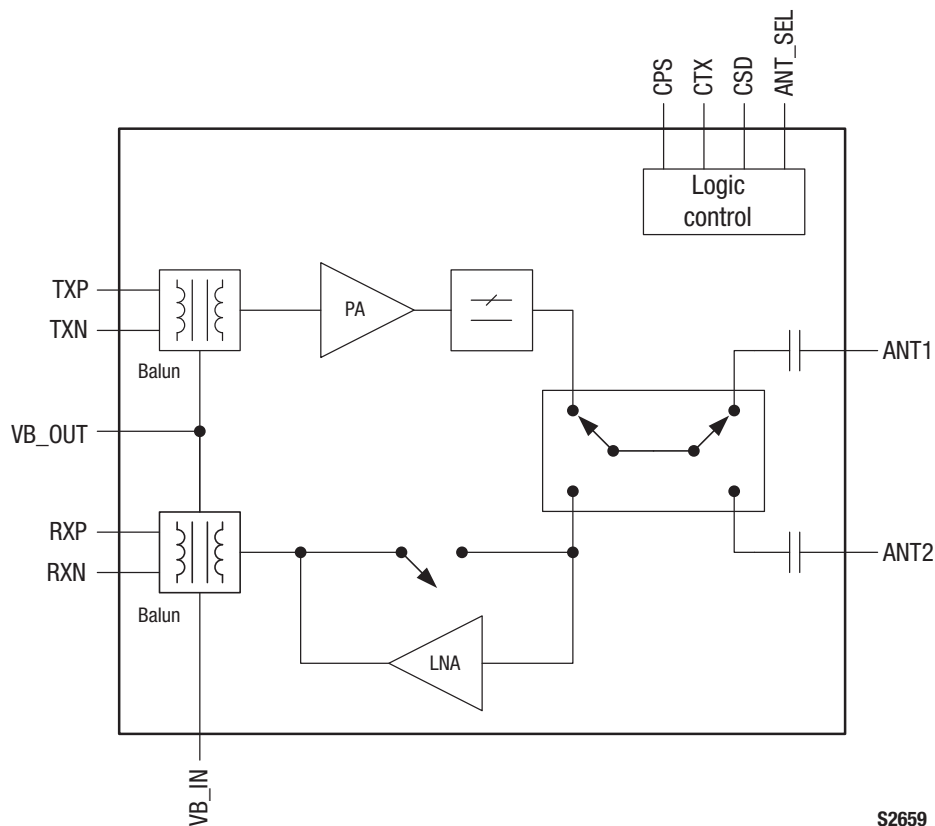


Figure 2. SE2432L Block Diagram

Table 1. SE2432L Signal Descriptions

| Pin | Name | Description | Pin | Name | Description |
|-----|--------|--|-----|---------|--|
| 1 | B2 | Connect through bias resistor to pin 23 | 13 | ANT2 | Connect to 50 Ω antenna |
| 2 | B1 | Connect through bias resistor to pin 23 | 14 | GND | Ground |
| 3 | TXP | Positive transmit input signal from transceiver, 200 Ω differential | 15 | ANT1 | Connect to 50 Ω antenna |
| 4 | TXN | Negative transmit input signal from transceiver, 200 Ω differential | 16 | ANT_SEL | Connect to GPIO signal to control antenna switch (see Table 7) |
| 5 | VB_OUT | Transmit balun bias core supply from transceiver (optional connection) | 17 | N/C | No connection |
| 6 | RXP | Positive receiver output signal to transceiver, 200 Ω differential | 18 | GND | Ground |
| 7 | RXN | Negative receiver output signal to transceiver, 200 Ω differential | 19 | VCC2 | Connect to positive supply |
| 8 | VB_IN | Receive balun bias core supply from transceiver (optional connection) | 20 | CSD | Connect to GPIO signal for mode control (see Table 9) |
| 9 | GND | Ground | 21 | CPS | Connect to GPIO signal for mode control (see Table 6) |
| 10 | GND | Ground | 22 | VCC1 | Connect to positive supply |
| 11 | GND | Ground | 23 | BOUT | Star connect to bias1 and bias 2 resistors |
| 12 | GND | Ground | 24 | CTX | Connect to GPIO signal for mode control (see Table 6) |

Table 2. SE2432L Absolute Maximum Ratings (Note 1)

| Parameter | Symbol | Minimum | Maximum | Units |
|--|-------------------------|---------|---------------|-------|
| Supply voltage | V _{CC1} | −0.3 | +3.6 | V |
| Supply voltage | V _{CC2} | −0.3 | +3.8 (Note 2) | V |
| Control pin voltages | | −0.3 | +3.6 | V |
| Transmit output power at ANT1 or ANT2 port into 50 Ω load | P _{OUT_TX_MAX} | | +24 | dBm |
| Transmit input power at the TXN and TXP ports | P _{IN_TX_MAX} | | +6 | dBm |
| Receive input power at ANT1 or ANT2 ports | P _{IN_RX_MAX} | | +5 | dBm |
| Operating temperature | T _A | −40 | +125 | °C |
| Storage temperature | T _{STG} | −40 | +125 | °C |
| Electrostatic discharge: Human Body Model (HBM), Class 1C | ESD | | 1000 | V |

Note 1: Exposure to maximum rating conditions for extended periods may reduce device reliability. There is no damage to device with only one parameter set at the limit and all other parameters set at or below their nominal value. Exceeding any of the limits listed here may result in permanent damage to the device.

Note 2: V_{CC2} is restricted to +3.6 V when operated at T_A = 125 °C.

CAUTION: Although this device is designed to be as robust as possible, Electrostatic Discharge (ESD) can damage this device. This device must be protected at all times from ESD. Static charges may easily produce potentials of several kilovolts on the human body or equipment, which can discharge without detection. Industry-standard ESD precautions should be used at all times.

Table 3. Recommended Operating Conditions

| Parameter | Symbol | Minimum | Typical | Maximum | Units |
|-------------------------------|----------------|---------|---------|---------|-------|
| Supply voltage for balun bias | VB_IN, VB_OUT | 1.6 | | 3.6 | V |
| Supply voltage on VCC pins | VCC1, VCC2 | 2.0 | 3.0 | 3.6 | V |
| Operating temperature | T _A | −40 | +25 | +125 | °C |

Electrical and Mechanical Specifications

The absolute maximum ratings of the SE2432L are provided in Table 2. The recommended operating conditions are specified in Table 3 and electrical specifications are provided in Tables 4 through 8.

The state of the SE2432L is determined by the logic provided in Table 6.

Table 4. SE2432L Electrical Specifications (Note 1)
(VCC1 = VCC2 = 3.0 V, TA = +25 °C, Unless Otherwise Noted)

| Parameter | Symbol | Test Condition | Min | Typical | Max | Units |
|--|------------------------------------|---|----------|-----------------|------------|----------------|
| DC Characteristics | | | | | | |
| Total supply current | I _{CC_TX} | Transmit mode, CPS = CSD = CTX = 3.0 V: P _{OUT} = +20 dBm P _{OUT} = +17 dBm P _{OUT} = +10 dBm | | 110 90 45 | | mA mA mA |
| Total supply current | I _{CC_RX} | Receive mode, CPS = CSD = 3.0 V, CTX = 0 V | | 5 | 7 | mA |
| Total supply current | I _{CC_RX_BYPASS} | Receive bypass mode, CSD = 3.0 V, CPS = CTX = 0 V | | | 300 | μA |
| Sleep supply current | I _{CC_OFF} | No RF, CTX = CPS = CSD = 0 V | | 0.05 | 1.00 | μA |
| Quiescent current | I _Q | No RF, CPS = CSD = CTX = 3.0 V | | 30 | | mA |
| Logic Characteristics | | | | | | |
| Control voltage: High Low | V _{IH} V _{IL} | | 1.6 0 | | 3.6 0.3 | V V |
| Control current: High Low | I _{IH} I _{IL} | | | | 1 1 | μA μA |
| Dual Antenna Switch Characteristics | | | | | | |
| Isolation between ANT1 and ANT2 ports | ISOL _{ANTSW} | | | -20 | | dB |
| ANT1 to ANT2 switching time | t _{ANT1_ANT2} | | | 400 | | ns |

Note 1: Performance is guaranteed only under the conditions listed in this Table.

Table 5. SE2432L Electrical Specifications (1 of 2) (Note 1)**(VB_IN = VB_OUT = 1.6 to 3.6 V, VCC1 = VCC2 = 3.0 V, TA = +25 °C, All Unused Ports Terminated With 50 Ω, Unless Otherwise Noted)**

| Parameter | Symbol | Test Condition | Min | Typical | Max | Units |
|---|-------------------|--|---|---|------|---------------------------------|
| AC Transmit Characteristics | | | | | | |
| Frequency range | f | | 2400 | | 2483 | MHz |
| Output power at ANT1 or ANT2 port | P _{OUT} | @ 2400 to 2483 MHz, OEVM = 1% typical, VCC1 = VCC2 =: 3.6 V 3.3 V 3.0 V 2.7 V 2.0 V | | +24.0 +22.5 +21.0 +20.5 +17.0 | | dBm dBm dBm dBm dBm |
| Small signal gain, high power mode | S ₂₁ | @ 2400 to 2483 MHz | 20 | 22 | 24 | dB |
| Small signal gain variation | ΔS ₂₁ | @ 2400 to 2483 MHz, across all ZigBee channels | | | 2 | dBp-p |
| 2 nd and 3 rd harmonics | 2fo, 3fo | @ 2400 to 2483 MHz, P _{OUT} = +20 dBm, IEEE 802.15.4 source | | | −42 | dBm/MHz |
| Output return loss | S ₂₂ | @ 2400 to 2483 MHz, ANT1 or ANT2 port | | −10 | −5 | dB |
| Transmit port impedance | Z _{IN} | | | 200 | | Ω |
| Turn-on time | t _{RISE} | From 50% of CTX edge to 90% of final RF output power | | | 800 | ns |
| Turn-off time | t _{FALL} | From 50% of CTX edge to 10% of final RF output power | | | 800 | ns |
| Stability | Stab | CW, Pin = 0 dBm, 0.1 GHz to 20 GHz, load VSWR = 6:1 | All non-harmonically related outputs < −42 dBm/MHz | | | — |
| Ruggedness | RU | CW, Pin = +6 dBm, load VSWR = 10:1 | No permanent damage | | | — |
| AC Receive Characteristics | | | | | | |
| Frequency range | f | | 2400 | | 2483 | MHz |
| Receive gain | RX_GAIN | @ 2400 to 2483 MHz, CPS = CSD = logic “1,” CTX = logic “0” | 10.0 | 11.5 | 13.0 | dB |
| Receive Noise Figure | NF | @ 2400 to 2483 MHz, CPS = CSD = logic “1,” CTX = logic “0” | | 2.0 | 2.5 | dB |
| 3 rd Order Input Intercept Point | IIP3 | @ 2400 to 2483 MHz, CPS = CSD = logic “1,” CTX = logic “0” | −3 | +2 | | dBm |

Table 5. SE2432L Electrical Specifications: (2 of 2) (Note 1)**(VB_IN = VB_OUT = 1.6 to 3.6 V, VCC1 = VCC2 = 3.0 V, Ta = +25 °C, All Unused Ports Terminated With 50 Ω, Unless Otherwise Noted)**

| Parameter | Symbol | Test Condition | Min | Typical | Max | Units |
|---|-------------------|--|-----|---------|-----|-------|
| AC Receive Characteristics (continued) | | | | | | |
| 1 dB Input Compression Point | IP1dB | @ 2400 to 2483 MHz, CPS = CSD = logic "1," CTX = logic "0" | −13 | −8 | | dBm |
| 1 dB Input Compression Point in bypass mode | IP1dB | CPS = CTX = logic "0," CSD = logic "1" | +10 | | | dBm |
| Input return loss | S11 | @ 2400 to 2483 MHz, ANT1 or ANT2 ports | | −10 | −5 | dBm |
| Receive port impedance | Z _{OUT} | Measured differentially between RXP and RXN | | 200 | | Ω |
| Turn-on time | t _{RISE} | From 50% of CTX edge to 90% of final RF output power | | | 800 | ns |
| Turn-off time | t _{FALL} | From 50% of CTX edge to 10% of final RF output power | | | 800 | ns |
| Gain in bypass mode | G _{BP} | CPW = CTX = logic "0," CSD = logic "1" | | −3 | | dB |

Note 1: Performance is guaranteed only under the conditions listed in this Table.**Table 6. SE2432L Mode Control Logic (Note 1)****(VCC1 = VCC2 = 3.0 V, Ta = +25 °C)**

| Mode | Description | CPS (Pin 21) | CSD (Pin 20) | CTX (Pin 24) |
|------|-------------------------------|-----------------|-----------------|-----------------|
| 0 | All off (sleep mode) (Note 2) | 0 | 0 | 0 |
| 1 | Receive bypass mode | 0 | 1 | 0 |
| 2 | Receive LNA mode | 1 | 1 | 0 |
| 4 | Transmit mode | X | 1 | 1 |

Note 1: "0" = 0 V. "1" = +3.0 V. "X" = don't care (must be either 0 V or Vcc voltage). Any state other than described in this Table places the switch into an undefined state. An undefined state will not damage the device.**Note 2:** All controls must be at logic "0" to achieve the specified sleep current.**Table 7. SE2432L Antenna Enable Logic****(VCC1 = VCC2 = 3.0 V, Ta = +25 °C)**

| Description | CPS (Pin 21) | CSD (Pin 20) | CTX (Pin 24) | ANT_SEL (Pin 16) |
|-------------------|-----------------|-----------------|-----------------|---------------------|
| ANT1 port enabled | X | X | X | 0 |
| ANT2 port enabled | X | X | X | 1 |

Note: "0" = 0 V. "1" = +3.0 V. "X" = don't care. Any state other than described in this Table places the switch into an undefined state. An undefined state will not damage the device.

Evaluation Board Description

The SE2432L Evaluation Board is used to test the performance of the SE2432L FEM. The board is optimized for evaluation, experimentation, and investigation with an 802.15.4 signal source. The design and layout can be quickly and easily transferred into a production design.

An Evaluation Board schematic diagram is provided in Figure 3. A reference design schematic is provided in Figure 4. Table 8 describes the pins on the power and control I/O header (J27). Table 9 provides the Bill of Materials (BOM) list for Evaluation Board components. A photograph of the Evaluation Board is shown in Figure 5.

Evaluation Board Setup Procedure

1. Connect J21, J23, J25, and J26 to 50 Ω instruments. Terminate all unused ports (if applicable) with 50 Ω .
2. Connect the supply ground to pins 19 and 20 of J27.
3. Connect 3.0 V to pins 15 and 16 of J27.
4. Connect 1.8 V to pins 7 and 8 of J36.
5. Connect 3.0 V to pins 3 and 4 of J27.

NOTE: By following the logic in Table 6, the required RF path is selected. Refer to Tables 7 and 8 for antenna port control.

6. Monitor the 2.5 GHz amplifier transmit performance by applying an RF signal to J25 and monitoring the output power on J26 (ANT1) or J23 (ANT2).

CAUTION: Care should be taken not to overdrive the amplifier by applying too much RF on the input to the device. A suitable starting input power would be -20 dBm.

7. Monitor the 2.5 GHz amplifier receive performance by applying an RF signal to J26 (ANT1) or J23 (ANT2) and monitoring the output signal on J25.

Package Dimensions

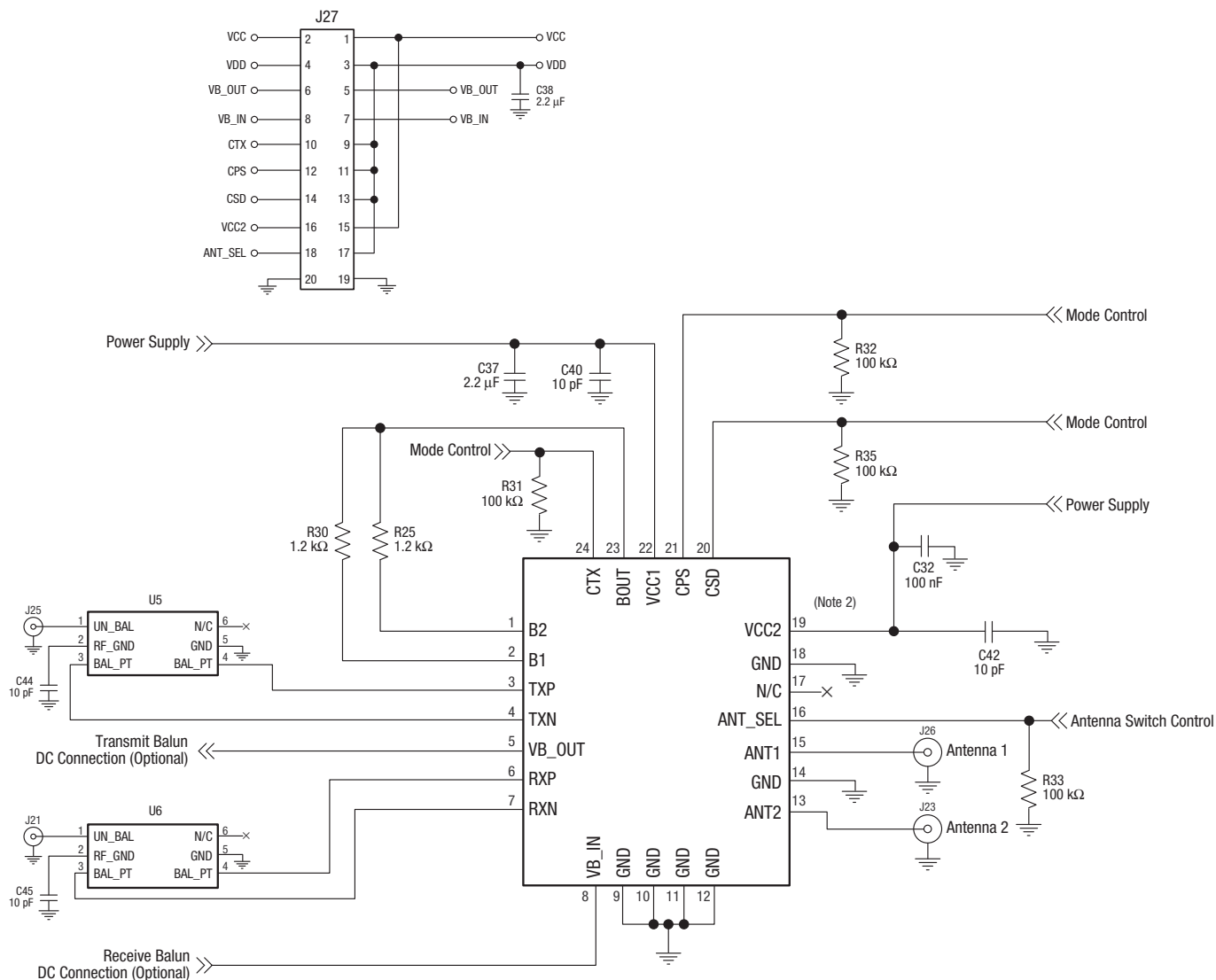
The PCB layout footprint for the SE2432L is provided in Figure 6. Typical case markings are shown in Figure 7. Package dimensions for the 24-pin QFN are shown in Figure 8, and tape and reel dimensions are provided in Figure 9.

Package and Handling Information

Instructions on the shipping container label regarding exposure to moisture after the container seal is broken must be followed. Otherwise, problems related to moisture absorption may occur when the part is subjected to high temperature during solder assembly.

The SE2432L is rated to Moisture Sensitivity Level 1 (MSL1) at 260 °C. It can be used for lead or lead-free soldering. For additional information, refer to the Skyworks Application Note, *Solder Reflow Information*, document number 200164.

Care must be taken when attaching this product, whether it is done manually or in a production solder reflow environment. Production quantities of this product are shipped in a standard tape and reel format.



Notes:

1. The following components are for evaluation purposes only and can be removed in the final application: C38, C44, C45, C46, J27, R31, R32, R33, R35, U5, and U6.
2. L19 is made of a trace between the VCC2 pin and the C42/C32 capacitors.
3. PCB Recommendations:

*Metal Layer 1 = RF traces + control lines. Core thickness between top RF layer and ground plane is critical.
 Metal Layer 2 = Solid ground plane. No traces routing.
 Metal Layer 3 and 4 = Control lines + VCC traces (no VCC plane).
 Pore copper on each layer connected to the ground plane. Use VCC traces in a star distribution pattern.
 Always use 4 layers.*

S2723

Figure 3. SE2432L Evaluation Board Schematic

Table 8. Power and Analog I/O Header: J27, 10x2

| Pin | Pin Name | Description | Recommended Setting |
|-----------------------|----------|------------------------|---|
| 1, 2, 15 | VCC | Supply voltage | General purpose VCC provided as the main power supply |
| 3, 4, 9, 11, 12,13,17 | VDD | Digital supply voltage | Connect to separate power supply voltage |
| 5, 6 | VB_OUT | Bias output | – |
| 7, 8 | VB_IN | Supply voltage | Optional DC connection for transceiver |
| 16 | VCC2 | Supply voltage | General purpose VCC provided as the main power supply |
| 10 | CTX | Control | See Tables 6 and 7 |
| 12 | CPS | Control | |
| 14 | CSD | Control | |
| 18 | ANT_SEL | Control | |
| 19, 20 | GND | Ground | General purpose ground |

Table 9. SE2432L Evaluation Board Bill of Materials (BOM) (Note 1)

| Component | Value | Size | Manufacturer | Mfr Part Number | Characteristics |
|--------------------|----------------|--------------|--------------------------|--------------------|---|
| C32 | 100 nF | 0402 | Murata | GRM155R71C104KA88D | Monolithic ceramic |
| C37, C38 | 2.2 μ F | 0805 | Murata | GRM21BR71A225KA01L | Ceramic capacitor, 2.2 μ F, 10V, 10%, X7R 0805 |
| C40, C42, C44, C45 | 10 pF | 0402 | Murata | GRM1555C1H100JZ01 | Multilayer ceramic |
| J21, J23, J25, J26 | SMA | End launch | Johnson Components | 142-0701-851 | SMA end launch straight jack receptacle – tab contact |
| J27 | 10X2 | 100MIL | Samtec | TSW-110-07-G-D | 100 mil header |
| R25, R30 | 1.2 k Ω | 0402 | Panasonic | ERJ2GEJ122 | Thick film chip resistor |
| R31, R32, R33, R35 | 100 k Ω | 0402 | Panasonic | ERJ2GEJ104 | Thick film chip resistor |
| U3 | – | 3 x 4 mm QFN | Skyworks Solutions, Inc. | SE2432L | 2.4 GHz ZigBee FEM with differential transmit/receive |
| U5, U6 | – | 2 x 1.25 mm | TDK | HHM1521 | Multilayer 2.4 GHz chip baluns |

Note 1: Schematic and BOM have been designed to optimize performance in 802.11a/n applications.

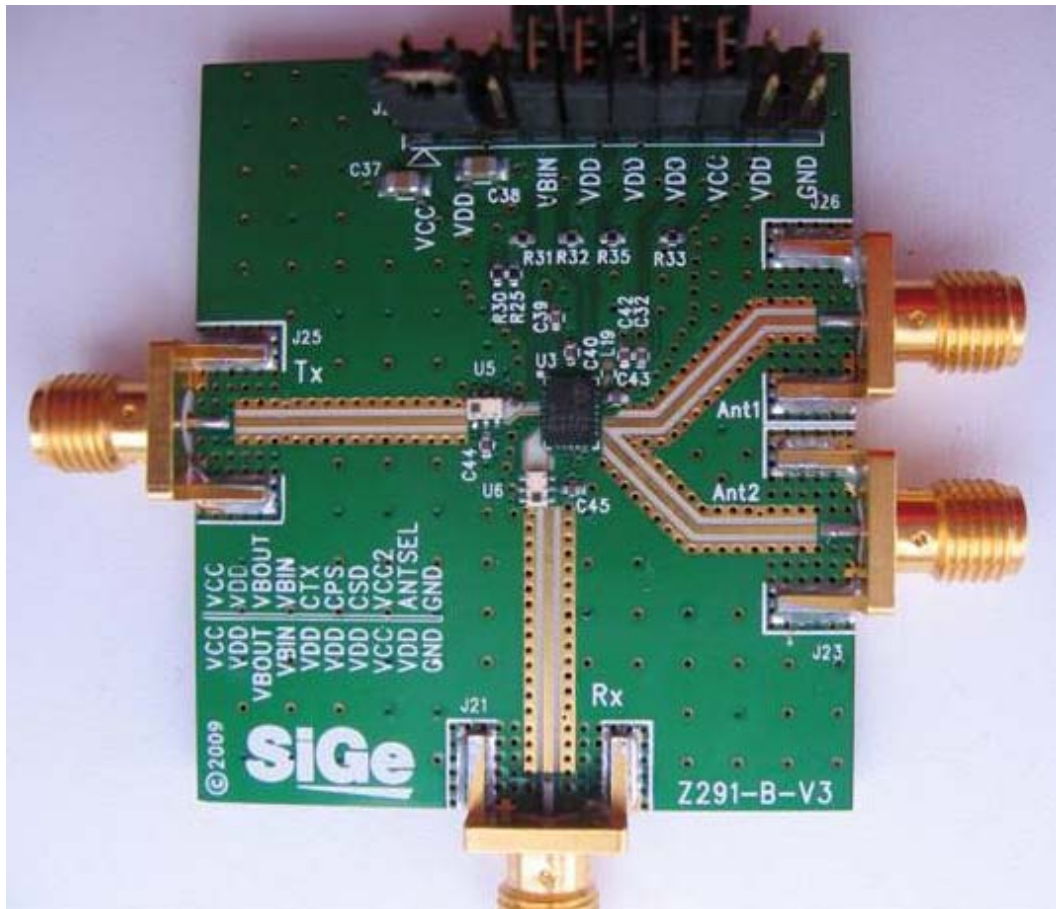
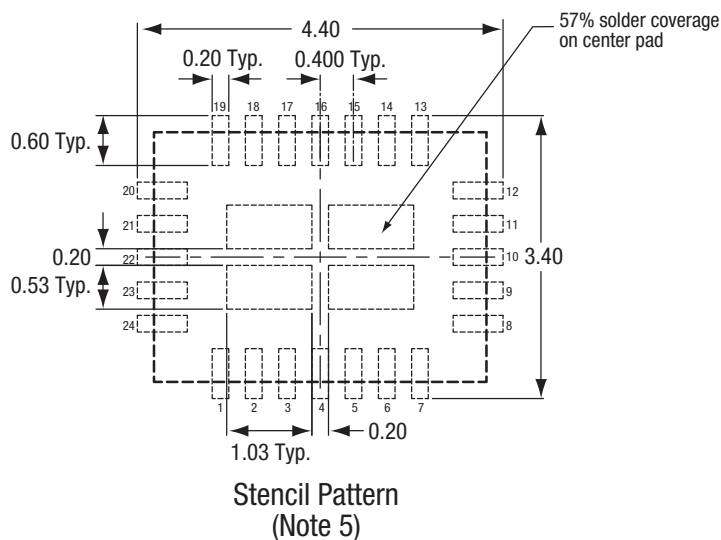
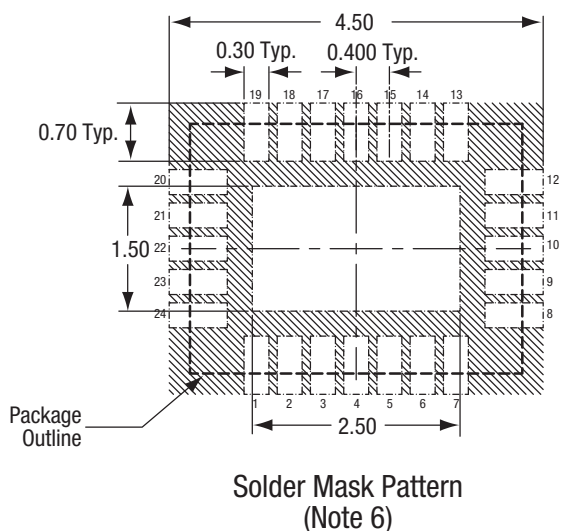
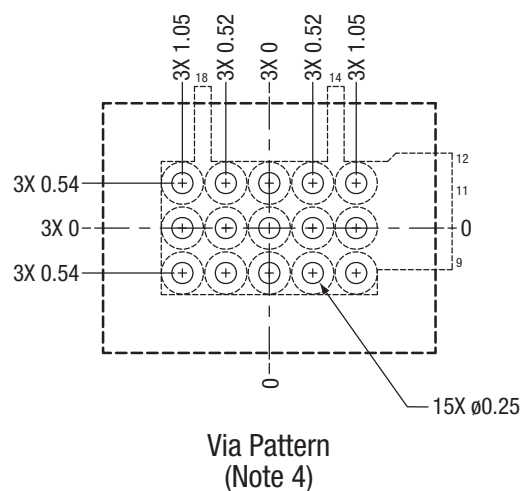
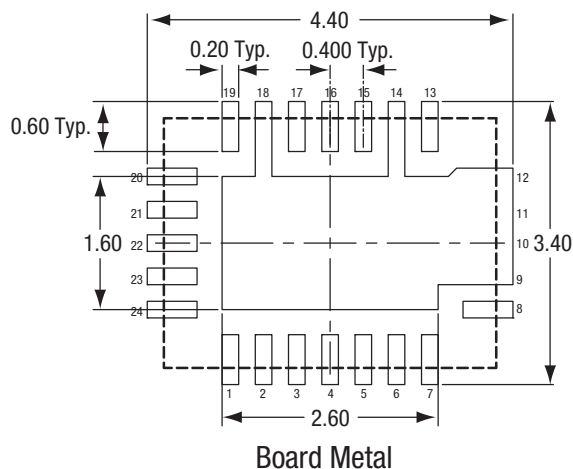


Figure 5. SE2432L Evaluation Board



Notes:

1. All dimensions are in millimeters
2. Dimensioning and tolerancing according to ASME Y14.5M-1994
3. Unless specified, dimensions are symmetrical about center lines.
4. Via hole recommendations: 0.025 mm Cu via wall plating (minimum), soldermask on the far side should tent or plug via holes.
5. Stencil recommendations: 0.10 mm stencil thickness, laser cut apertures, trapezoidal walls and rounded corners offer better paste release.
6. Solder mask recommendations: contact board fabricator for recommended solder mask offset and tolerance.

S2663

Figure 6. PCB Layout Footprint

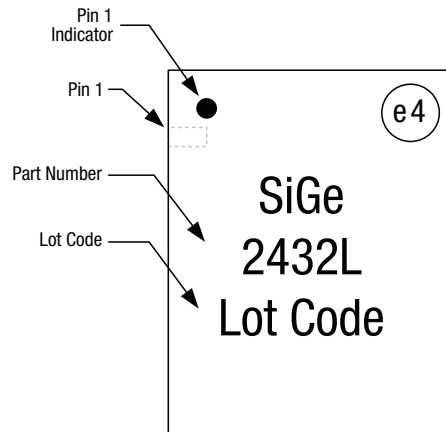
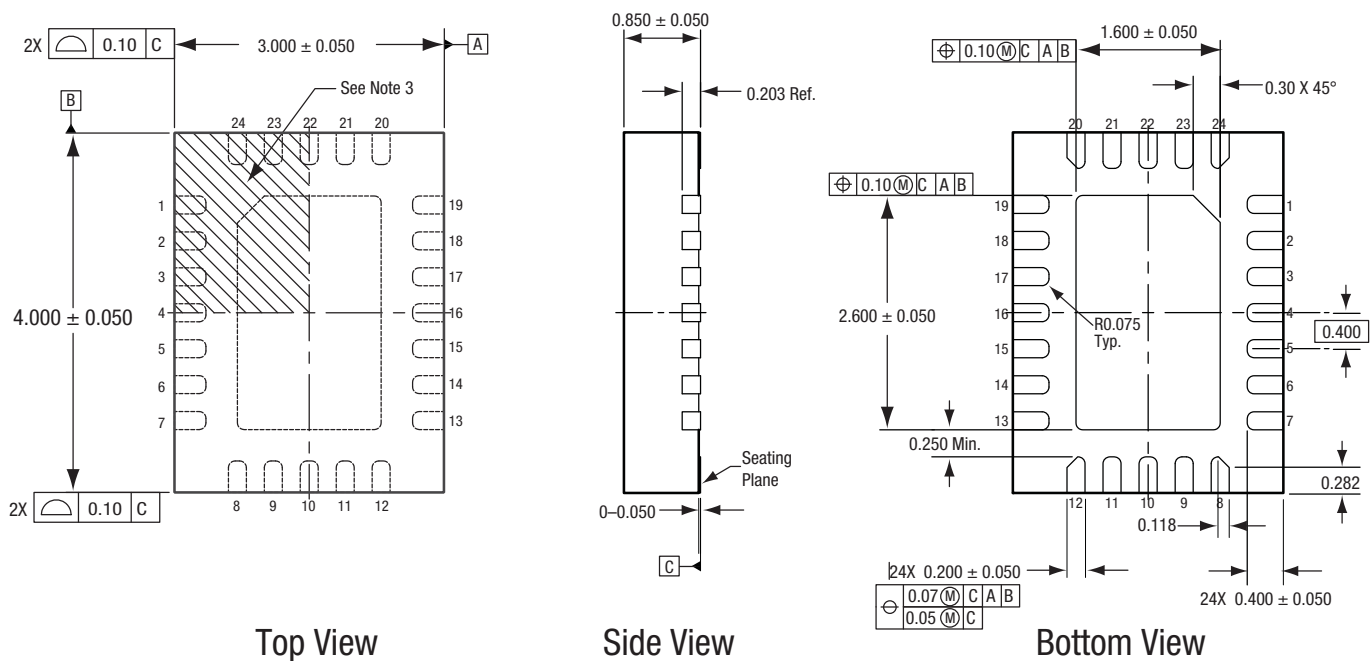


Figure 7. Typical Case Markings

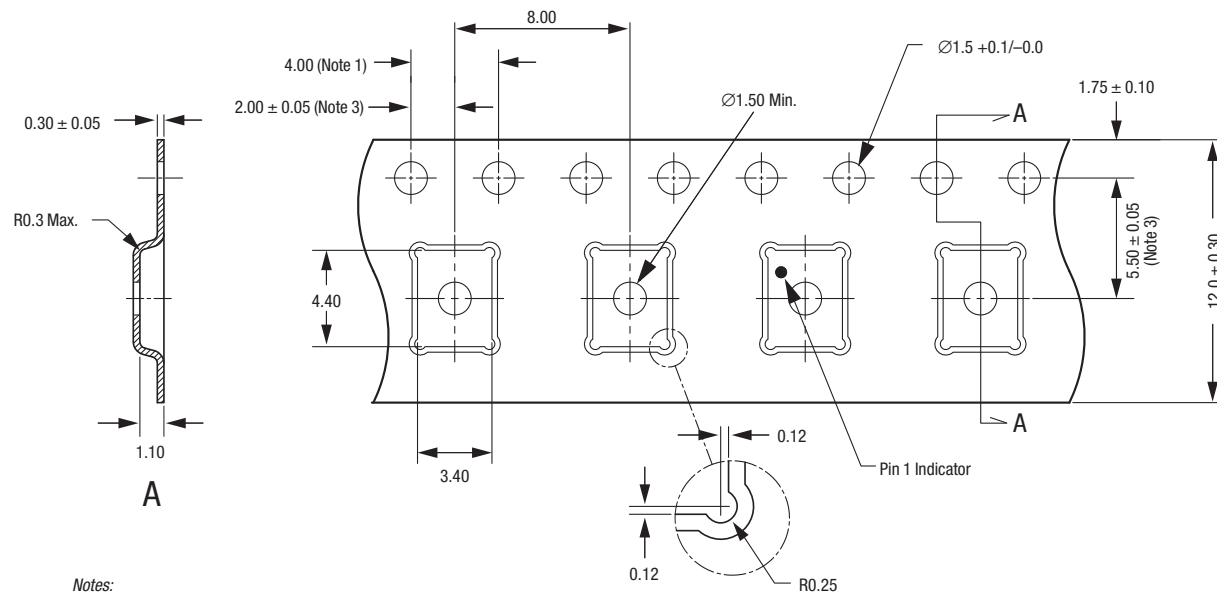


Notes:

1. All measurements are in millimeters.
2. Dimensions and tolerances according to ASME Y14.5M-1994.
Unless otherwise specified, the following values apply:
Decimal Tolerance: Angular Tolerance:
X.X (1 place) ± 0.1 mm $\pm 1^\circ$
X.XX (2 places) ± 0.05 mm
X.XXX (3 places) ± 0.025 mm
3. Terminal #1 identification mark located within marked area.
4. Unless specified, dimensions are symmetrical about center lines.

Y0675

Figure 8. SE2432L 24-Pin QFN Package Dimensions



Notes:

1. 10 sprocket hole pitch cumulative tolerance ± 0.2 .
2. Camber in compliance with EIA 481.
3. Pocket position relative to sprocket hole measured as true position of pocket, not pocket hole.
4. All measurements are in millimeters.

S2742

Figure 9. SE2432L Tape and Reel Dimensions

Ordering Information

| Model Name | Manufacturing Part Number | Evaluation Board Part Number |
|---------------------------------|---------------------------|------------------------------|
| SE2432L ZigBee/Smart Energy FEM | SE2432L-R | SE2432L-EK1 |

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