

## IR2133/IR2135(J&S)&(PbF) IR2233/IR2235(J&S)&(PbF)

### 3-PHASE BRIDGE DRIVER

#### Features

- Floating channel designed for bootstrap operation  
Fully operational to +600V or +1200V  
Tolerant to negative transient voltage  
dV/dt immune
- Gate drive supply range from 10V/12V to 20V DC and  
up to 25V for transient
- Undervoltage lockout for all channels
- Over-current shut down turns off all six drivers
- Independent 3 half-bridge drivers
- Matched propagation delay for all channels
- 2.5V logic compatible
- Outputs out of phase with inputs
- All parts are also available LEAD-FREE

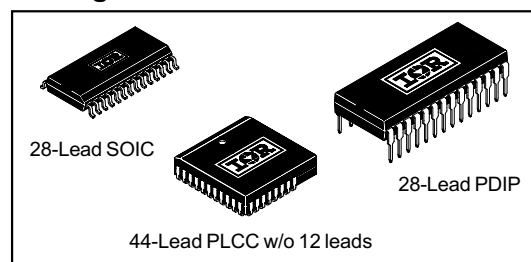
#### Description

The IR2133/IR2135/IR2233/IR2355 (J&S) are high voltage, high speed power MOSFET and IGBT driver with three independent high side and low side referenced output channels for 3-phase applications. Proprietary HVIC technology enables ruggedized monolithic construction. Logic inputs are compatible with CMOS or LSTTL outputs, down to 2.5V logic. An independent operational amplifier provides an analog feedback of bridge current via an external current sense resistor. A current trip function which terminates all six outputs can also be derived from this resistor. A shutdown function is available to terminate all six outputs. An open drain FAULT signal is provided to indicate that an over-current or undervoltage shutdown has occurred. Fault conditions are cleared with the FLT-CLR lead. The output drivers feature a high pulse current buffer stage designed for minimum driver cross-conduction. Propagation delays are matched to simplify use in high frequency applications. The floating channels can be used to drive N-channel power MOSFETs or IGBTs in the high side configuration which operates up to 600 volts or 1200 volts.

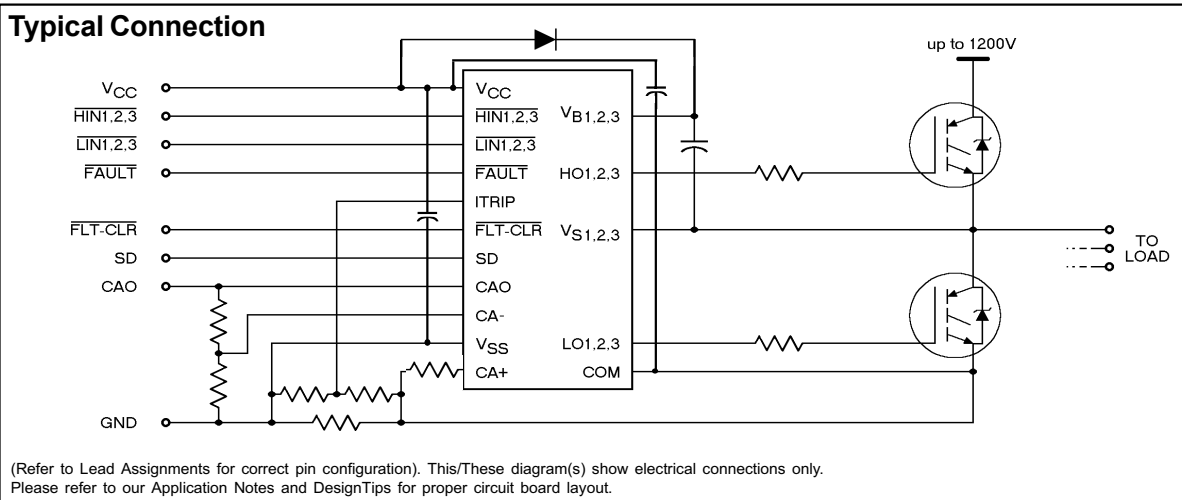
#### Product Summary

|                                  |                             |
|----------------------------------|-----------------------------|
| <b>V<sub>OFFSET</sub></b>        | <b>600V or 1200V max.</b>   |
| <b>I<sub>O+/-</sub></b>          | <b>200 mA / 420 mA</b>      |
| <b>V<sub>OUT</sub></b>           | <b>10 - 20V or 12 - 20V</b> |
| <b>t<sub>on/off</sub> (typ.)</b> | <b>750/700 ns</b>           |
| <b>Deadtime (typ.)</b>           | <b>250 ns</b>               |

#### Packages



#### Typical Connection



# IR2133/IR2135/IR2233/IR2235(J&S)&(PbF)

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## Absolute Maximum Ratings

Absolute Maximum Ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM. The Thermal Resistance and Power Dissipation ratings are measured under board mounted and still air conditions.

| Symbol        | Definition                                                                                     | Min.               | Max.                                                       | Units              |
|---------------|------------------------------------------------------------------------------------------------|--------------------|------------------------------------------------------------|--------------------|
| $V_{B1,2,3}$  | High side floating supply voltage (IR2133/IR2135)                                              | -0.3               | 625                                                        | V                  |
|               | (IR2233/IR2235)                                                                                | -0.3               | 1225                                                       |                    |
| $V_{S1,2,3}$  | High side floating supply offset voltage                                                       | $V_{B1,2,3} - 25$  | $V_{B1,2,3} + 0.3$                                         |                    |
| $V_{HO1,2,3}$ | High side floating output voltage                                                              | $V_{S1,2,3} - 0.3$ | $V_{B1,2,3} + 0.3$                                         |                    |
| $V_{CC}$      | Fixed supply voltage                                                                           | -0.3               | 25                                                         |                    |
| $V_{SS}$      | Logic ground                                                                                   | $V_{CC} - 25$      | $V_{CC} + 0.3$                                             |                    |
| $V_{LO1,2,3}$ | Low side output voltage                                                                        | -0.3               | $V_{CC} + 0.3$                                             |                    |
| $V_{IN}$      | Logic input voltage ( $\overline{HIN}$ , $\overline{LIN}$ , ITRIP, SD & $\overline{FLT-CLR}$ ) | $V_{SS} - 0.3$     | ( $V_{SS} + 15$ ) or ( $V_{CC} + 0.3$ ) whichever is lower |                    |
| $V_{IN,AMP}$  | Op amp input voltage (CA+ & CA-)                                                               | $V_{SS} - 0.3$     | $V_{CC} + 0.3$                                             |                    |
| $V_{OUT,AMP}$ | Op amp output voltage (CAO)                                                                    | $V_{SS} - 0.3$     | $V_{CC} + 0.3$                                             |                    |
| $V_{FLT}$     | FAULT output voltage                                                                           | $V_{SS} - 0.3$     | $V_{CC} + 0.3$                                             |                    |
| $dV_S/dt$     | Allowable offset supply voltage transient                                                      | —                  | 50                                                         | V/ns               |
| $P_D$         | Package power dissipation @ $T_A \leq 25^\circ\text{C}$                                        | —                  | 1.5                                                        | W                  |
|               | (28 Lead PDIP)                                                                                 | —                  | 1.6                                                        |                    |
|               | (28 Lead SOIC)                                                                                 | —                  | 2.0                                                        |                    |
|               | (44 lead PLCC)                                                                                 | —                  | 63                                                         | $^\circ\text{C/W}$ |
| $R_{thJA}$    | Thermal resistance, junction to ambient                                                        | —                  | 83                                                         |                    |
|               | (28 Lead PDIP)                                                                                 | —                  | 78                                                         |                    |
|               | (28 Lead SOIC)                                                                                 | —                  | 63                                                         | $^\circ\text{C}$   |
| $T_J$         | Junction temperature                                                                           | —                  | 125                                                        |                    |
| $T_S$         | Storage temperature                                                                            | -55                | 150                                                        |                    |
| $T_L$         | Lead temperature (soldering, 10 seconds)                                                       | —                  | 300                                                        |                    |

## Recommended Operating Conditions

The input/output logic timing diagram is shown in figure 1. For proper operation the device should be used within the recommended conditions. All voltage parameters are absolute voltages referenced to COM. The  $V_S$  offset rating is tested with all supplies biased at 15V differential.

| Symbol        | Parameter Definition                                                                           | Min.                 | Max.              | Units |
|---------------|------------------------------------------------------------------------------------------------|----------------------|-------------------|-------|
| $V_{B1,2,3}$  | High side floating supply voltage                                                              | $V_{S1,2,3} + 10/12$ | $V_{S1,2,3} + 20$ | V     |
| $V_{S1,2,3}$  | High side floating supply offset voltage (IR2133/IR2135)                                       | Note 1               | 600               |       |
|               | (IR2233/IR2235)                                                                                | Note 1               | 1200              |       |
| $V_{HO1,2,3}$ | High side floating output voltage                                                              | $V_{S1,2,3}$         | $V_{B1,2,3}$      |       |
| $V_{CC}$      | Fixed supply voltage                                                                           | 10 or 12             | 20                |       |
| $V_{SS}$      | Low side driver return                                                                         | -5                   | 5                 |       |
| $V_{LO1,2,3}$ | Low side output voltage                                                                        | 0                    | $V_{CC}$          |       |
| $V_{IN}$      | Logic input voltage ( $\overline{HIN}$ , $\overline{LIN}$ , ITRIP, SD & $\overline{FLT-CLR}$ ) | $V_{SS}$             | $V_{SS} + 5$      |       |
| $V_{IN,AMP}$  | Op amp input voltage (CA+ & CA-)                                                               | $V_{SS}$             | $V_{SS} + 5$      |       |
| $V_{OUT,AMP}$ | Op amp output voltage (CAO)                                                                    | $V_{SS}$             | $V_{SS} + 5$      |       |
| $V_{FLT}$     | FAULT output voltage                                                                           | $V_{SS}$             | $V_{CC}$          |       |

**Note 1:** Logic operational for  $V_S$  of COM - 5V to COM + 600V/1200V. Logic state held for  $V_S$  of COM -5V to COM - $V_{BS}$ . (Please refer to the Design Tip DT97-3 for more details).

**Note 2:** All input pins, op amp input and output pins are internally clamped with a 5.2V zener diode.

### Dynamic Electrical Characteristics

$V_{BIAS}$  ( $V_{CC}$ ,  $V_{BS1,2,3}$ ) = 15V,  $V_{S1,2,3}$  =  $V_{SS}$ ,  $T_A$  = 25°C and  $C_L$  = 1000 pF unless otherwise specified.

| Symbol       | Definition                                                      | Min. | Typ. | Max. | Units      | Test Conditions                                                              |
|--------------|-----------------------------------------------------------------|------|------|------|------------|------------------------------------------------------------------------------|
| $t_{on}$     | Turn-on propagation delay                                       | 500  | 750  | 1000 | ns         | $V_{IN} = 0 \text{ \& } 5V$<br>$V_{S1,2,3} = 0 \text{ to } 600V$<br>or 1200V |
| $t_{off}$    | Turn-off propagation delay                                      | 450  | 700  | 950  |            |                                                                              |
| $t_r$        | Turn-on rise time                                               | —    | 90   | 150  |            |                                                                              |
| $t_f$        | Turn-off fall time                                              | —    | 40   | 70   |            |                                                                              |
| $t_{sd}$     | SD to output shutdown propagation delay                         | 500  | 750  | 1000 |            |                                                                              |
| $t_{itrip}$  | ITRIP to output shutdown propagation delay                      | 600  | 850  | 1100 |            |                                                                              |
| $t_{bl}$     | ITRIP blanking time                                             | —    | 400  | —    |            |                                                                              |
| $t_{flt}$    | ITRIP to $\overline{FAULT}$ propagation delay                   | 400  | 650  | 900  |            |                                                                              |
| $t_{fil,in}$ | Input filter time ( $H_{IN}$ , $L_{IN}$ and SD)                 | —    | 310  | —    |            |                                                                              |
| $t_{fltclr}$ | FLT-CLR to $\overline{FAULT}$ clear time                        | 600  | 850  | 1100 |            |                                                                              |
| DT           | Deadtime, LS turn-off to HS turn-on & HS turn-off to LS turn-on | 100  | 250  | 400  | V/ $\mu$ s | $V_{IN} = 0 \text{ \& } 5V$                                                  |
| SR+          | Amplifier slew rate (positive)                                  | 5    | 10   | —    |            |                                                                              |
| SR-          | Amplifier slew rate (negative)                                  | 2    | 2.5  | —    |            |                                                                              |

NOTE: For high side PWM,  $H_{IN}$  pulse width must be  $\geq 1\mu$  sec

### Static Electrical Characteristics

$V_{BIAS}$  ( $V_{CC}$ ,  $V_{BS1,2,3}$ ) = 15V unless otherwise specified and  $T_A$  = 25°C. All static parameters other than IO and VO are referenced to  $V_{SS}$  and are applicable to all six channels ( $H_{S1,2,3}$  &  $L_{S1,2,3}$ ). The VO and IO parameters are referenced to COM and  $V_{S1,2,3}$  and are applicable to the respective output leads:  $H_{O1,2,3}$  or  $L_{O1,2,3}$ .

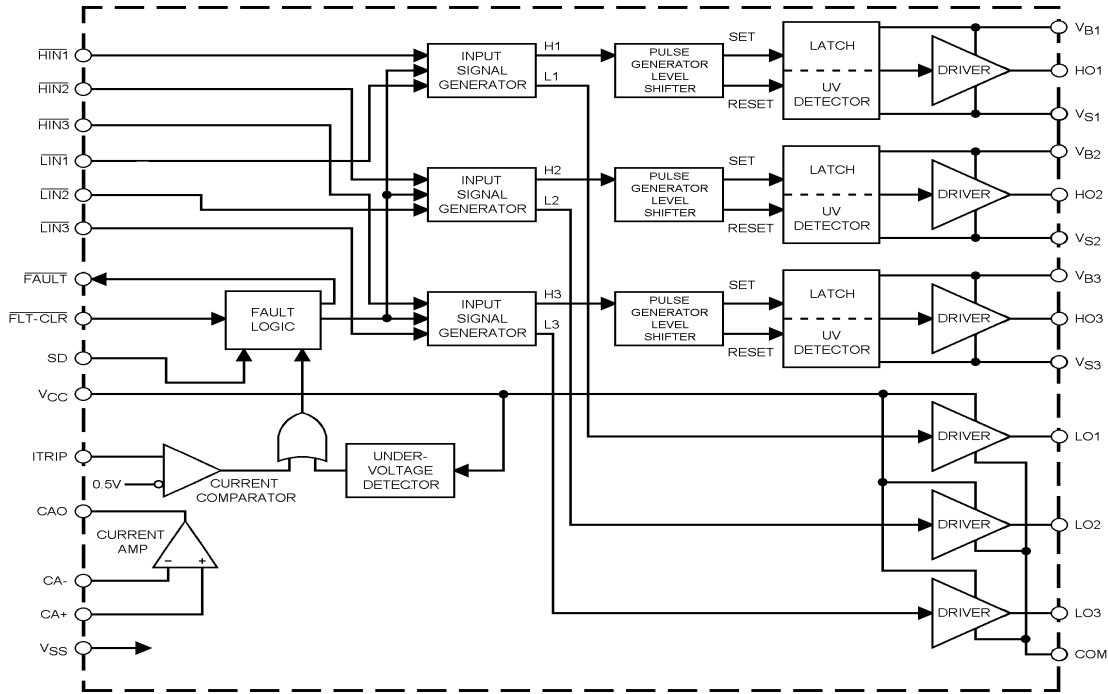
| Symbol        | Definition                                    | Min. | Typ. | Max. | Units   | Test Conditions                   |
|---------------|-----------------------------------------------|------|------|------|---------|-----------------------------------|
| $V_{IH}$      | Logic "0" Input Voltage (OUT = LO)            | 2.2  | —    | —    | V       |                                   |
| $V_{IL}$      | Logic "1" Input Voltage (OUT = HI)            | —    | —    | 0.8  |         |                                   |
| $V_{FCLR,IH}$ | Logic "0" Fault Clear Input Voltage           | 2.2  | —    | —    |         |                                   |
| $V_{FCLR,IL}$ | Logic "1" Fault Clear Input Voltage           | —    | —    | 0.8  |         |                                   |
| $V_{SD,TH+}$  | SD Input Positive Going Threshold             | 1.6  | 1.9  | 2.2  |         |                                   |
| $V_{SD,TH-}$  | SD Input Negative Going Threshold             | 1.4  | 1.7  | 2.0  |         |                                   |
| $V_{IT,TH+}$  | ITRIP Input Positive Going Threshold          | 470  | 570  | 670  | mV      |                                   |
| $V_{IT,TH-}$  | ITRIP Input Negative Going Threshold          | 360  | 460  | 560  |         |                                   |
| $V_{OH}$      | High Level Output Voltage, $V_{BIAS} - V_O$   | —    | —    | 100  |         | $V_{IN} = 0V$ , $I_O = 0A$        |
| $V_{OL}$      | Low Level Output Voltage, $V_O$               | —    | —    | 100  |         |                                   |
| $I_{LK}$      | Offset Supply Leakage Current (IR2133/IR2135) | —    | —    | 50   | $\mu A$ | $V_{B1,2,3} = V_{S1,2,3} = 600V$  |
|               | (IR2233/IR2235)                               | —    | —    | 50   |         | $V_{B1,2,3} = V_{S1,2,3} = 1200V$ |
| $I_{QBS}$     | Quiescent $V_{BS}$ Supply Current             | —    | 50   | 100  | mA      | $V_{IN} = 0V$ or 5V               |
| $I_{QCC}$     | Quiescent $V_{CC}$ Supply Current             | —    | 4    | 8    |         | $V_{IN} = 0V$ or 5V               |
| $I_{IN+}$     | Logic "1" Input Bias Current (OUT = HI)       | —    | 200  | 350  | $\mu A$ | $V_{IN} = 0V$                     |
| $I_{IN-}$     | Logic "0" Input Bias Current (OUT = LO)       | —    | 100  | 250  |         | $V_{IN} = 5V$                     |
| $I_{SD+}$     | "High" Shutdown Bias Current                  | —    | 30   | 100  |         | SD = 5V                           |
| $I_{SD-}$     | "Low" Shutdown Bias Current                   | —    | —    | 100  | nA      | SD = 0V                           |
| $I_{ITRIP+}$  | "High" ITRIP Bias Current                     | —    | 30   | 100  | $\mu A$ | ITRIP = 5V                        |
| $I_{ITRIP-}$  | "Low" ITRIP Bias Current                      | —    | —    | 100  | nA      | ITRIP = 0V                        |

**Static Electrical Characteristics — Continued**

$V_{BIAS}$  ( $V_{CC}$ ,  $V_{BS1,2,3}$ ) = 15V unless otherwise specified and  $T_A = 25^\circ\text{C}$ . All static parameters other than IO and VO are referenced to  $V_{SS}$  and are applicable to all six channels ( $H_{S1,2,3}$  &  $L_{S1,2,3}$ ). The VO and IO parameters are referenced to COM and  $V_{S1,2,3}$  and are applicable to the respective output leads:  $H_{O1,2,3}$  or  $L_{O1,2,3}$ .

| Symbol        | Parameter Definition                                                                                | Min.       | Typ.        | Max.        | Units         | Test Conditions                                                              |
|---------------|-----------------------------------------------------------------------------------------------------|------------|-------------|-------------|---------------|------------------------------------------------------------------------------|
| $I_{FLTCLR+}$ | "High" Fault Clear Input Bias Current                                                               | —          | 200         | 350         | $\mu\text{A}$ | $\overline{\text{FLT-CLR}} = 0\text{V}$                                      |
| $I_{FLTCLR-}$ | "Low" Fault Clear Input Bias Current                                                                | —          | 100         | 250         |               | $\overline{\text{FLT-CLR}} = 5\text{V}$                                      |
| $V_{BSUV+}$   | $V_{BS}$ Supply Undervoltage Positive Going Threshold<br>(for IR2133/IR2233)<br>(for IR2135/IR2235) | 7.6<br>9.2 | 8.6<br>10.4 | 9.6<br>11.6 | V             |                                                                              |
| $V_{BSUV-}$   | $V_{BS}$ Supply Undervoltage Negative Going Threshold<br>(for IR2133/IR2233)<br>(for IR2135/IR2235) | 7.2<br>8.3 | 8.2<br>9.4  | 9.2<br>10.5 |               |                                                                              |
| $V_{BSUVH}$   | $V_{BS}$ Supply Undervoltage Lockout Hysteresis<br>(for IR2133/IR2233)<br>(for IR2135/IR2235)       | —<br>—     | 0.4<br>1    | —<br>—      |               |                                                                              |
| $V_{CCUV+}$   | $V_{CC}$ Supply Undervoltage Positive Going Threshold<br>(for IR2133/IR2233)<br>(for IR2135/IR2235) | 7.6<br>9.2 | 8.6<br>10.4 | 9.6<br>11.6 |               |                                                                              |
| $V_{CCUV-}$   | $V_{CC}$ Supply Undervoltage Negative Going Threshold<br>(for IR2133/IR2233)<br>(for IR2135/IR2235) | 7.2<br>8.3 | 8.2<br>9.4  | 9.2<br>10.5 |               |                                                                              |
| $V_{CCUVH}$   | $V_{CC}$ Supply Undervoltage Lockout Hysteresis<br>(for IR2133/IR2233)<br>(for IR2135/IR2235)       | —<br>—     | 0.4<br>1    | —<br>—      |               |                                                                              |
| $R_{on,FLT}$  | FAULT- Low On Resistance                                                                            | —          | 70          | 100         | $\Omega$      |                                                                              |
| $I_{O+}$      | Output High Short Circuit Pulsed Current                                                            | 200        | 250         | —           | mA            | $V_{OUT} = 0\text{V}$ , $V_{IN} = 0\text{V}$<br>$PW \leq 10 \mu\text{s}$     |
| $I_{O-}$      | Output Low Short Circuit Pulsed Current                                                             | 420        | 500         | —           |               | $V_{OUT} = 15\text{V}$ , $V_{IN} = 5\text{V}$<br>$PW \leq 10 \mu\text{s}$    |
| $V_{OS}$      | Amplifier Input Offset Voltage                                                                      | —          | 0           | 30          | mV            | $CA+ = 0.2\text{V}$ , $CA- = CAO$                                            |
| $I_{IN,AMP}$  | Amplifier Input Bias Current                                                                        | —          | —           | 4           | nA            | $CA+ = CA- = 2.5\text{V}$                                                    |
| CMRR          | Amplifier Common Mode Rejection Ratio                                                               | 50         | 70          | —           | dB            | $CA+ = 0.1\text{V} \ \& \ 5\text{V}$ , $CA- = CAO$                           |
| PSRR          | Amplifier Power Supply Rejection Ratio                                                              | 50         | 70          | —           |               | $CA+ = 0.2\text{V}$ , $CA- = CAO$<br>$V_{CC} = 10\text{V} \ \& \ 20\text{V}$ |
| $V_{OH,Amp}$  | Amplifier High Level Output Voltage                                                                 | 5          | 5.2         | 5.4         | V             | $CA+ = 1\text{V}$ , $CA- = 0\text{V}$                                        |
| $V_{OL,Amp}$  | Amplifier Low Level Output Voltage                                                                  | —          | —           | 20          | mV            | $CA+ = 0\text{V}$ , $CA- = 1\text{V}$                                        |
| $I_{SRC,Amp}$ | Amplifier Output Source Current                                                                     | 4          | 7           | —           | mA            | $CA+ = 1\text{V}$ , $CA- = 0\text{V}$ , $CAO = 4\text{V}$                    |
| $I_{SNK,Amp}$ | Amplifier Output Sink Current                                                                       | 0.5        | 1           | —           |               | $CA+ = 0\text{V}$ , $CA- = 1\text{V}$ , $CAO = 2\text{V}$                    |
| $I_{O+,Amp}$  | Amplifier Output High Short Circuit Current                                                         | —          | 10          | —           |               | $CA+ = 5\text{V}$ , $CA- = 0\text{V}$ , $CAO = 0\text{V}$                    |
| $I_{O-,Amp}$  | Amplifier Output Low Short Circuit Current                                                          | —          | 4           | —           |               | $CA+ = 0\text{V}$ , $CA- = 5\text{V}$ , $CAO = 5\text{V}$                    |

## Functional Block Diagram

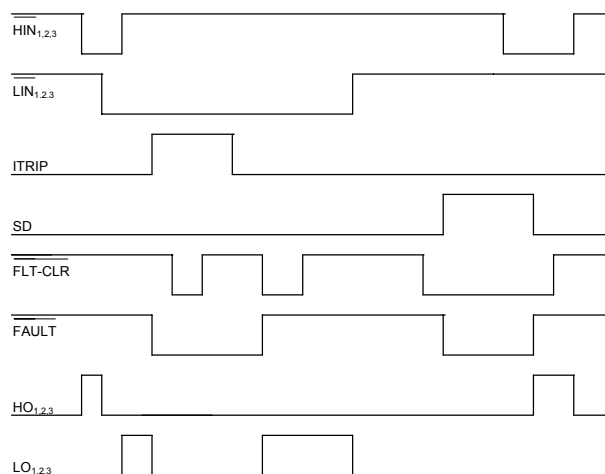


## Lead Definitions

| Symbol   | Lead Description                                                                        |
|----------|-----------------------------------------------------------------------------------------|
| HIN1,2,3 | Logic inputs for high side gate driver outputs (HO1,2,3), out of phase.                 |
| LIN1,2,3 | Logic inputs for low side gate driver outputs (LO1,2,3), out of phase.                  |
| FAULT    | Indicates over-current or undervoltage lockout (low side) has occurred, negative logic. |
| VCC      | Logic and low side fixed supply.                                                        |
| ITRIP    | Input for over-current shut down.                                                       |
| FLT-CLR  | Logic input for fault clear, negative logic.                                            |
| SD       | Logic input for shut down.                                                              |
| CAO      | Output of current amplifier.                                                            |
| CA-      | Negative input of current amplifier.                                                    |
| CA+      | Positive input of current amplifier.                                                    |
| VSS      | Logic ground.                                                                           |
| COM      | Low side return.                                                                        |
| Vb1,2,3  | High side floating supplies.                                                            |
| HO1,2,3  | High side gate drive outputs.                                                           |
| Vs1,2,3  | High side floating supply returns.                                                      |
| LO1,2,3  | Low side gate drive outputs                                                             |

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|                                                           |                                                                                                                 |                                                                                                                |
|-----------------------------------------------------------|-----------------------------------------------------------------------------------------------------------------|----------------------------------------------------------------------------------------------------------------|
|                                                           |                                                                                                                 |                                                                                                                |
| <p>28 Lead DIP</p> <p><b>IR2133</b><br/><b>IR2135</b></p> | <p>44 Lead PLCC w/o 12 Leads</p> <p><b>IR2133J</b><br/><b>IR2135J</b><br/><b>IR2233J</b><br/><b>IR2235J</b></p> | <p>28 Lead SOIC (Wide Body)</p> <p><b>IR2133S</b><br/><b>IR2135S</b><br/><b>IR2233S</b><br/><b>IR2235S</b></p> |
| <p><b>Part Number</b></p>                                 |                                                                                                                 |                                                                                                                |



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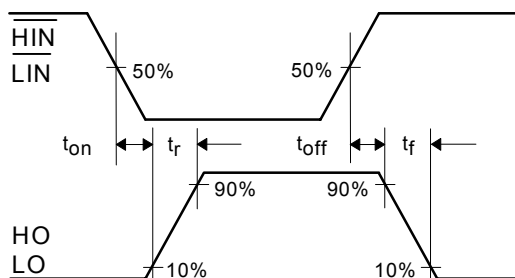


Figure 2. Switching Time Waveform Definitions

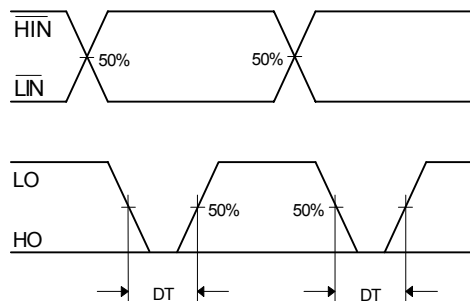


Figure 3. Deadtime Waveform Definitions

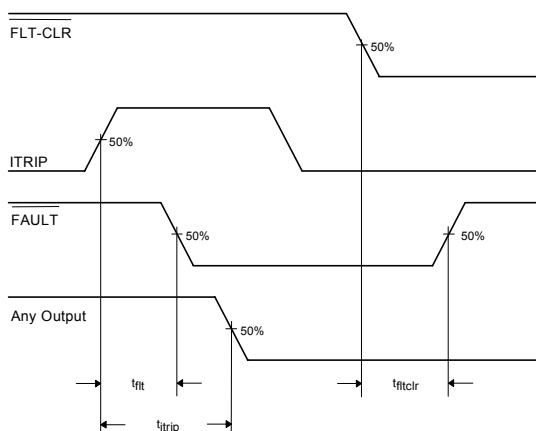


Figure 4. Overcurrent Shutdown Waveform

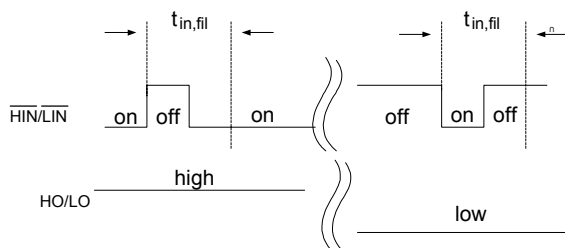


Figure 4.5. Input Filter Function

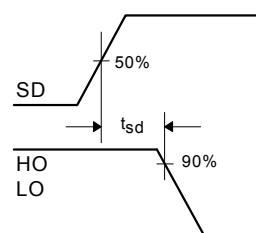


Figure 5. Shutdown Waveform Definitions

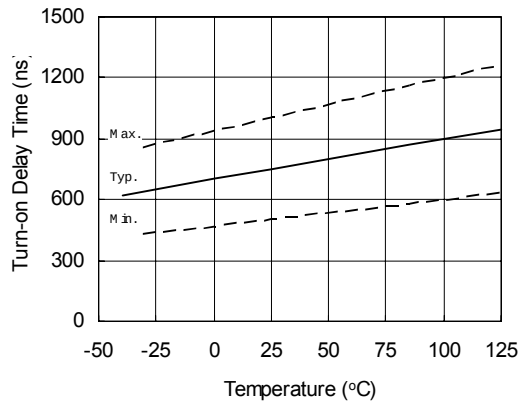


Figure 6A. Turn-On Time vs. Temperature

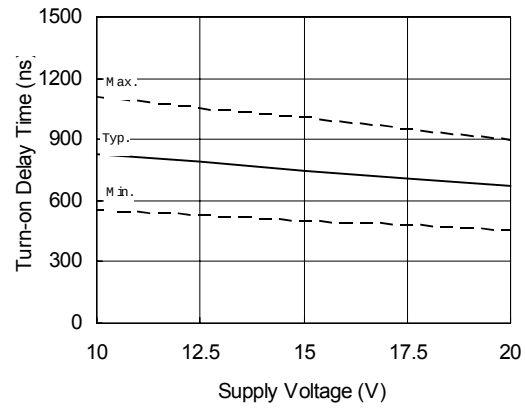


Figure 6B. Turn-On Time vs. Voltage

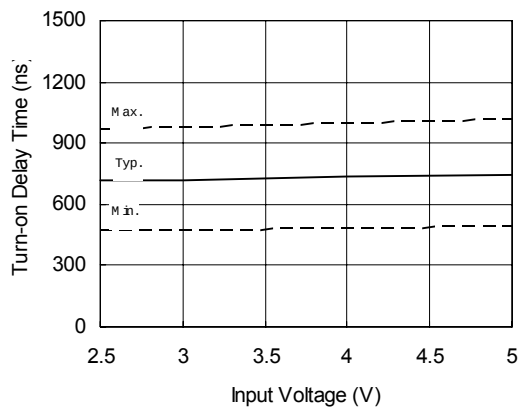


Figure 6C. Turn-On Time vs. Input Voltage

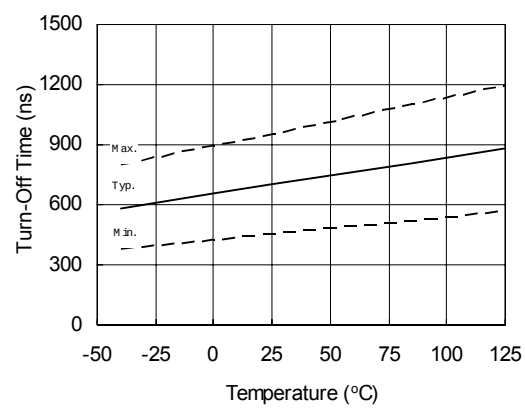


Figure 7A. Turn-Off Time vs. Temperature

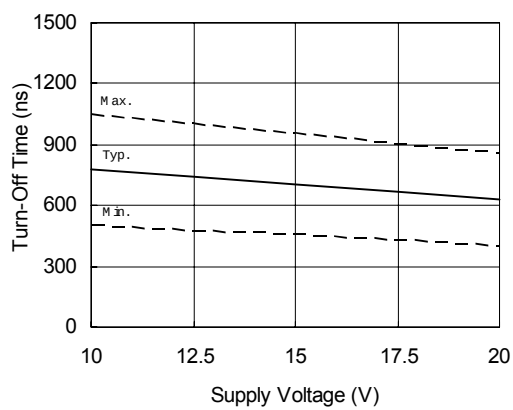


Figure 7B. Turn-Off Time vs. Voltage

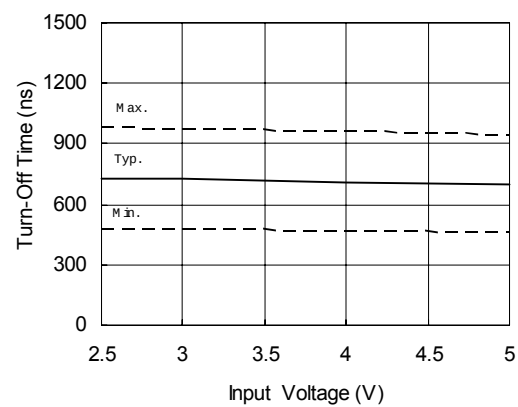


Figure 7C. Turn-Off Time vs. Input Voltage

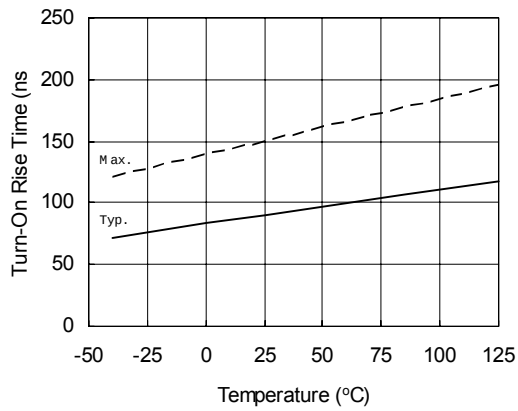


Figure 8A. Turn-On Rise Time vs. Temperature

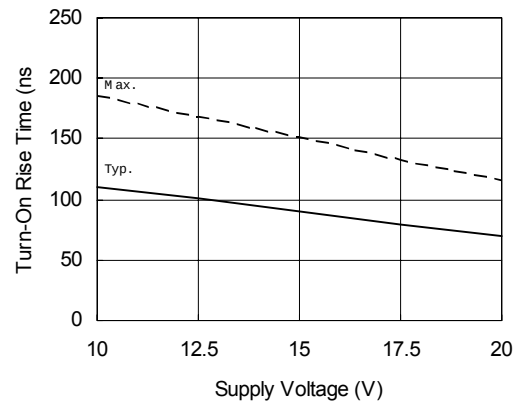


Figure 8B. Turn-On Rise Time vs. Voltage

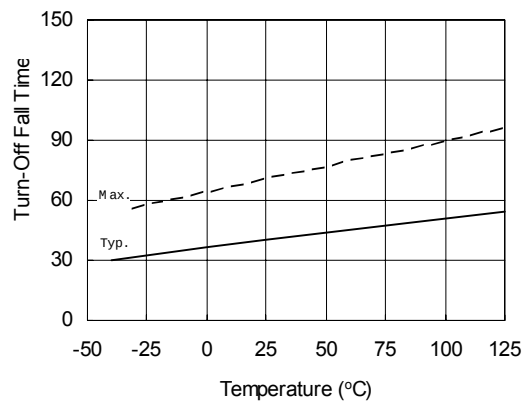


Figure 9A. Turn-Off Fall Time vs. Temperature

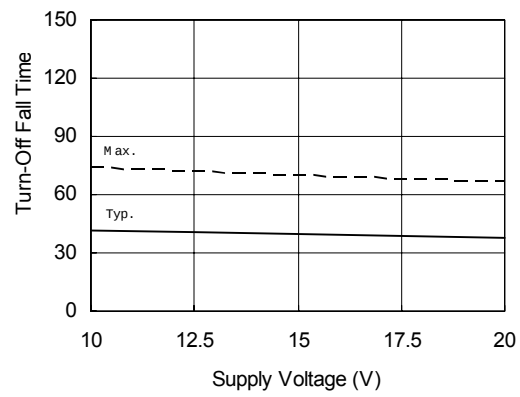


Figure 9B. Turn-Off Fall Time vs. Voltage

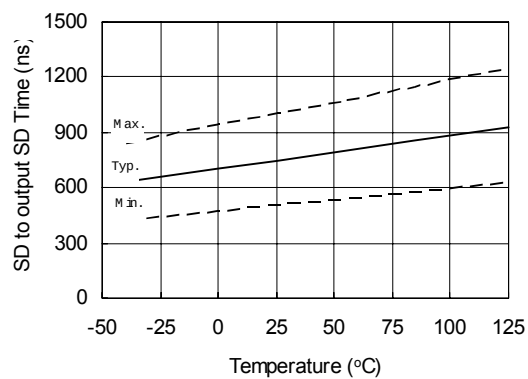


Figure 10A. SD to Output shutdown Time vs. Temperature

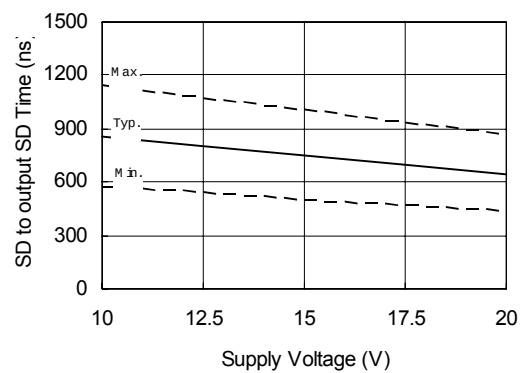


Figure 10B. SD to Output shutdown Time vs. Voltage

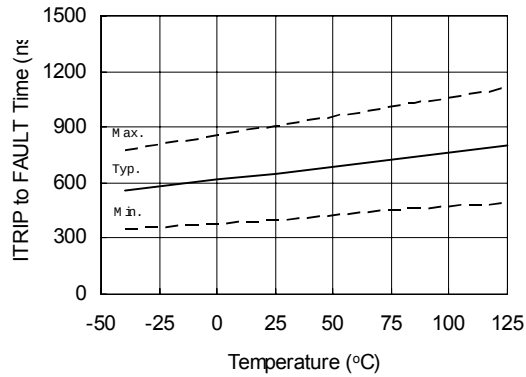


Figure 11A. ITRIP to FAULT Time vs. Temperature

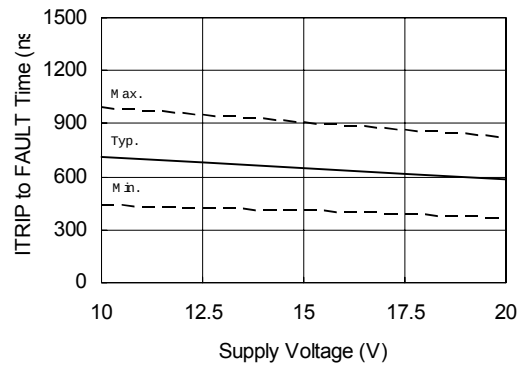


Figure 11B. ITRIP to FAULT Time vs. Voltage

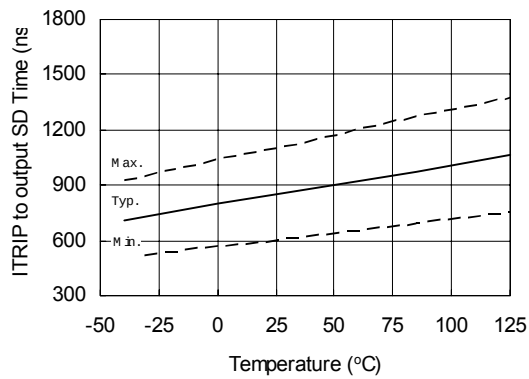


Figure 12A. ITRIP to output shutdown Time vs. Temperature

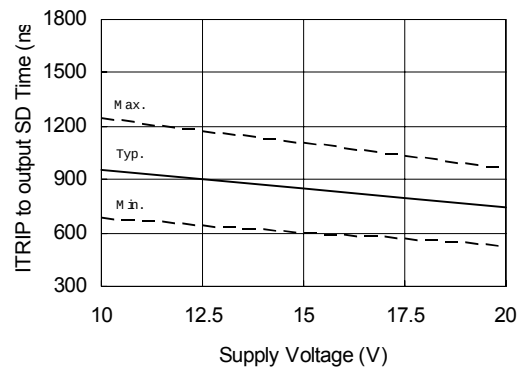


Figure 12B. ITRIP to output shutdown Time vs. Voltage

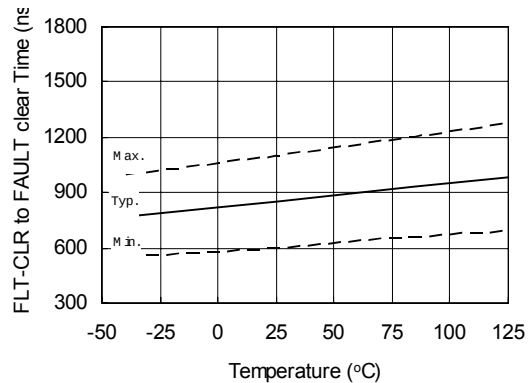


Figure 13A. FLT-CLR to FAULT clear Time vs. Temperature

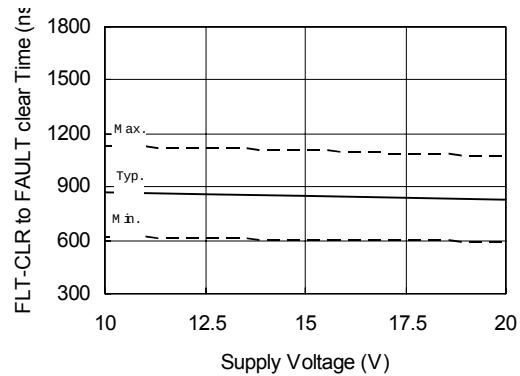


Figure 13B. FLT-CLR to FAULT clear Time vs. Voltage

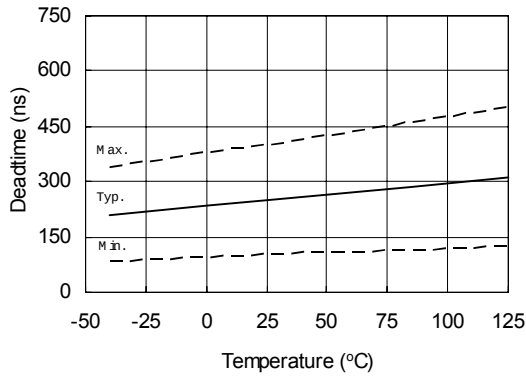


**Figure 14A. Deadtime vs. Temperature**

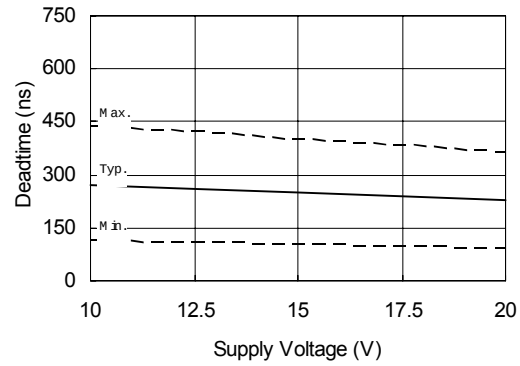


**Figure 14B. Deadtime vs. Voltage**

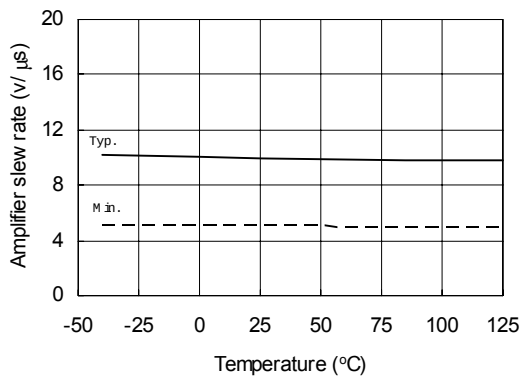


**Figure 15A. Amplifier slew rate (+)  
vs. Temperature**

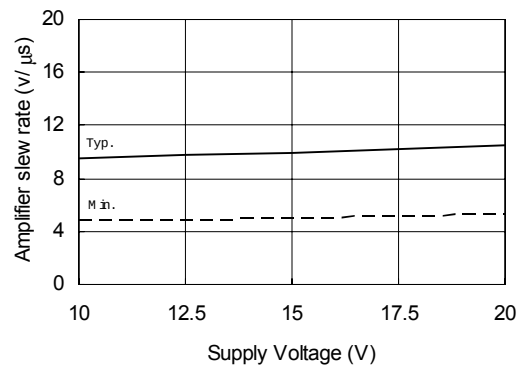


**Figure 15B. Amplifier slew rate (+)  
vs. Voltage**

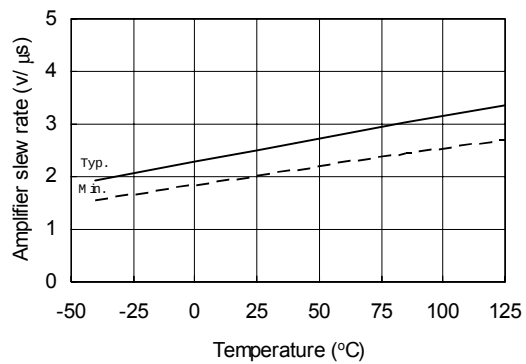


**Figure 16A. Amplifier slew rate (-)  
vs. Temperature**

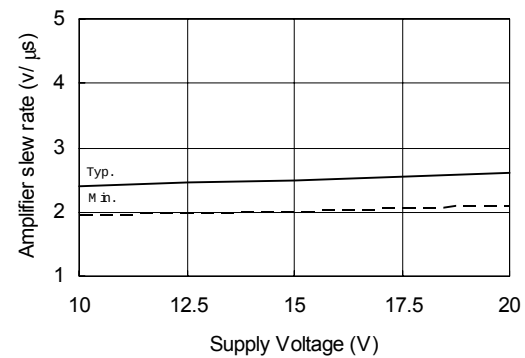


**Figure 16B. Amplifier slew rate (-)  
vs. Voltage**

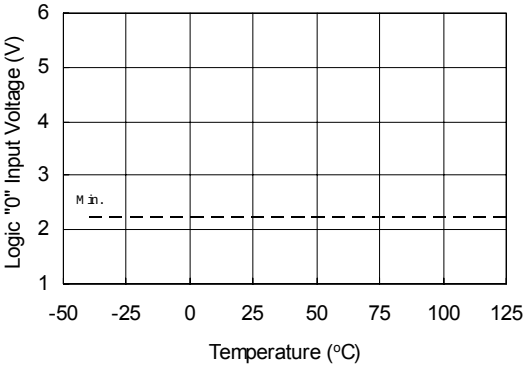


Figure 17A. Logic "0" Input Voltage (OUT=LO), Fault Clear Voltage vs. Temperature

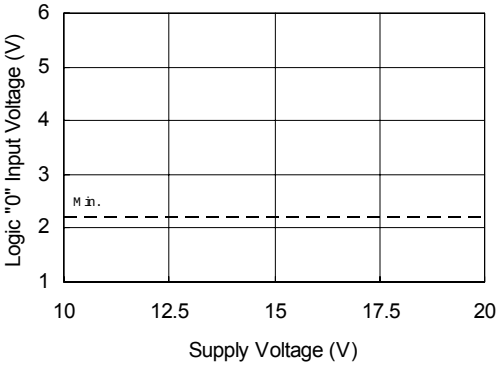


Figure 17B. Logic "0" Input Voltage (OUT=LO), Fault Clear Voltage vs. Voltage

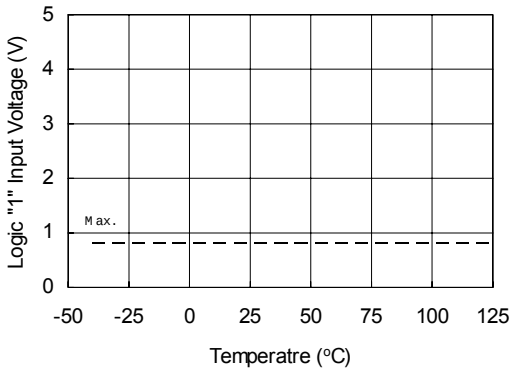


Figure 18A. Logic "1" Input (OUT=HI), Fault Clear Input Voltage vs. Temperature

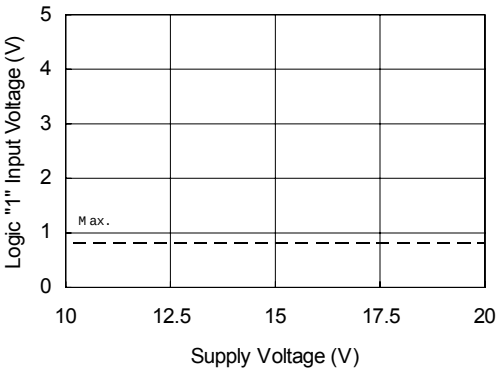


Figure 18B. Logic "1" Input (OUT=HI), Fault Clear Input Voltage vs. Voltage

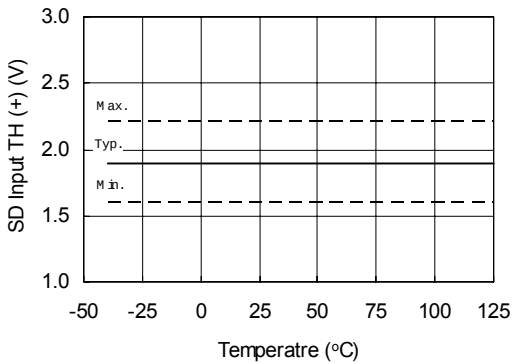


Figure 21A. SD Input TH(+) vs. Temperature

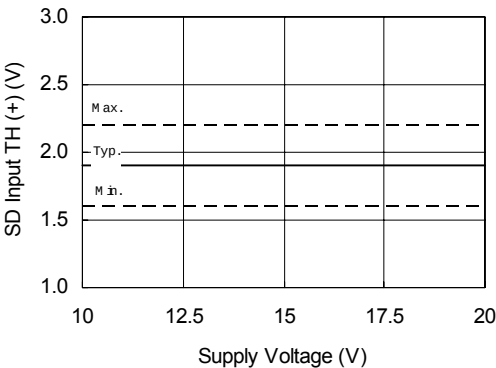


Figure 21B. SD Input TH(+) vs. Voltage

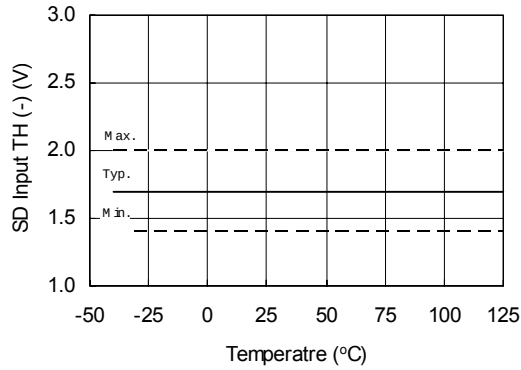


**Figure 22A. SD Input TH(-) vs. Temperature**

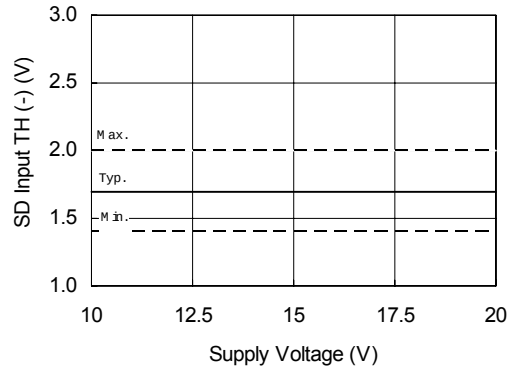


**Figure 22B. SD Input TH(-) vs. Voltage**

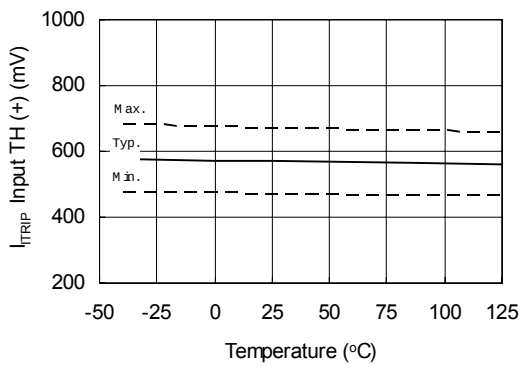


**Figure 23A.  $I_{TRIP}$  Input TH(+) vs. Temperature**

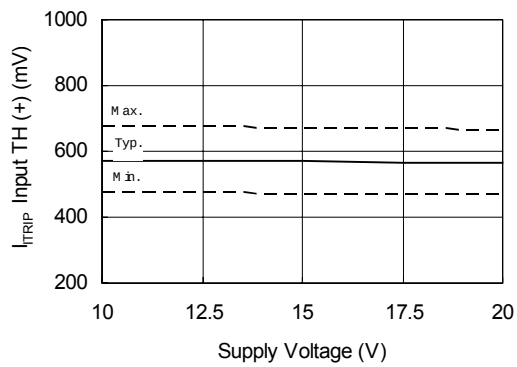


**Figure 23B.  $I_{TRIP}$  Input TH(+) vs. Voltage**

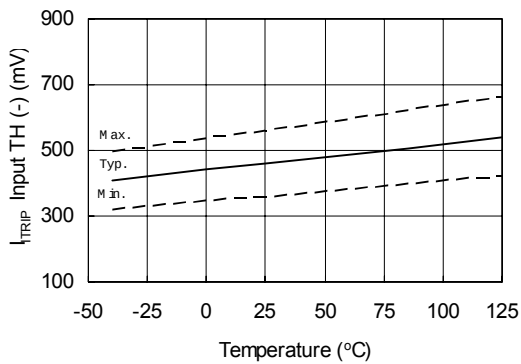


**Figure 24A.  $I_{TRIP}$  Input TH(-) vs. Temperature**

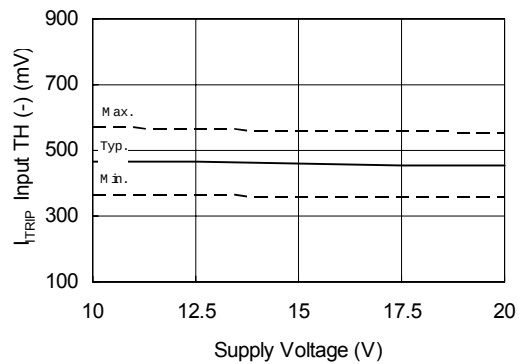


**Figure 24B.  $I_{TRIP}$  Input TH(-) vs. Voltage**

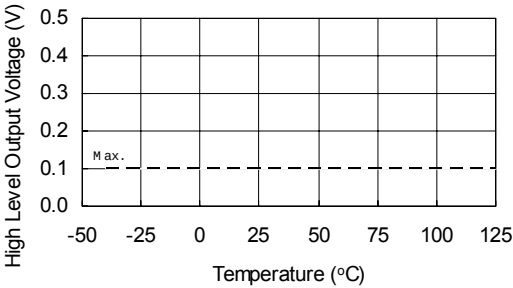


Figure 25A. High Level Output vs. Temperature

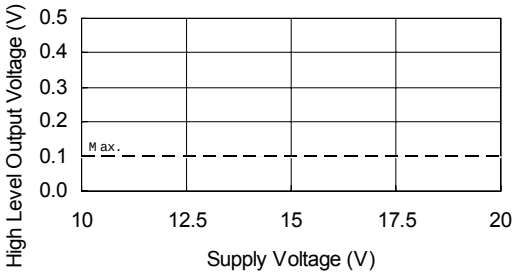


Figure 25B. High Level Output vs. Voltage

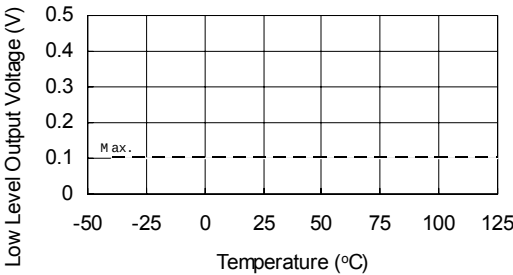


Figure 26A. Low Level Output vs. Temperature

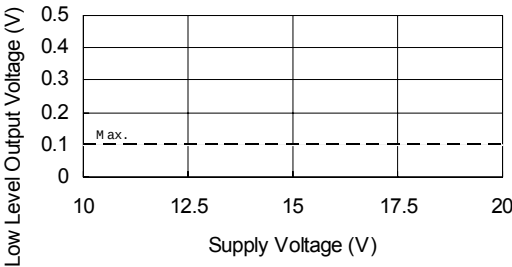


Figure 26B. Low Level Output vs. Voltage

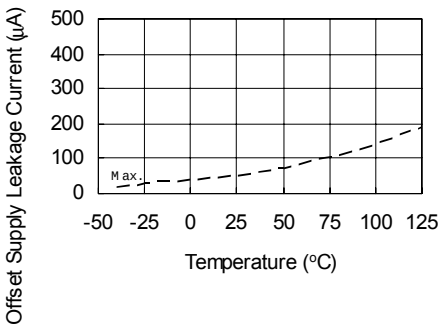


Figure 27A. Offset Supply Leakage Current vs. Temperature

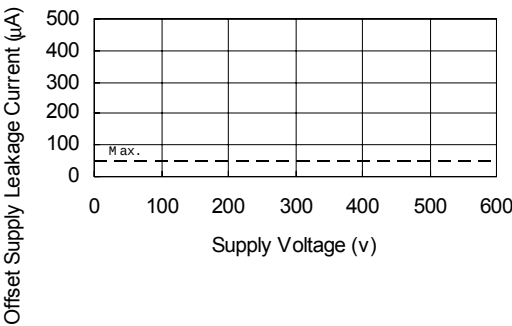


Figure 27B. Offset Supply Leakage Current vs. Voltage

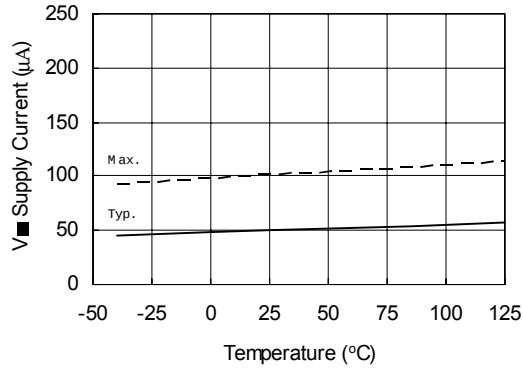


**Figure 28A.  $V_{BS}$  Supply Current vs. Temperature**

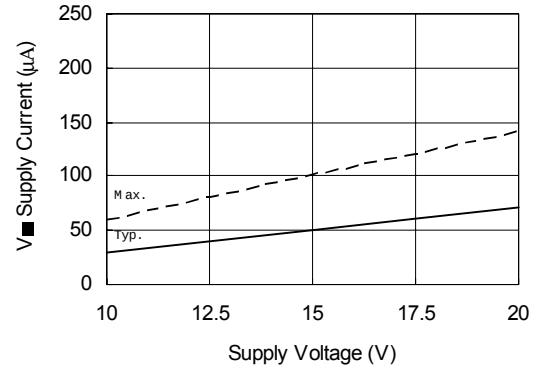


**Figure 28B.  $V_{BS}$  Supply Current vs. Voltage**

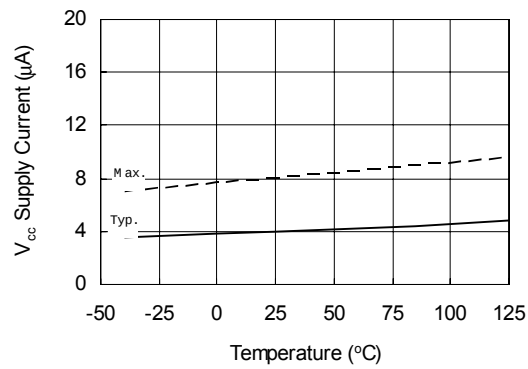


**Figure 29A.  $V_{CC}$  Supply Current vs. Temperature**

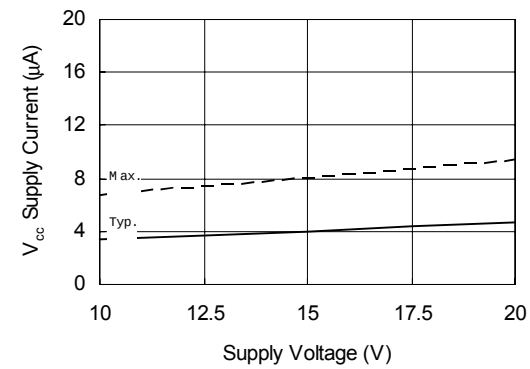


**Figure 29B.  $V_{CC}$  Supply Current vs. Voltage**

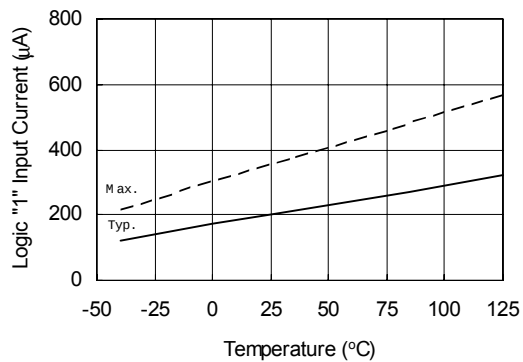


**Figure 30A. Logic "1" Input Bias Current vs. Temperature**

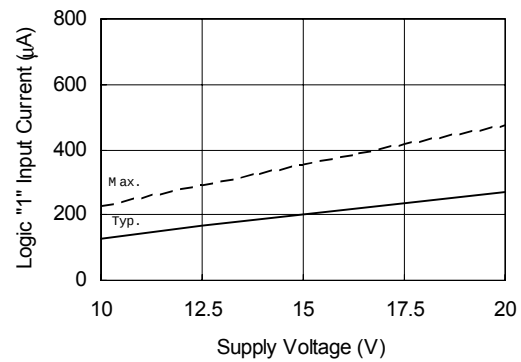


**Figure 30B. Logic "1" Input Bias Current vs. Voltage**

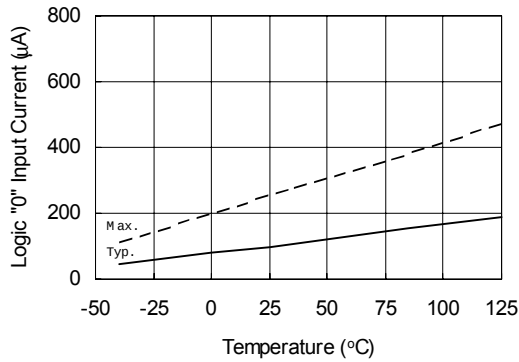


**Figure 31A. Logic "0" Input Bias Current vs. Temperature**

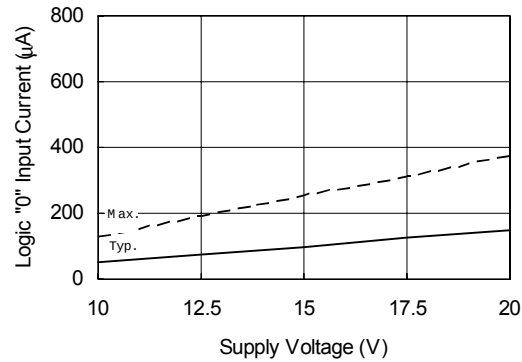


**Figure 31B. Logic "0" Input Bias Current vs. Supply Voltage**

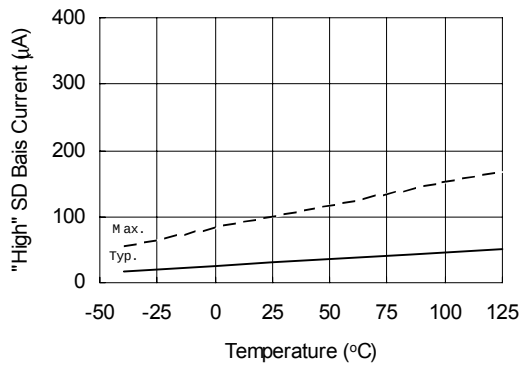


**Figure 32A. "High" Shutdown Bias Current vs. Temperature**

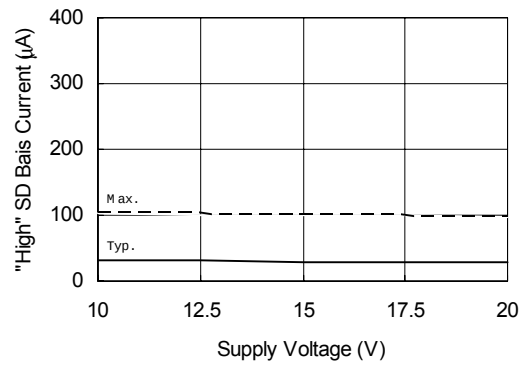


**Figure 32B. "High" Shutdown Bias Current vs. Supply Voltage**

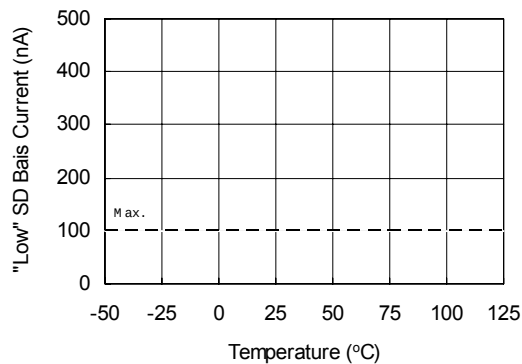


**Figure 33A. "Low" Shutdown Bias Current vs. Temperature**

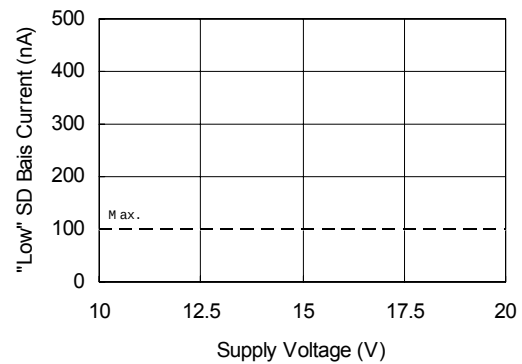


**Figure 33B. "Low" Shutdown Bias Current vs. Supply Voltage**

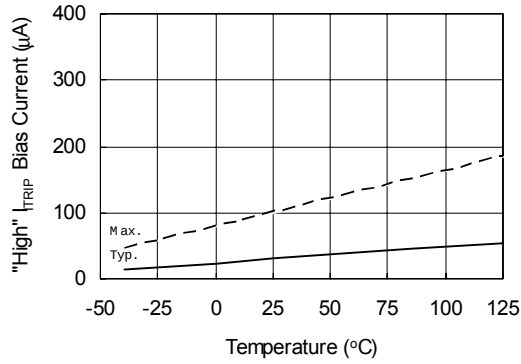


**Figure 34A. "High"  $I_{TRIP}$  Bias Current vs. Temperature**

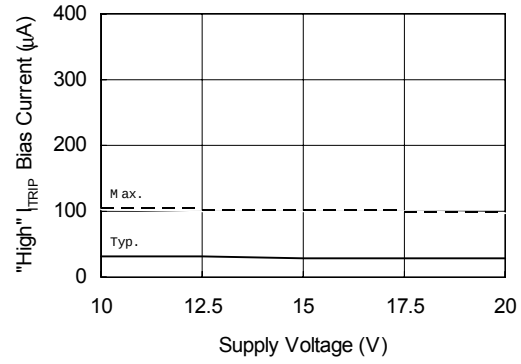


**Figure 34B. "High"  $I_{TRIP}$  Bias Current vs. Supply Voltage**

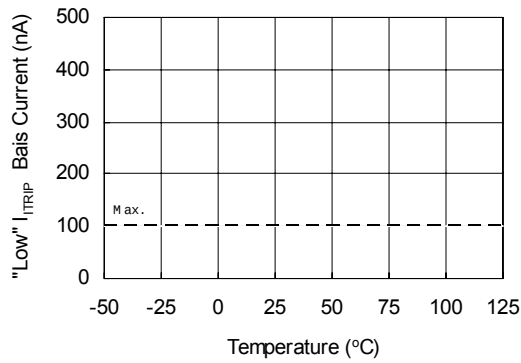


**Figure 35A. "Low"  $I_{TRIP}$  Bias Current vs. Temperature**

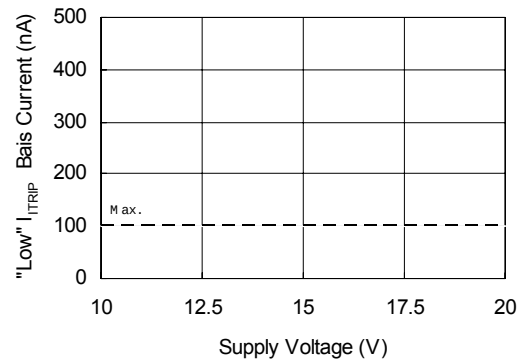


**Figure 35B. "Low"  $I_{TRIP}$  Bias Current vs. Supply Voltage**

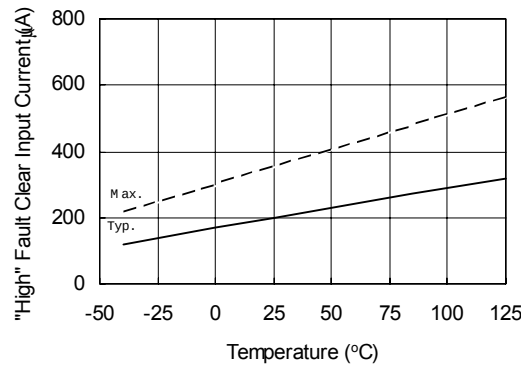


**Figure 36A. "High" Fault Clear Input Bias Current vs. Temperature**

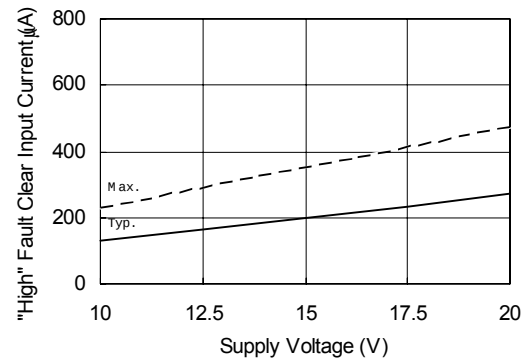


**Figure 36B. "High" Fault Clear Input Bias Current vs. Supply voltage**

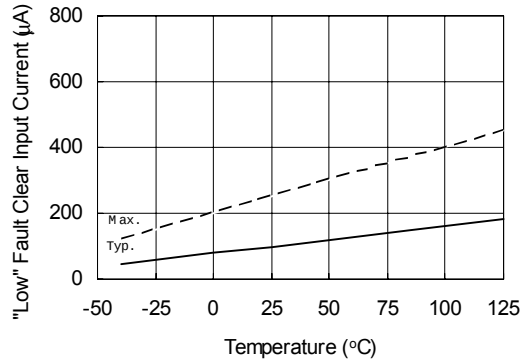


**Figure 37A. "Low" Fault Clear Input Bias Current vs. Temperature**

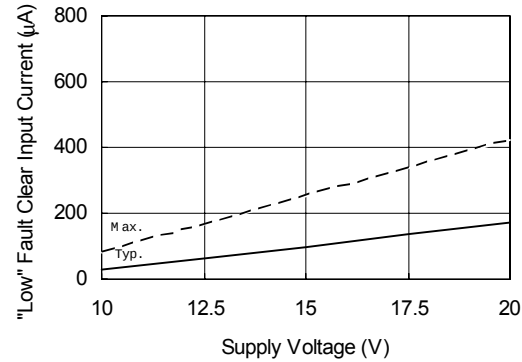


**Figure 37B. "Low" Fault Clear Input Bias Current vs. Supply Voltage**

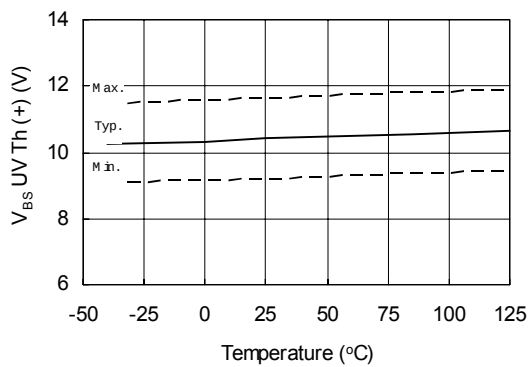


**Figure 38A. IR2135/IR2235  $V_{BS}$  Undervoltage Threshold (+) vs. Temperature**

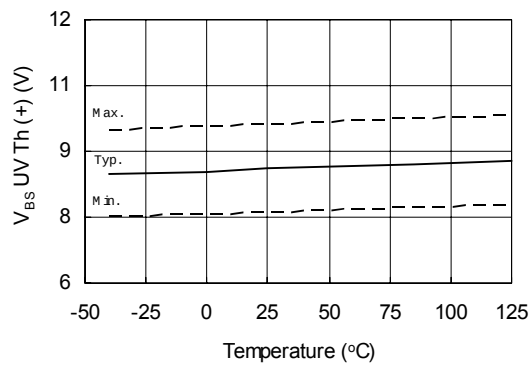


**Figure 38B. IR2133/IR2233  $V_{BS}$  Undervoltage Threshold (+) vs. Temperature**

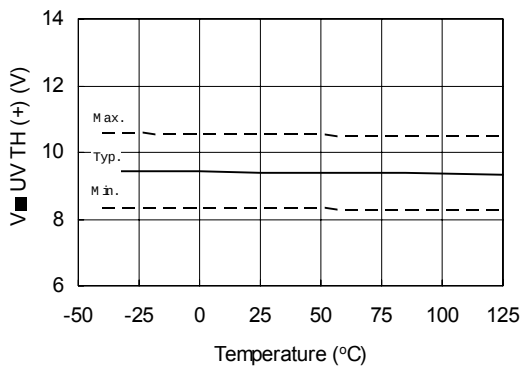


**Figure 39A. IR2135/IR2235  $V_{BS}$  Undervoltage Threshold (-) vs. Temperature**

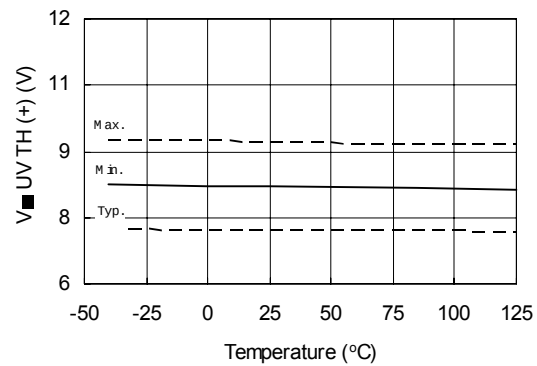


**Figure 39B. IR2133/IR2233  $V_{BS}$  Undervoltage Threshold (-) vs. Temperature**

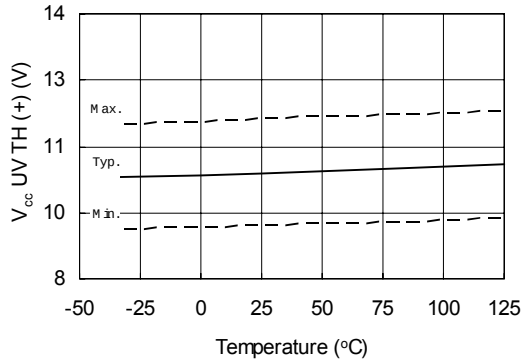


**Figure 40A. IR2135/IR2235  $V_{cc}$  Undervoltage Threshold (+) vs. Temperature**

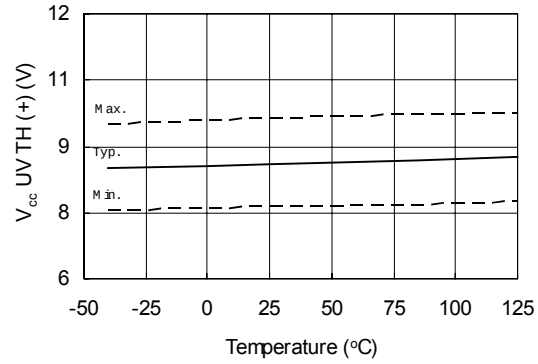


**Figure 40B. IR2133/IR2233  $V_{cc}$  Undervoltage Threshold (+) vs. Temperature**

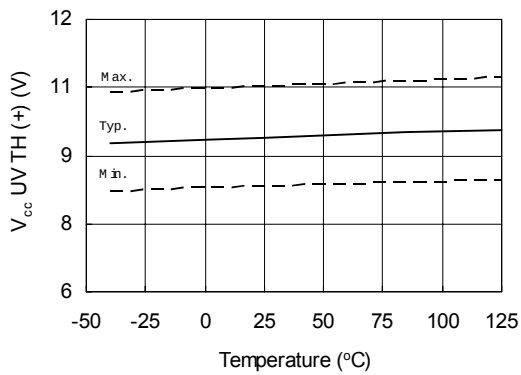


**Figure 41A. IR2135/IR2235  $V_{cc}$  Undervoltage Threshold (-) vs. Temperature**

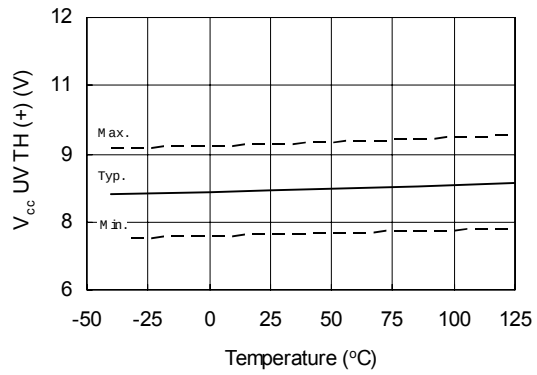


**Figure 41B. IR2133/IR2233  $V_{cc}$  Undervoltage Threshold (-) vs. Temperature**

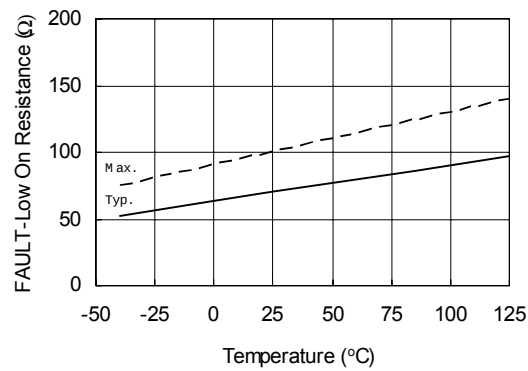


**Figure 42A. FAULT- Low On Resistance vs. Temperature**

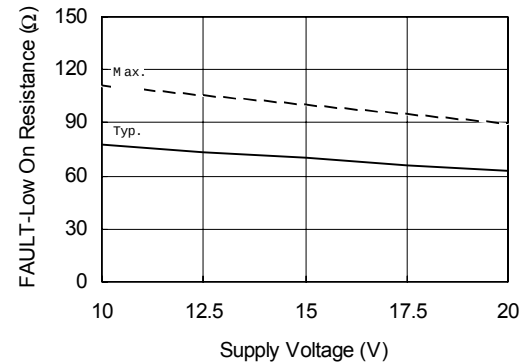


**Figure 42B. FAULT- Low On Resistance vs. Supply Voltage**

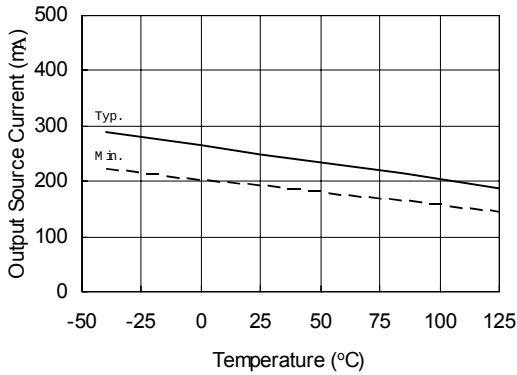


Figure 43A. Output Source Current vs. Temperature

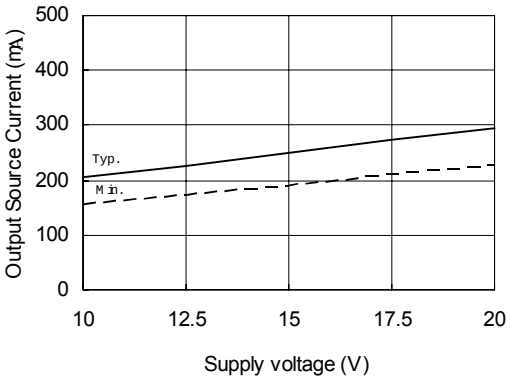


Figure 43B. Output Source Current vs. Supply Voltage

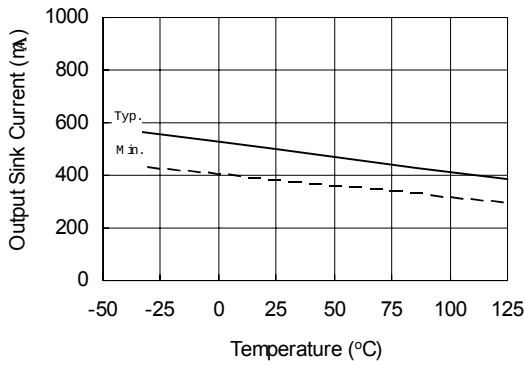


Figure 44A. Ourput Sink Current vs. Temperature

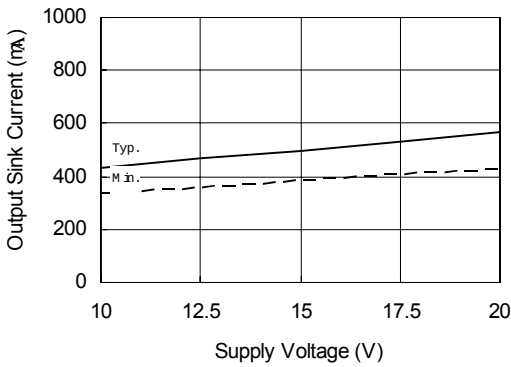


Figure 44B. Ourput Sink Current vs. Supply Voltage

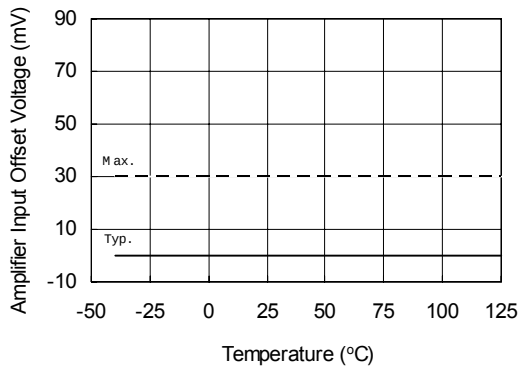


Figure 45A. Amplifier Input Offset Voltage vs. Temperature

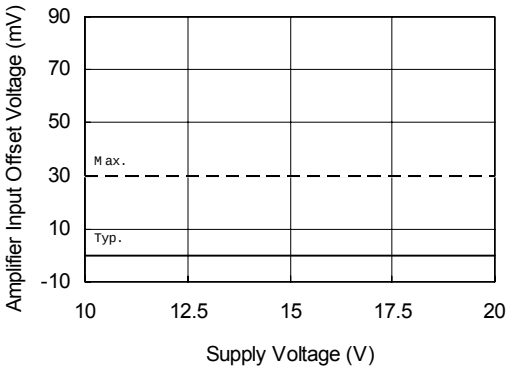


Figure 45B. Amplifier Input Offset Voltage vs. Supply Voltage

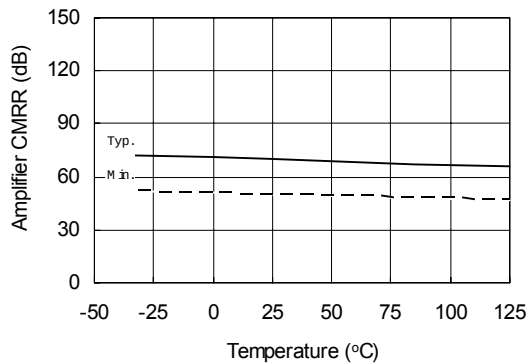


Figure 46A. Amplifier Common Mode Rejection Ratio vs. Temperature

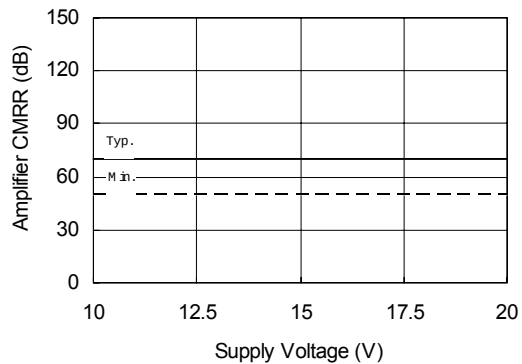


Figure 46B. Amplifier Common Mode Rejection Ratio vs. Supply Voltage

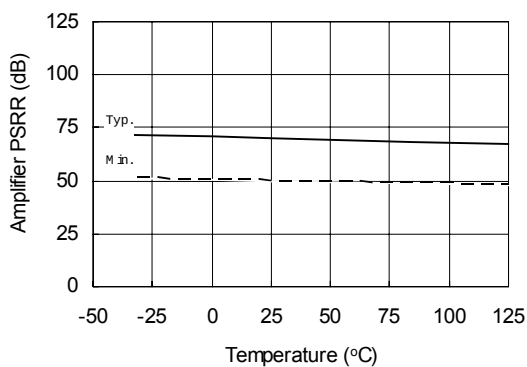


Figure 47A. Amplifier Power Supply Rejection Ratio vs. Temperature

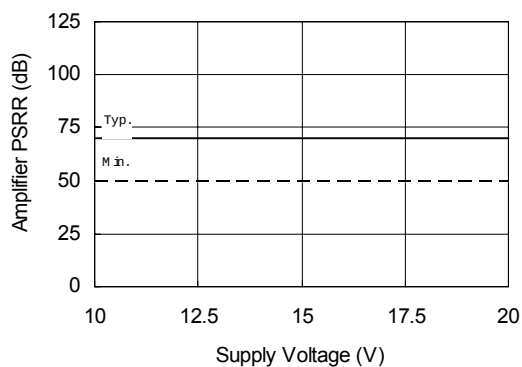


Figure 47B. Amplifier Power Supply Rejection Ratio vs. Supply Voltage

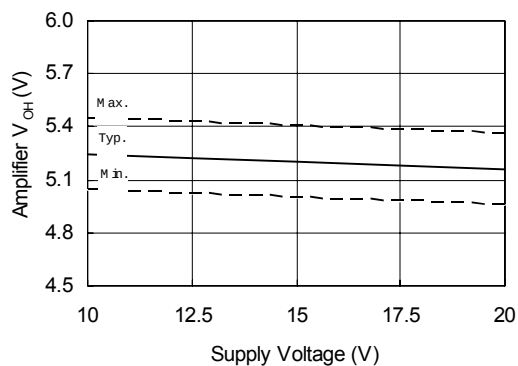


Figure 48. Amplifier High Level Output Voltage vs. Supply Voltage

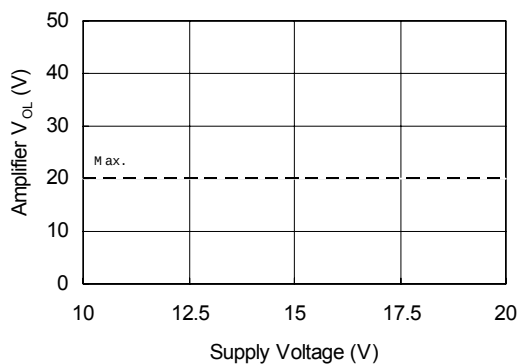


Figure 49. Amplifier Low Level Output Voltage vs. Supply Voltage

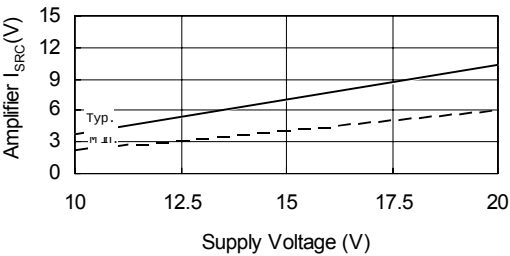


Figure 50. Amplifier Output Source Current vs. Supply Voltage

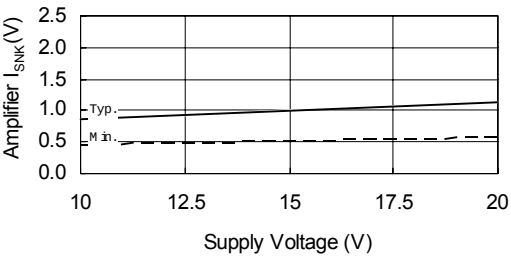


Figure 51. Amplifier Output Sink Current vs. Supply Voltage

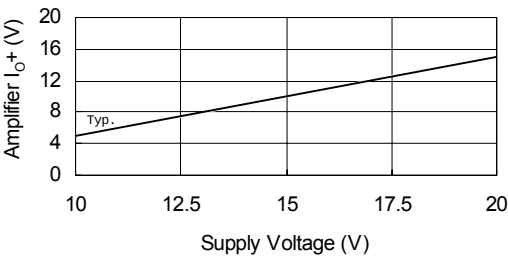


Figure 52. Amplifier Output High Short Circuit Current vs. Supply Voltage

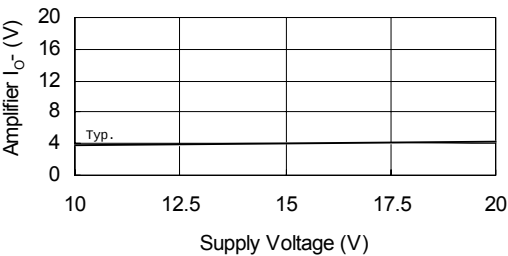


Figure 53. Amplifier Output Low Short Circuit Current vs. Supply Voltage

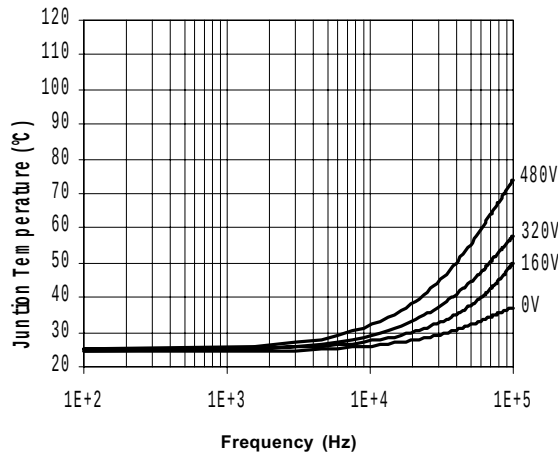


Figure 7. IR2133J Junction Temperature vs Frequency Driving (IRGPC20KD2) Rgate = 5.1Ω @ Vcc = 15V

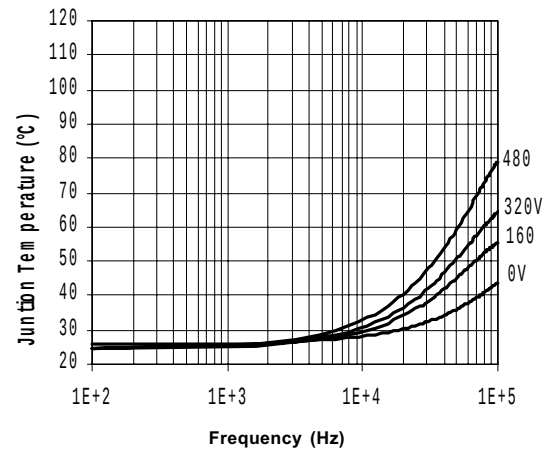


Figure 8. IR2133J Junction Temperature vs Frequency Driving (IRGPC30KD2) Rgate = 5.1Ω @ Vcc = 15V

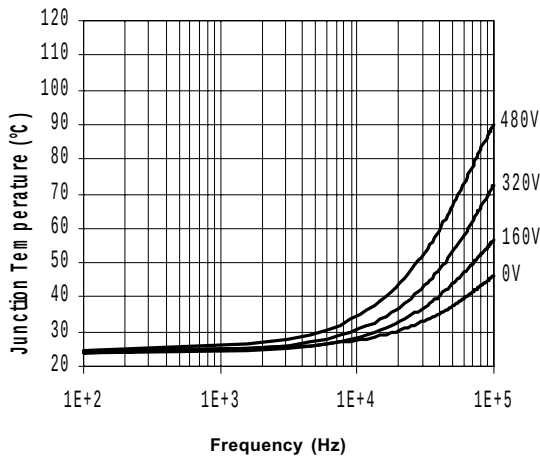


Figure 9. IR2133J Junction Temperature vs Frequency Driving (IRGPC40KD2) Rgate = 5.1Ω @ Vcc = 15V

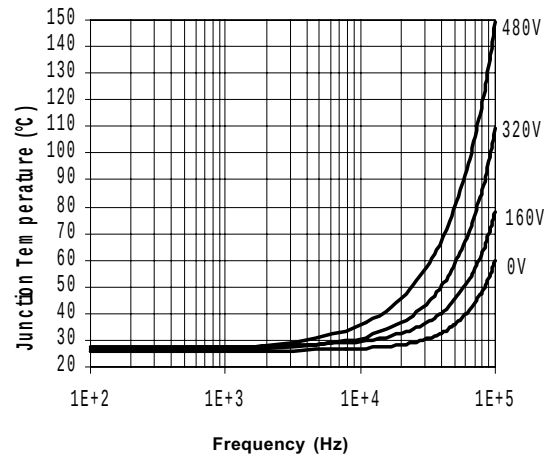


Figure 10. IR2133J Junction Temperature vs Frequency Driving (IRGPC50KD2) Rgate = 5.1Ω @ Vcc = 15V

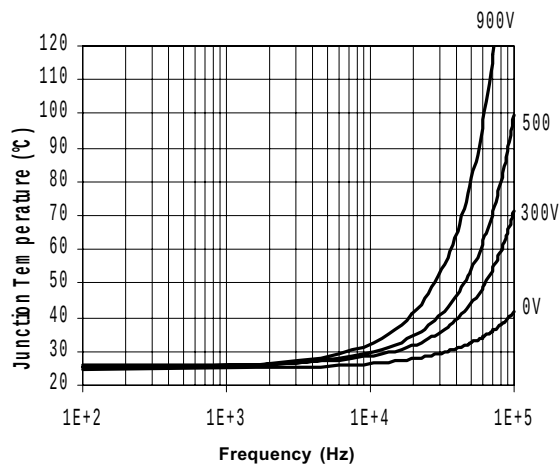


Figure 11. IR2233J Junction Temperature vs Frequency Driving (IRG4PH30KD)  $R_{gate} = 20\Omega$  @  $V_{cc} = 15V$

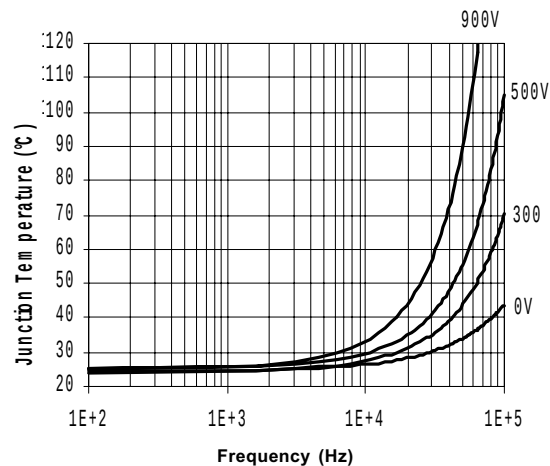


Figure 12. IR2233J Junction Temperature vs Frequency Driving (IRG4PH40KD)  $R_{gate} = 15\Omega$  @  $V_{cc} = 15V$

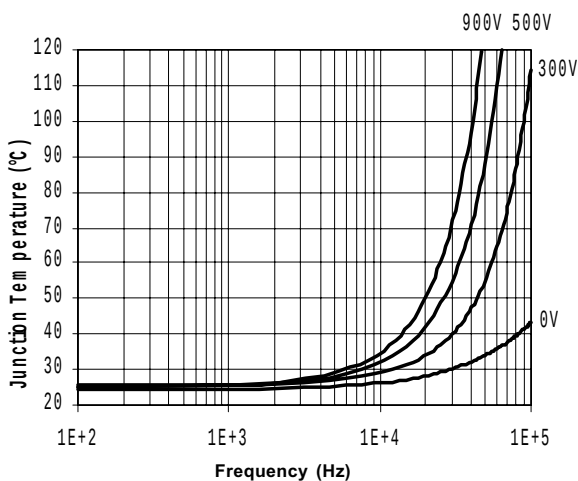


Figure 13. IR2233J Junction Temperature vs Frequency Driving (IRG4PH50KD)  $R_{gate} = 10\Omega$  @  $V_{cc} = 15V$

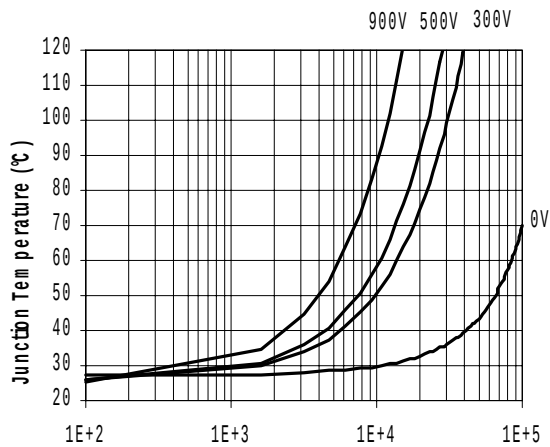
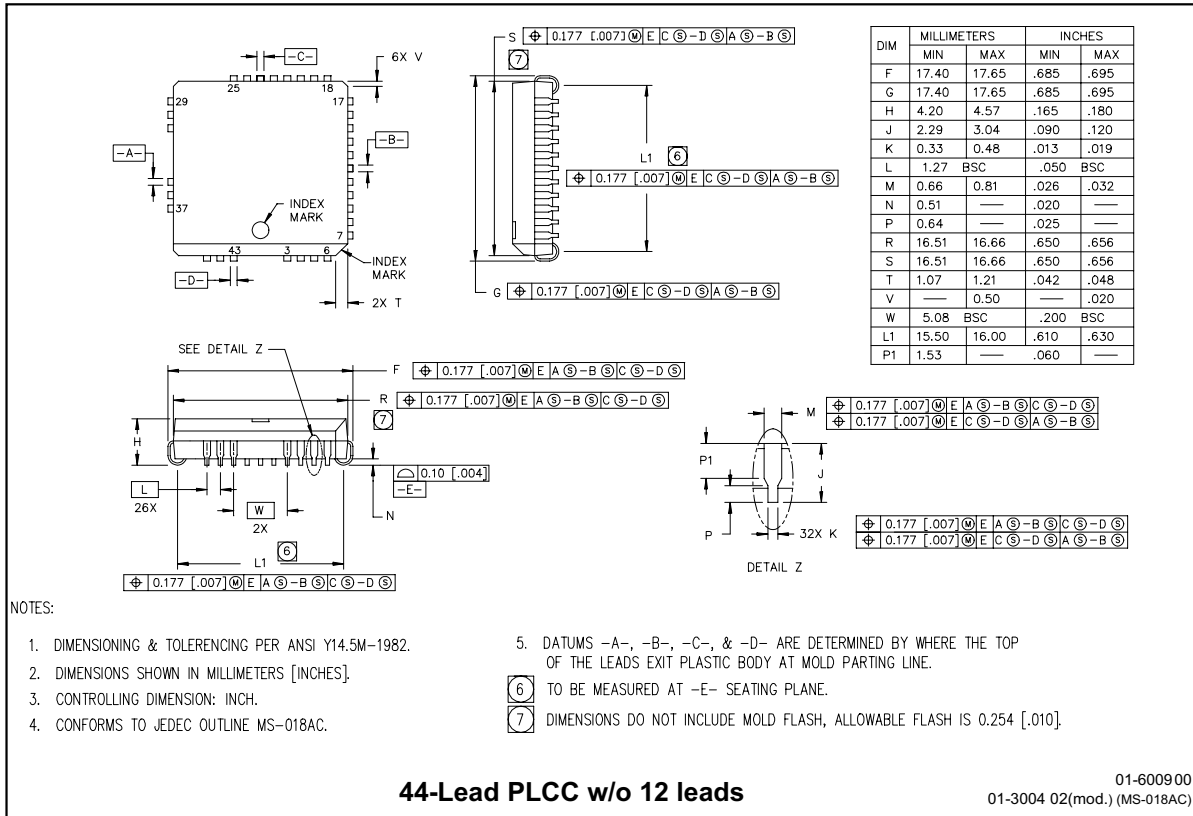


Figure 14. IR2233J Junction Temperature vs Frequency Driving (IRG4ZH71KD)  $R_{gate} = 5\Omega$  @  $V_{cc} = 15V$

[illegible]

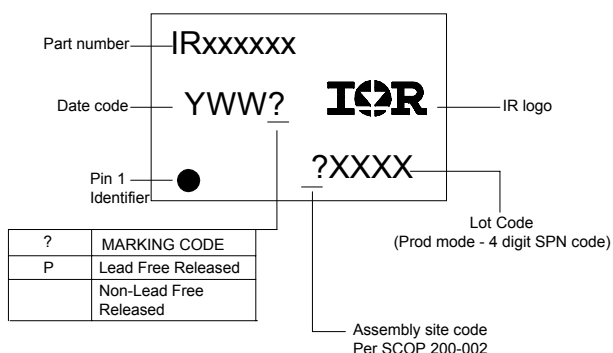
# IR2133/IR2135/IR2233/IR2235(J&S)&(PbF)

International  
**IR** Rectifier



## IR2133/IR2135/IR2233/IR2235(J&S)&(PbF)

### LEADFREE PART MARKING INFORMATION



### ORDER INFORMATION

#### Basic Part (Non-Lead Free)

|         |      |         |               |          |
|---------|------|---------|---------------|----------|
| 28-Lead | PDIP | IR2133  | order         | IR2133 2 |
| 8-Lead  | SOIC | IR2133S | order         | IR2133S  |
| 28-Lead | PDIP | IR2135  | order         | IR2135   |
| 28-Lead | SOIC | IR2135S | order         | IR2135S  |
| 28-Lead | PDIP | IR2233  | not available |          |
| 28-Lead | SOIC | IR2233S | order         | IR2233S  |
| 28-Lead | PDIP | IR2235  | not available |          |
| 28-Lead | SOIC | IR2235S | order         | IR2235S  |
| 44-Lead | PLCC | IR2133J | order         | IR2133J  |
| 44-Lead | PLCC | IR2135J | order         | IR2135J  |
| 44-Lead | PLCC | IR2233J | order         | IR2233J  |
| 44-Lead | PLCC | IR2235J | order         | IR2235J  |

#### Leadfree Part

|         |      |         |       |            |
|---------|------|---------|-------|------------|
| 28-Lead | PDIP | IR2133  | order | IR2133PbF  |
| 28-Lead | SOIC | IR2133S | order | IR2133SPbF |
| 28-Lead | PDIP | IR2135  | order | IR2135PbF  |
| 28-Lead | SOIC | IR2135S | order | IR2135SPbF |
| 28-Lead | PDIP | IR2233  | order | IR2233PbF  |
| 28-Lead | SOIC | IR2233S | order | IR2233SPbF |
| 28-Lead | PDIP | IR2235  | order | IR2235PbF  |
| 28-Lead | SOIC | IR2235S | order | IR2235SPbF |
| 44-Lead | PLCC | IR2133J | order | IR2133JPbF |
| 44-Lead | PLCC | IR2135J | order | IR2135JPbF |
| 44-Lead | PLCC | IR2233J | order | IR2233JPbF |
| 44-Lead | PLCC | IR2235J | order | IR2235JPbF |

## Данный компонент на территории Российской Федерации

**Вы можете приобрести в компании MosChip.**

Для оперативного оформления запроса Вам необходимо перейти по данной ссылке:

<http://moschip.ru/get-element>

Вы можете разместить у нас заказ для любого Вашего проекта, будь то серийное производство или разработка единичного прибора.

В нашем ассортименте представлены ведущие мировые производители активных и пассивных электронных компонентов.

Нашей специализацией является поставка электронной компонентной базы двойного назначения, продукции таких производителей как XILINX, Intel (ex.ALTERA), Vicor, Microchip, Texas Instruments, Analog Devices, Mini-Circuits, Amphenol, Glenair.

Сотрудничество с глобальными дистрибьюторами электронных компонентов, предоставляет возможность заказывать и получать с международных складов практически любой перечень компонентов в оптимальные для Вас сроки.

На всех этапах разработки и производства наши партнеры могут получить квалифицированную поддержку опытных инженеров.

Система менеджмента качества компании отвечает требованиям в соответствии с ГОСТ Р ИСО 9001, ГОСТ РВ 0015-002 и ЭС РД 009

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