2ED2304S06F

650 V Half Bridge Gate Driver with Integrated Bootstrap Diode

Feature list

- Infineon Thin-film-SOI-technology
- Fully operational to +650 V
- Floating channel designed for bootstrap operation
- Output source/sink current capability +0.36 A/-0.7 A
- Integrated Ultra-fast, low R_{DSON} Bootstrap Diode
- Tolerant to negative transient voltage up to -50 V (Pulse width is up 500 ns) given by SOI-technology
- 10 ns typ., 60 ns max. propagation delay matching
- dV/dt immune ±50 V
- Gate drive supply range from 10 V to 20 V
- Undervoltage lockout for both channels
- 3.3 V, 5 V and 15 V input logic compatible
- RoHS compliant

Product summary

- V_{OFFSET} = 670 V max.
- $I_{O+/-}$ (typ.) = 0.36 A/0.7 A
- V_{OUT} = 10 V - 17.5 V
- Delay Matching = 60 ns max.
- Internal deadtime = 75 ns
- $t_{on/off}$ (typ.) = 310 ns/300 ns

Package

DSO-8

Potential applications

- Motor drives, General purpose inverters
- Refrigeration compressors
- Half-bridge and full-bridge converters in offline AC-DC power supplies for telecom and lighting

Product validation

Qualified for industrial applications according to the relevant tests of JEDEC47/20/22.

Description

The 2ED2304S06F is a 650-V half-bridge gate driver. Its Infineon thin-film-SOI technology provides excellent ruggedness and noise immunity. The Schmitt trigger logic inputs are compatible with standard CMOS or LSTTL logic down to 3.3 V. The output drivers features a high pulse current buffer stage designed for minimum driver cross-conduction. The floating channel can be used to drive an N-channel power MOSFET or IGBT in the high side configuration which operates up to 650 V. Additionally, the offline clamping function provides an inherent protection of the parasitic turn-on by floating gate conditions when IC is not supplied.

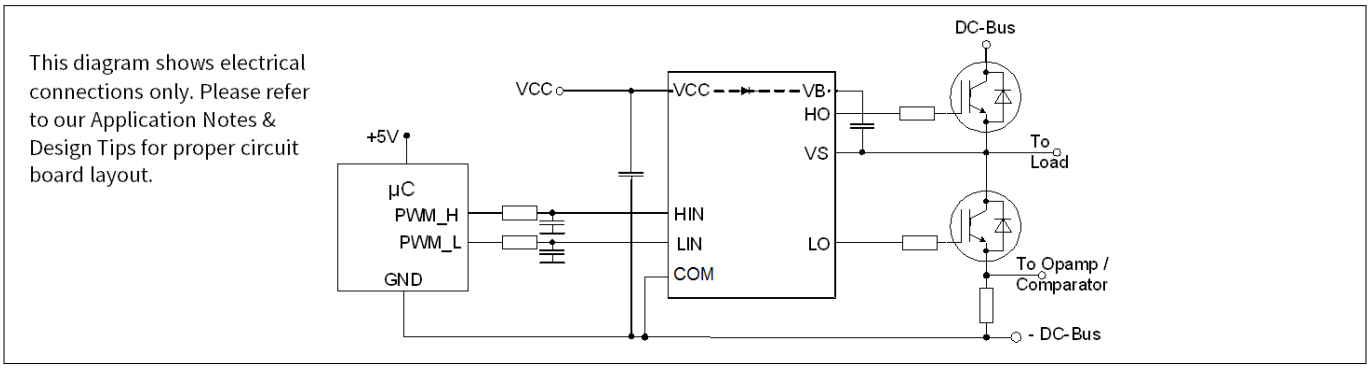


Figure 1 Typical connection diagram

Device information

Base Part Number	Package Type	Standard Pack		Orderable Part Number
		Form	Quantity	
2ED2304S06F	DSO-8	Tube/Bulk	95	2ED2304S06FXLSA1
		Tape and Reel	2500	2ED2304S06FXUMA1

Table of contents

1 Block diagram

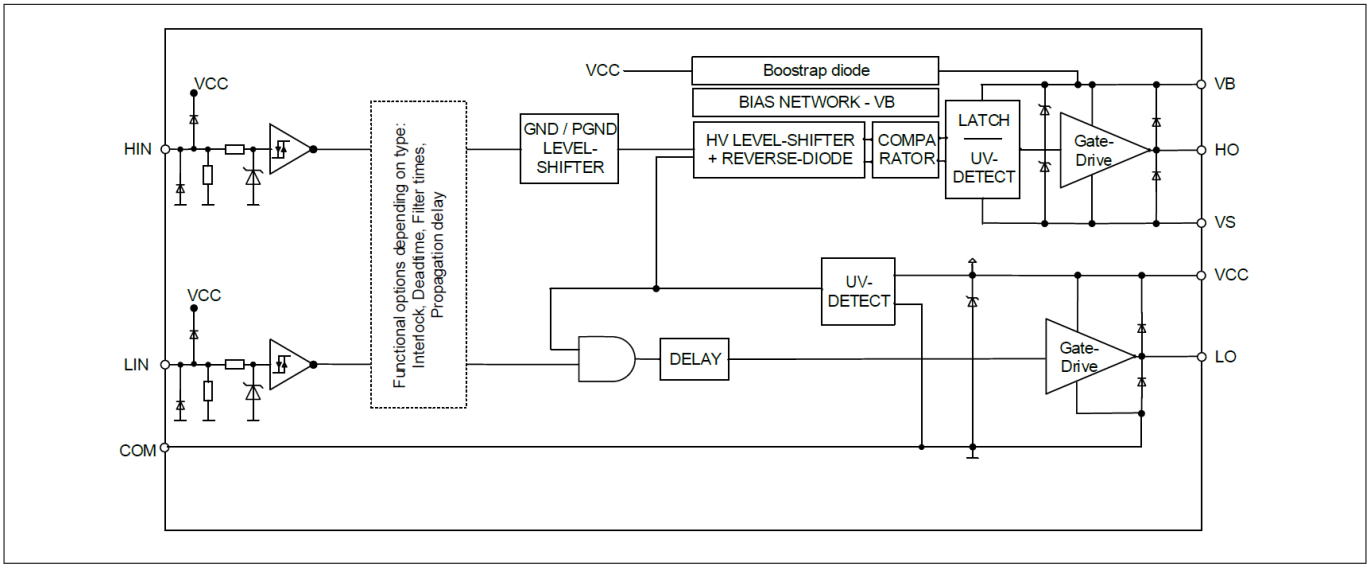


Figure 2 Functional block diagram

2 Lead definitions

Table 1 2ED2304S06F lead definitions

Pin	Symbol	Description
1	LIN	Logic input for low-side gate driver output (LO), in phase. Schmitt trigger inputs with hysteresis and pull down
2	HIN	Logic input for high-side gate driver output (HO), in phase. Schmitt trigger inputs with hysteresis and pull down
3	VCC	Low-side and logic supply voltage
4	COM	Low-side gate drive return
5	LO	Low-side driver output
6	VS	High voltage floating supply return
7	HO	High-side driver output
8	VB	High-side gate drive floating supply

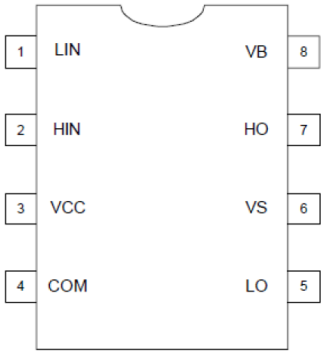


Figure 3 2ED2304S06F lead assignments (DSO-8)

3 Absolute maximum ratings

Table 2 Absolute maximum ratings

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM unless otherwise stated in the table. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.

Parameter	Symbol	Values		Unit	Note or Test Condition
		Min.	Max.		
High side floating offset voltage	V_B	V_{CC} – 6	670	V	[1]
		V_{CC} - 50	–	V	t_p < 500 ns [1]
High side floating offset voltage	V_S	V_{CC} - V_{BS} - 6	650	V	–
		V_{CC} - V_{BS} - 50	–	V	t_p < 500 ns [1]
High side floating output voltage	V_{HO}	V_S - 0.5	V_B + 0.5	V	–
Floating gate drive voltage supply voltage	V_{BS}	-1	20	V	
Low side supply voltage	V_{CC}	-1	20	V	–
Low-side output voltage	V_{LO}	-0.5	V_{CC} + 0.5	V	–
Logic input voltage	V_{IN}	-0.5	V_{CC} - 0.5	V	–
Allowable V_S offset supply transient relative to COM	dV_S/dt	–	50	V/ns	[2]
Package power dissipation	P_D	–	0.6	W	@ $T_A \leq +25$ °C
Thermal resistance, junction to ambient	R_{thJA}	–	195	°C/W	–
Junction temperature	T_J	–	150	°C	–
Storage temperature	T_S	-40	150	°C	–
Lead temperature	T_L	–	300	°C	soldering, 10 seconds

1 In case $V_{CC} > V_B$ there is an additional power dissipation in the internal bootstrap diode between pins V_{CC} and V_B in case of activated bootstrap diode. Insensivity to negative transient not subject to production test. Verified by design/characterization.

2 Not subject to production test, verified by characterization

4 Recommended operating conditions

Table 3 Recommended operating conditions

For proper operation, the device should be used within the recommended conditions. All voltage parameters are absolute voltages referenced to COM unless otherwise stated in the table. The offset rating is tested with supplies of (V_{CC} - COM) = (V_B - V_S) = 15 V.

Parameter	Symbol	Values		Unit	Note or Test Condition
		Min.	Max.		
High side floating well supply voltage	V_B	V_S + 10	V_S + 17.5	V	–
High side floating well supply offset voltage	V_S	V_{CC} - V_{BS} - 1	650	V	1)
Floating gate drive output voltage	V_{HO}	10	V_{BS}	V	–
High-side supply voltage	V_{BS}	10	17.5	V	
Low-side supply voltage	V_{CC}	10	17.5	V	–
Low side output voltage	V_{LO}	0	V_{CC}	V	–
Logic input voltage	V_{IN}	0	V_{CC}	V	2)
Ambient temperature	T_A	-40	125	°C	–
Pulse width for ON and OFF	t_{IN}	0.3	–	µs	3)

1 Logic operation for V_S of -8 V to +600 V
2 All input pins (HIN, LIN) are internally clamped
3 Input pulses may not be transmitted properly in case of LIN/HIN below 0.3 µs

5 Electrical characteristics

5.1 Static electrical characteristics

Table 4 Static electrical characteristics

(V_{CC} – COM) = (V_B – V_S) = 15 V, and T_A = 25 °C unless otherwise specified. The V_{IL}, V_{IH} and I_{IN} parameters are referenced to COM and are applicable to the respective input pins: HIN and LIN. The V_O and I_O parameters are referenced to COM/VS and are applicable to the respective output leads HO or LO. The V_{CCUV} parameters are referenced to COM. The V_{BSUV} parameters are referenced to V_S.

Parameter	Symbol	Values			Unit	Note or test condition
		Min.	Typ.	Max.		
V_{BS} supply undervoltage positive going threshold	V_{BSUV+}	8.3	9.1	9.9	V	–
V_{BS} supply undervoltage negative going threshold	V_{BSUV-}	7.5	8.3	9.0	V	–
V_{BS} supply undervoltage hysteresis	V_{BSUVHY}	0.5	0.9	–	V	–
V_{CC} supply undervoltage positive going threshold	V_{CCUV+}	8.3	9.1	9.9	V	–
V_{CC} supply undervoltage negative going threshold	V_{CCUV-}	7.5	8.3	9.0	V	–
V_{CC} supply undervoltage hysteresis	V_{CCUVHY}	0.5	0.9	–	V	–
High-side floating well offset supply leakage	I_{LK}	–	1	12.5	µA	V_B = V_S = 600 V
		–	10	–	µA	[1] T_J = 125 °C, V_S = 600 V
Quiescent V_{BS} supply current	I_{QBS}	–	170	300	µA	–
Quiescent V_{CC} supply current	I_{QCC}	–	300	600	µA	–
High level output voltage drop, V_{BIAS} - V_O	V_{OH}	–	0.45	1	V	I_O = 20 mA
Low level output voltage drop, V_O	V_{OL}	–	0.13	0.3	V	I_O = 20 mA
Peak output current turn-on	I_{o+}	–	360	–	mA	[1] V_O = 0 V, PW ≤ 10 µs
Mean output current from 3 V (20%) to 6 V (40%)	I_{o+mean}	180	230	–	mA	C_L = 22 nF
Peak output current turn-off	I_{o-}	–	700	–	mA	[1] V_O = 15 V, PW ≤ 10 µs
Mean output current from 12 V (80%) to 9 V (60%)	I_{o-mean}	390	480	–	mA	C_L = 22 nF
Logic “1” input voltage	V_{IH}	1.7	2.1	2.4	V	–
Logic “0” input voltage	V_{IL}	0.7	0.9	1.1	V	–
Input bias current (HO = High)	I_{IN+}	15	35	60	µA	V_{IN} = 3.3 V
Input bias current (HO = Low)	I_{IN-}	–	0	–	µA	V_{IN} = 0 V
Bootstrap diode forward voltage between V_{CC} and V_B	V_{FBSD}	–	1	1.2	V	I_F = 0.3 mA
Bootstrap diode forward current between V_{CC} and V_B	I_{FBSD}	30	55	80	mA	V_{CC} - V_B = 4 V

1 Not subject of production test, verified by characterization

Table 4 Static electrical characteristics (continued)

(V_{CC} – COM) = (V_B – V_S) = 15 V, and T_A = 25 °C unless otherwise specified. The V_{IL}, V_{IH} and I_{IN} parameters are referenced to COM and are applicable to the respective input pins: HIN and LIN. The V_O and I_O parameters are referenced to COM/VS and are applicable to the respective output leads HO or LO. The V_{CCUV} parameters are referenced to COM. The V_{BSUV} parameters are referenced to V_S.

Parameter	Symbol	Values			Unit	Note or test condition
		Min.	Typ.	Max.		
Bootstrap diode resistance	R_{BSD}	20	36	55	Ω	V_{F1} = 4 V, V_{F2} = 5 V

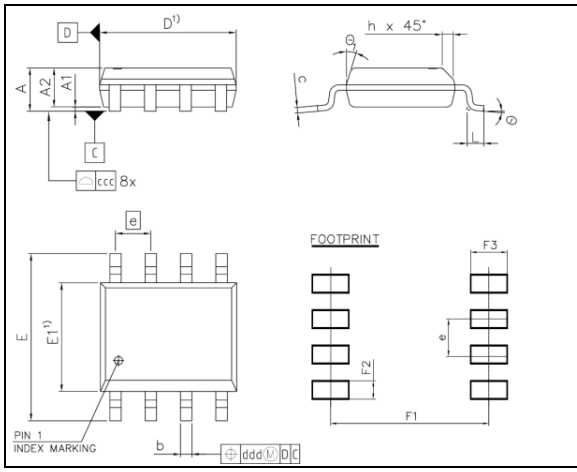
5.2 Dynamic electrical characteristics

Table 5 Dynamic electrical characteristics

V_{CC} = V_{BS} = 15 V, V_{SS} = COM, T_A = 25°C and *CL* = 1000 pF unless otherwise specified.

Parameter	Symbol	Values			Unit	Note or test condition
		Min.	Typ.	Max.		
Turn-on propagation delay	t_{on}	210	310	460	ns	$V_{LIN/HIN}$ = 0 or 3.3 V
Turn-off propagation delay	t_{off}	200	300	440	ns	$V_{LIN/HIN}$ = 0 or 3.3 V
Turn-on rise time	t_r	–	48	80	ns	$V_{LIN/HIN}$ = 0 or 3.3 V C_L = 1 nF
Turn-off fall time	t_f	–	24	40	ns	$V_{LIN/HIN}$ = 0 or 3.3 V C_L = 1 nF
Input filter time	t_{FILIN}	100	150	250	ns	$V_{LIN/HIN}$ 0 & 3.3 V
Delay matching time (HS & LS turn-on/off)	MT	–	10	60	ns	ext. dead time > 500 ns
Dead time	DT	30	75	140	ns	$V_{LIN/HIN}$ 0 & 3.3 V
Dead time matching time	MDT	–	10	50	ns	ext. dead time 0 ns

6 Package information DSO-8



1) DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	-	1.75	-	0.069
A1	0.10	-	0.004	-
A2	1.25	1.65	0.049	0.065
b	0.35	0.51	0.014	0.020
c	0.17	0.25	0.007	0.010
D	4.80	5.00	0.189	0.197
E	5.80	6.20	0.228	0.244
E1	3.80	4.00	0.150	0.157
e	1.27		0.050	
N	8		8	
L	0.39	0.89	0.015	0.035
h	0.23	0.50	0.009	0.020
Θ	0°	8°	0°	8°
Θ1	-	19°	-	19°
ccc	0.10		0.004	
ddd	0.25		0.010	
F1	5.59	5.79	0.220	0.228
F2	0.55	0.75	0.022	0.030
F3	1.21	1.41	0.048	0.056

Max. reflow solder temperature: 265 °C acc. JEDEC
Max. wave solder temperature: 245 °C acc. JEDEC

Figure 4 Package outline PG-DSO-8

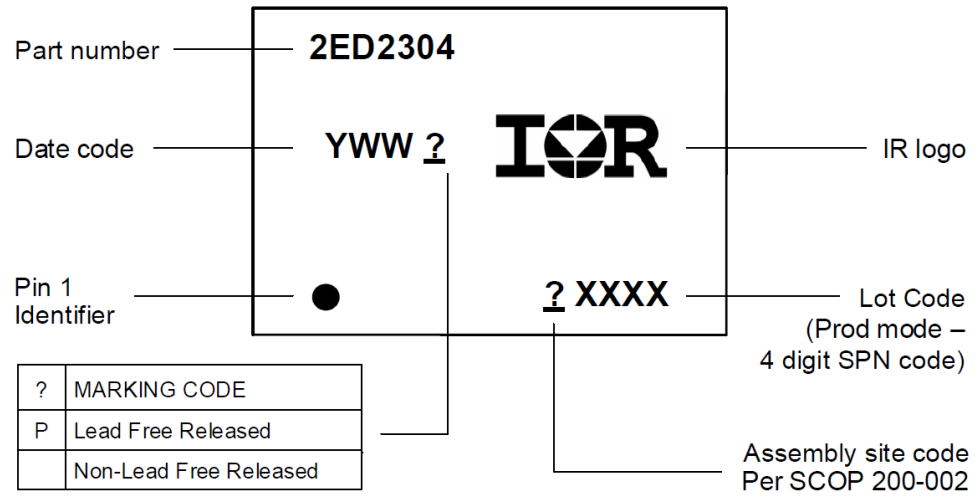
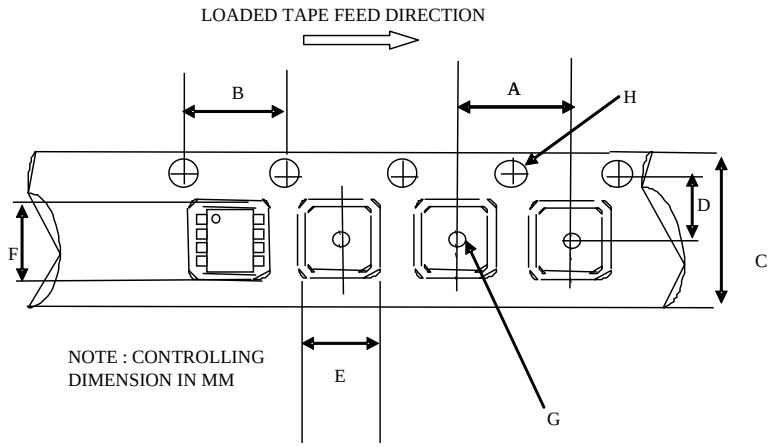


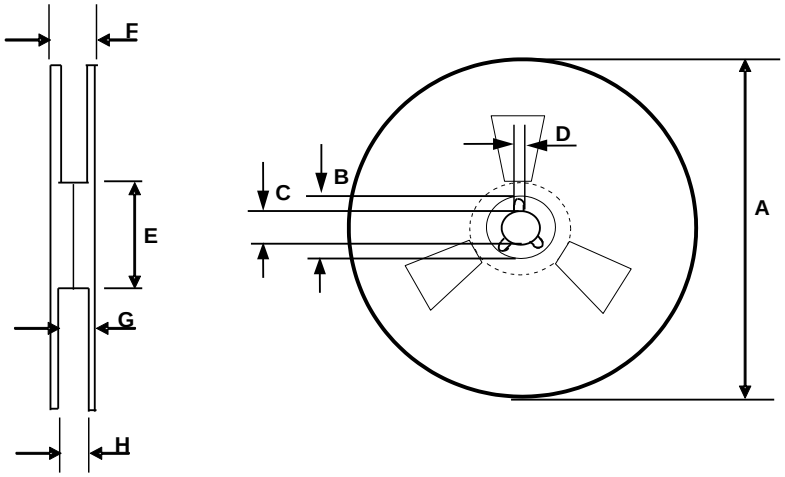
Figure 5 Marking information PG-DSO-8 (2ED2304S06F)

Package information DSO-8



CARRIER TAPE DIMENSION FOR 8SOICN

	Metric		Imperial	
Code	Min	Max	Min	Max
A	7.90	8.10	0.311	0.318
B	3.90	4.10	0.153	0.161
C	11.70	12.30	0.46	0.484
D	5.45	5.55	0.214	0.218
E	6.30	6.50	0.248	0.255
F	5.10	5.30	0.200	0.208
G	1.50	n/a	0.059	n/a
H	1.50	1.60	0.059	0.062



REEL DIMENSIONS FOR 8SOICN

	Metric		Imperial	
Code	Min	Max	Min	Max
A	329.60	330.25	12.976	13.001
B	20.95	21.45	0.824	0.844
C	12.80	13.20	0.503	0.519
D	1.95	2.45	0.767	0.096
E	98.00	102.00	3.858	4.015
F	n/a	18.40	n/a	0.724
G	14.50	17.10	0.570	0.673
H	12.40	14.40	0.488	0.566

Figure 6 Tape and reel details PG-DSO-8

7 Qualification information

Table 6 Qualification information [1)]

Qualification Level		Industrial [2)] *Note: This family of ICs has passed JEDEC's Industrial qualification. Consumer qualification level is granted by extension of the higher Industrial level.*	
Moisture Sensitivity Level		DSO-8	MSL2 [3)], 250 °C (per IPC/JEDEC J-STD-020)
ESD	Human Body Model	Class 1C (>1.5 kV) (per JEDEC standard JESD22-A114)	
	Charged Device Model	Class C3 (> 1.0 kV) (per JESD22-C101)	
IC Latch-Up Test		Class II Level A (per JESD85)	
RoHS Compliant		Yes	

1 Qualification standards can be found at Infineon's web site ***www.infineon.com***
2 Higher qualification ratings may be available should the user have such requirements. Please contact your Infineon sales representative for further information.
3 Higher MSL ratings may be available for the specific package types listed here. Please contact your Infineon sales representative for further information.

8 Related products

Table 7 Related products

Product	Description
Gate Driver ICs	
6EDL04I06 / 6EDL04N06	600 V, 3 phase level shift thin-film SOI gate driver with integrated high speed, low R_{DSON} bootstrap diodes with over-current protection (OCP), 240/420 mA source/sink current drive, Fault reporting, and Enable for MOSFET or IGBT switches.
2EDL23I06 / 2EDL23N06	600 V, Half-bridge thin-film SOI level shift gate driver with integrated high speed, low R_{DSON} bootstrap diode, with over-current protection (OCP), 2.3/2.8 A source/sink current driver, and one pin Enable/Fault function for MOSFET or IGBT switches.
Power Switches	
IKD04N60R / RF	600 V TRENCHSTOP™ IGBT with integrated diode in PG-TO252-3 package
IKD06N65ET6	650 V TRENCHSTOP™ IGBT with integrated diode in DPAK
IPD65R950CFD	650 V CoolMOS CFD2 with integrated fast body diode in DPAK
IPN50R950CE	500 V CoolMOS CE Superjunction MOSFET in PG-SOT223 package
iMOTION™ Controllers	
IRMCK099	iMOTION™ Motor control IC for variable speed drives utilizing sensor-less Field Oriented Control (FOC) for Permanent Magnet Synchronous Motors (PMSM).
IMC101T	High performance Motor Control IC for variable speed drives based on field oriented control (FOC) of permanent magnet synchronous motors (PMSM).

Revision history

Document version	Date of release	Description of changes
1.0	2016-07-12	Preliminary datasheet
2.0	2018-02-07	First Release Version
2.1	2018-07-13	Updated the marking information
2.11	2018-09-12	Deleting typo

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