



N- and P-Channel 20 V (D-S) MOSFET

PRODUCT SUMMARY						
	V _{DS} (V)	$R_{DS(on)}(\Omega)$	I _D (A) ^a	Q _g (Typ.)		
N-Channel	20	0.058 at $V_{GS} = 4.5 \text{ V}$	3.9	2.9 nC		
N-Chamile	20	0.078 at $V_{GS} = 2.5 \text{ V}$	3.3	2.9110		
P-Channel	- 20	0.195 at $V_{GS} = -4.5 \text{ V}$	- 2.1	1.6 nC		
r-Chamber	- 20	0.316 at $V_{GS} = -2.5$ V	- 1.7	1.0110		

TSOP-6

FEATURES

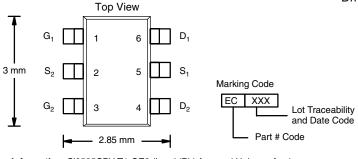
- Halogen-free According to IEC 61249-2-21 Definition
- TrenchFET® Power MOSFETs
- 100 % R_g Tested
 - Compliant to RoHS Directive 2002/95/EC

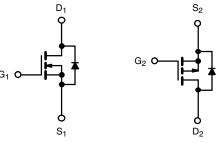


HALOGEN FREE

APPLICATIONS

- Load Switch for Portable Devices
- DC/DC Converters
- Drivers: Motor, Solenoid, Relay





N-Channel MOSFET

P-Channel MOSFET

Ordering Information: Si3585CDV-T1-GE3 (Lead (Pb)-free and Halogen-free)

ABSOLUTE MAXIMUM RATINGS	(T _A = 25 °C, unle	ess otherwise	e noted)		
Parameter	Symbol	N-Channel	P-Channel	Unit	
Drain-Source Voltage	V_{DS}	20	- 20	V	
Gate-Source Voltage		V_{GS}	± 12		V
	T _C = 25 °C		3.9	- 2.1	
Continuous Proin Current (T = 150 °C)	T _C = 70 °C	1_	3.1	- 1.7	
Continuous Drain Current (T _J = 150 °C)	T _A = 25 °C	l _D	3.5 ^{b, c}	- 1.9 ^{b, c}	
	T _A = 70 °C		2.8 ^{b, c}	- 1.5 ^{b, c}	Α
Pulsed Drain Current (t = 300 μs)	I _{DM}	12	- 5		
Source Drain Current Diode Current	T _C = 25 °C	I _S	1.2	- 1.1	
Source Drain Current Diode Current	T _A = 25 °C		0.9 ^{b, c}	- 0.9 ^{b, c}	
	T _C = 25 °C		1.4	1.3	
Maximum Power Dissipation	T _C = 70 °C	ь	0.9	0.8	147
	T _A = 25 °C	P _D	1.1 ^{b, c}	1.1 ^{b, c}	W
	T _A = 70 °C		0.7 ^{b, c}	0.7 ^{b, c}	
Operating Junction and Storage Temperature Range		T _J , T _{stg}	- 55 to 150		°C

THERMAL RESISTANCE RATINGS							
		N-Ch	annel	P-Ch	annel		
Parameter		Symbol	Тур.	Max.	Тур.	Max.	Unit
Maximum Junction-to-Ambient ^{b, d}	t ≤ 5 s	R _{thJA}	93	110	97	115	°C/W
Maximum Junction-to-Foot (Drain)	Steady State	R _{thJF}	75	90	78	95	C/VV

- a. Based on T_C = 25 °C.
- b. Surface mounted on 1" x 1" FR4 board.
- c. t = 5 s.
- d. Maximum under steady state conditions is 150 °C/W for N-Channel and 155 °C/W for P-Channel.

Si3585CDV

Vishay Siliconix



rameter Symbol Test Conditions				Min.	Typ. Max	Max.	Unit	
Static						I		
D : 0		$V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}$	N-Ch	20			.,	
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0 \text{ V}, I_D = -250 \mu\text{A}$	P-Ch	- 20			V	
V Tamanayah wa Caaffiniant	AV /T	I _D = 250 μA	N-Ch		15		mV/°C	
V _{DS} Temperature Coefficient	$\Delta V_{DS}/T_{J}$	I _D = - 250 μA	P-Ch		- 16.2			
V Tomporatura Coefficient	AV /T	I _D = 250 μA	N-Ch		- 2.8			
V _{GS(th)} Temperature Coefficient	$\Delta V_{GS(th)}/T_J$	I _D = - 250 μA	P-Ch		2.5			
Cata Thursels and Valtages	V	$V_{DS} = V_{GS}, I_{D} = 250 \mu A$	N-Ch	0.6		1.5	.,	
Gate Threshold Voltage	V _{GS(th)}	$V_{DS} = V_{GS}, I_{D} = -250 \mu A$	P-Ch	- 0.6		- 1.5	V	
Gate-Source Leakage	lasa	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 12 \text{ V}$	N-Ch			± 100	nΛ	
Gale-Source Leakage	I _{GSS}		P-Ch			± 100	nA	
		$V_{DS} = 20 \text{ V}, V_{GS} = 0 \text{ V}$	N-Ch			1		
Zero Gate Voltage Drain Current	Inno	$V_{DS} = -20 \text{ V}, V_{GS} = 0 \text{ V}$	P-Ch			- 1		
Zero Gate Voltage Drain Current	I _{DSS}	$V_{DS} = 20 \text{ V}, V_{GS} = 0 \text{ V}, T_{J} = 55 ^{\circ}\text{C}$	N-Ch			10	μΑ	
		$V_{DS} = -20 \text{ V}, V_{GS} = 0 \text{ V}, T_{J} = 55 ^{\circ}\text{C}$	P-Ch			- 10		
b		$V_{DS} \ge 5 \text{ V}, V_{GS} = 4.5 \text{ V}$	N-Ch	12				
On-State Drain Current ^D	I _{D(on)}	$V_{DS} \le -5 \text{ V}, V_{GS} = -4.5 \text{ V}$	P-Ch	- 5			Α	
		$V_{GS} = 4.5 \text{ V}, I_D = 2.5 \text{ A}$	N-Ch		0.048	0.058		
Drain-Source On-State Resistance ^b		V _{GS} = - 4.5 V, I _D = - 1.9 A	P-Ch		0.162	0.195	Ω	
	R _{DS(on)}	$V_{GS} = 2.5 \text{ V}, I_D = 1 \text{ A}$	N-Ch		0.065	0.078		
		V _{GS} = - 2.5 V, I _D = - 1 A	P-Ch		0.263	0.316		
h		V _{DS} = 10 V, I _D = 35 A			12			
Forward Transconductance ^b	9 _{fs}	V _{DS} = - 10 V, I _D = - 1.9 A	P-Ch		1		S	
Dynamic ^a							L	
			N-Ch		150			
Input Capacitance	C _{iss}	N-Channel $V_{DS} = 10 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHz}$	P-Ch		210		pF	
Output Capacitance	C _{oss}	$v_{DS} = 10 \text{ v}, v_{GS} = 0 \text{ v}, 1 = 1 \text{ Will 12}$	N-Ch		53			
- Carpat Capachario	-055	P-Channel	P-Ch		50			
Reverse Transfer Capacitance	C _{rss}	V_{DS} = - 10 V, V_{GS} = 0 V, f = 1 MHz	N-Ch		22			
			P-Ch		35			
		$V_{DS} = 10 \text{ V}, V_{GS} = 5 \text{ V}, I_D = 3.5 \text{ A}$	N-Ch P-Ch		3.2	4.8		
Total Gate Charge	Q_g	$V_{DS} = -10 \text{ V}, V_{GS} = -5 \text{ V}, I_{D} = -1.9 \text{ A}$			6	9		
		N-Channel	N-Ch		1.6	2.4	nC	
		$V_{DS} = 10 \text{ V}, V_{GS} = 4.5 \text{ V}, I_D = 3.5 \text{ A}$	P-Ch		2.9	4.3		
Gate-Source Charge	Q_{gs}		N-Ch		0.3			
		P-Channel	P-Ch N-Ch		0.6			
Gate-Drain Charge	Q_{gd}	$V_{DS} = -10 \text{ V}, V_{GS} = -4.5 \text{ V}, I_{D} = -1.9 \text{ A}$	P-Ch		0.4			
	R _g f = 1 MHz	N-Ch	0.9	4.8	9.6			
Gate Resistance		f = 1 MHz	P-Ch	1.2	6.2	12.4	Ω	



Parameter	Symbol	Test Conditions			Тур.	Max.	Unit
Dynamic ^a					•		
Turn-On Delay Time	t _{d(on)}	N-Channel	N-Ch P-Ch		5	10	
	4(0.1.)	V = 10 V B = 3.6 O			3	6	
Rise Time	t _r	$I_D \cong 2.8 \text{ A}, V_{GEN} = 10 \text{ V}, R_q = 1 \Omega$	N-Ch		20	30	
		-	P-Ch N-Ch		10	20 20	
Turn-Off Delay Time	t _{d(off)}	P-Channel	P-Ch		13	20	
		V_{DD} = - 10 V, R_L = 6.7 Ω $I_D \cong$ - 1.5 A, V_{GEN} = - 10 V, R_q = 1 Ω	N-Ch		8	16	
Fall Time	t _f	1D = 1.571, VGEN = 10 V, Hg = 132	P-Ch		7	14	
T 0 D 1 T			N-Ch		15	23	ns
Turn-On Delay Time	t _{d(on)}	N-Channel	P-Ch		16	25	
Rise Time	t _r	$V_{DD} = 10 \text{ V}, R_L = 3.6 \Omega$	N-Ch		37	56	
nise Tille	۲r	$I_D \cong 2.8 \text{ A}, V_{GEN} = 4.5 \text{ V}, R_g = 1 \Omega$			16	25	
Turn-Off Delay Time	elay Time $t_{d(off)}$ $V_{DD} = -10 \text{ V, } R_L = 6.7 \Omega$		N-Ch		25	38	
Tam on Boldy Timo			P-Ch		13	20	
Fall Time	t _f	$I_D \cong -1.5 \text{ A}, V_{GEN} = -4.5 \text{ V}, R_g = 1 \Omega$			28	42	
Posito Carros Barto Bia da Obras desirali			P-Ch		9	18	
Drain-Source Body Diode Characteristic	cs T	T	N. Ob	I		1.0	l
Continuous Source-Drain Diode Current	I _S	T _C = 25 °C	N-Ch P-Ch			1.2 - 1.1	-
			N-Ch			12	Α
Pulse Diode Forward Current ^a	I _{SM}		P-Ch			- 5	
		I _S = 2.8 A, V _{GS} = 0 V	N-Ch		0.8	1.2	
Body Diode Voltage	V_{SD}	I _S = - 1.5 A, V _{GS} = 0 V	P-Ch		- 0.8	- 1.2	V
	t _{rr}	3 - 7 G3 -	N-Ch		8	16	
Body Diode Reverse Recovery Time			P-Ch		21	32	ns
Pady Diada Payaraa Bassyary Charre	Q _{rr}	N-Channel	N-Ch		2	4	
Body Diode Reverse Recovery Charge		$I_F = 2.8 \text{ A}, \text{ dI/dt} = 100 \text{ A/}\mu\text{s}, T_J = 25 ^{\circ}\text{C}$	P-Ch		11	20	nC
Reverse Recovery Fall Time	t _a	P-Channel	N-Ch		5		
Tiovolad Hodovory Fall Tillie		$I_F = -1.5 \text{ A}, \text{ dI/dt} = -100 \text{ A/}\mu\text{s}, T_J = 25 ^{\circ}\text{C}$	P-Ch		10		ns
Reverse Recovery Rise Time	t _b		N-Ch		3		113
	ט־		P-Ch		11		

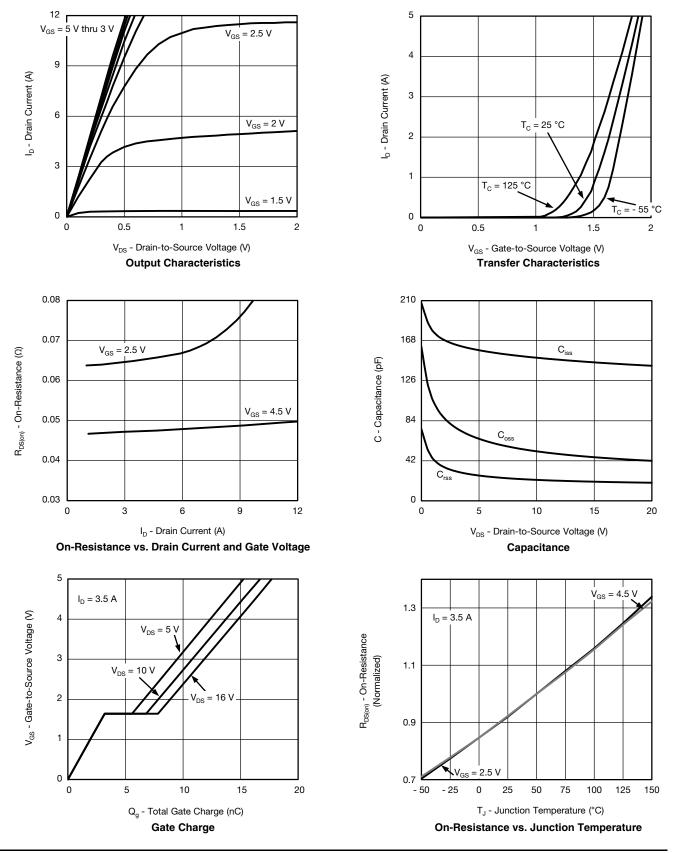
Notes:

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

a. Guaranteed by design, not subject to production testing.

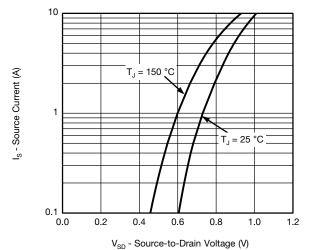
b. Pulse test; pulse width \leq 300 μ s, duty cycle \leq 2 %.

N-CHANNEL TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

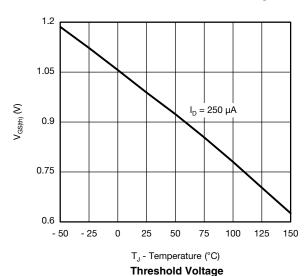


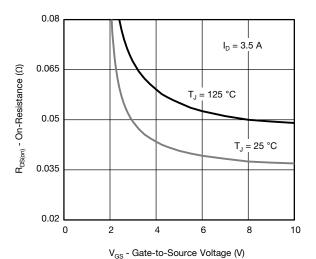


N-CHANNEL TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

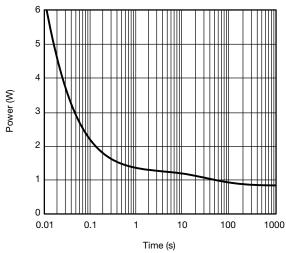


Source-Drain Diode Forward Voltage

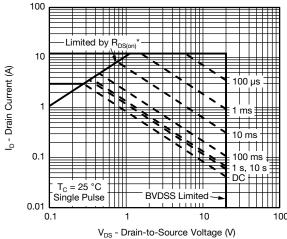




On-Resistance vs. Gate-to-Source Voltage



Single Pulse Power

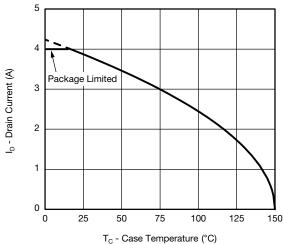


 * V_{GS} > minimum V_{GS} at which R_{DS(on)} is specified

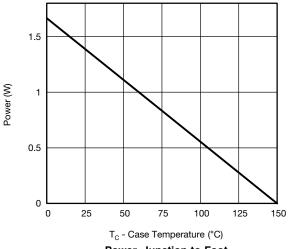
Safe Operating Area, Junction-to-Ambient

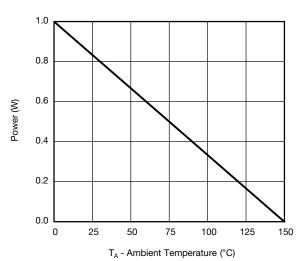


N-CHANNEL TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Current Derating*





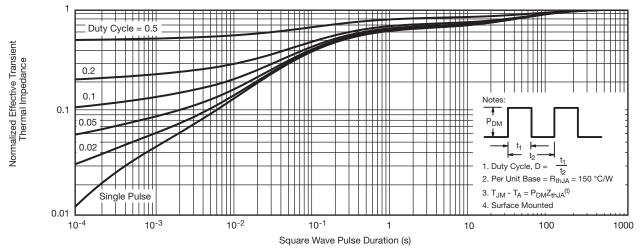
Power, Junction-to-Foot

Power, Junction-to-Ambient

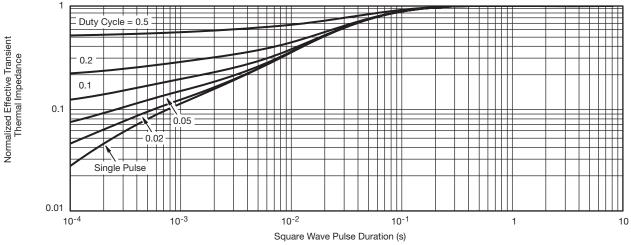
^{*} The power dissipation P_D is based on $T_{J(max)}$ = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.



N-CHANNEL TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



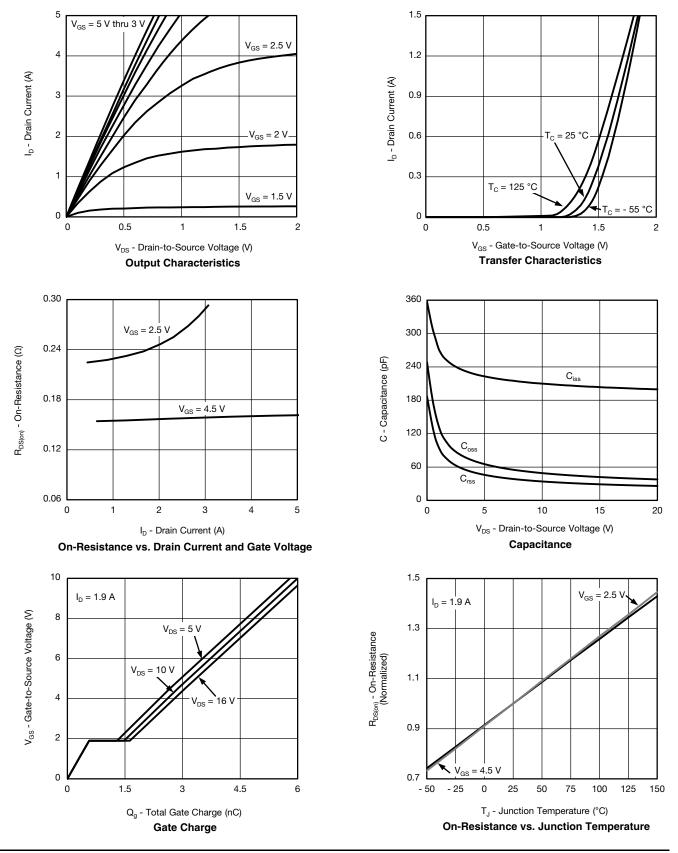
Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Foot

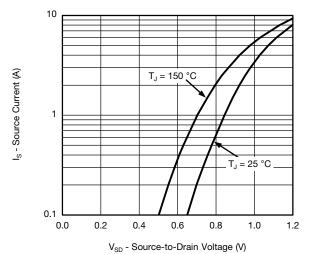
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P-CHANNEL TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

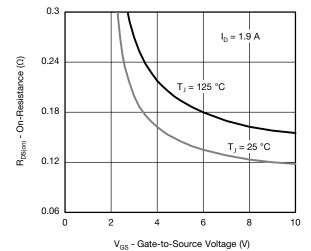




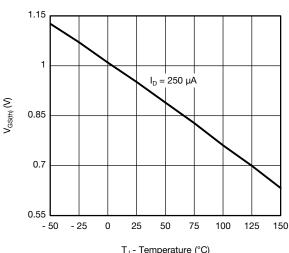
P-CHANNEL TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



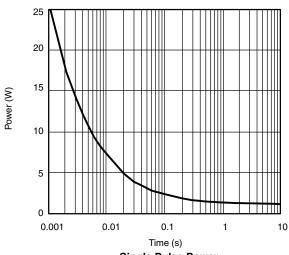
Source-Drain Diode Forward Voltage



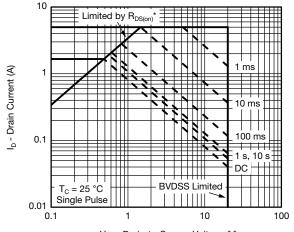
On-Resistance vs. Gate-to-Source Voltage







Single Pulse Power

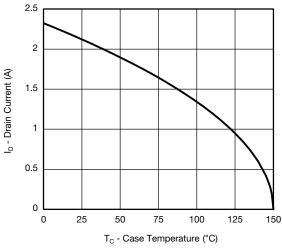


 $V_{DS} \text{ - Drain-to-Source Voltage (V)} \\ ^*V_{GS} \text{ > minimum } V_{GS} \text{ at which } R_{DS(on)} \text{ is specified}$

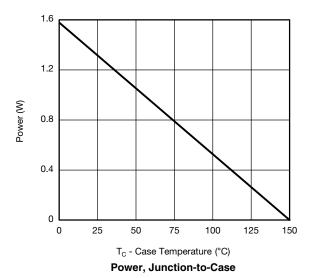
Safe Operating Area, Junction-to-Case

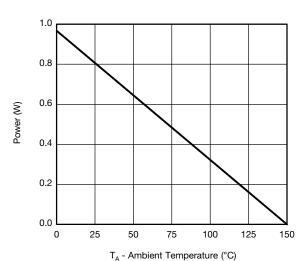


P-CHANNEL TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)







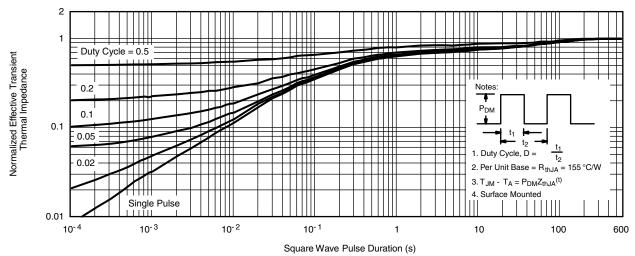


Power, Junction-to-Ambient

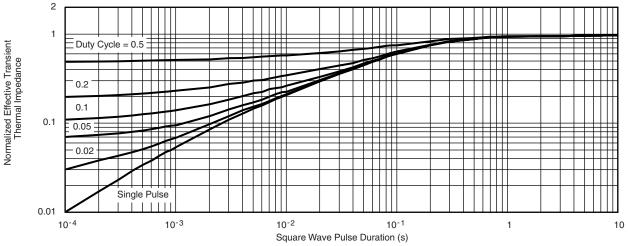
^{*} The power dissipation P_D is based on $T_{J(max)} = 150$ °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.



P-CHANNEL TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Foot

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?67470.

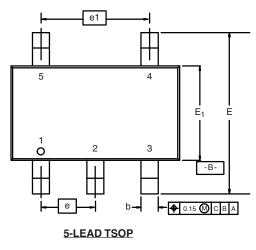
Document Number: 67470 S11-0613-Rev. A, 04-Apr-11

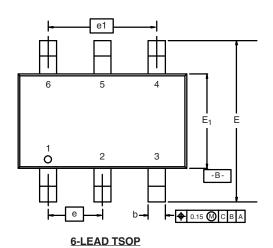




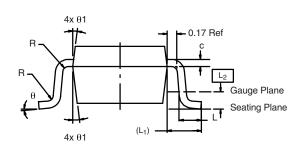
TSOP: 5/6-LEAD

JEDEC Part Number: MO-193C





D A₂ A
Seating Plane



	MIL	LIMETER	RS	ı	NCHES	
Dim	Min	Nom	Max	Min	Nom	Max
Α	0.91	-	1.10	0.036	-	0.043
A ₁	0.01	-	0.10	0.0004	-	0.004
A ₂	0.90	-	1.00	0.035	0.038	0.039
b	0.30	0.32	0.45	0.012	0.013	0.018
С	0.10	0.15	0.20	0.004	0.006	0.008
D	2.95	3.05	3.10	0.116	0.120	0.122
Е	2.70	2.85	2.98	0.106	0.112	0.117
E ₁	1.55	1.65	1.70	0.061	0.065	0.067
е		0.95 BSC		0.0374 BSC		
e ₁	1.80	1.90	2.00	0.071	0.075	0.079
L	0.32	-	0.50	0.012	-	0.020
L ₁		0.60 Ref			0.024 Ref	
L ₂		0.25 BSC		0.010 BSC		
R	0.10	-	-	0.004	-	-
θ	0°	4°	8°	0°	4°	8°
θ_1		7° Nom 7° Nom				
	ECN: C-06593-Rev. I, 18-Dec-06 DWG: 5540					

Document Number: 71200 www.vishay.com 18-Dec-06 uww.vishay.com



Mounting LITTLE FOOT® TSOP-6 Power MOSFETs

Surface mounted power MOSFET packaging has been based on integrated circuit and small signal packages. Those packages have been modified to provide the improvements in heat transfer required by power MOSFETs. Leadframe materials and design, molding compounds, and die attach materials have been changed. What has remained the same is the footprint of the packages.

The basis of the pad design for surface mounted power MOSFET is the basic footprint for the package. For the TSOP-6 package outline drawing see http://www.vishay.com/doc?71200 and see http://www.vishay.com/doc?72610 for the minimum pad footprint. In converting the footprint to the pad set for a power MOSFET, you must remember that not only do you want to make electrical connection to the package, but you must made thermal connection and provide a means to draw heat from the package, and move it away from the package.

In the case of the TSOP-6 package, the electrical connections are very simple. Pins 1, 2, 5, and 6 are the drain of the MOSFET and are connected together. For a small signal device or integrated circuit, typical connections would be made with traces that are 0.020 inches wide. Since the drain pins serve the additional function of providing the thermal connection to the package, this level of connection is inadequate. The total cross section of the copper may be adequate to carry the current required for the application, but it presents a large thermal impedance. Also, heat spreads in a circular fashion from the heat source. In this case the drain pins are the heat sources when looking at heat spread on the PC board.

Figure 1 shows the copper spreading recommended footprint for the TSOP-6 package. This pattern shows the starting point for utilizing the board area available for the heat spreading copper. To create this pattern, a plane of copper overlays the basic pattern on pins 1,2,5, and 6. The copper plane connects the drain pins electrically, but more importantly provides planar copper to draw heat from the drain leads and start the process of spreading the heat so it can be dissipated into the ambient air. Notice that the planar copper is shaped like a "T" to move heat away from the drain leads in all directions. This pattern uses all the available area underneath the body for this purpose.



FIGURE 1. Recommended Copper Spreading Footprint

Since surface mounted packages are small, and reflow soldering is the most common form of soldering for surface mount components, "thermal" connections from the planar copper to the pads have not been used. Even if additional planar copper area is used, there should be no problems in the soldering process. The actual solder connections are defined by the solder mask openings. By combining the basic footprint with the copper plane on the drain pins, the solder mask generation occurs automatically.

A final item to keep in mind is the width of the power traces. The absolute minimum power trace width must be determined by the amount of current it has to carry. For thermal reasons, this minimum width should be at least 0.020 inches. The use of wide traces connected to the drain plane provides a low impedance path for heat to move away from the device.

REFLOW SOLDERING

Vishay Siliconix surface-mount packages meet solder reflow reliability requirements. Devices are subjected to solder reflow as a test preconditioning and are then reliability-tested using temperature cycle, bias humidity, HAST, or pressure pot. The solder reflow temperature profile used, and the temperatures and time duration, are shown in Figures 2 and 3.



Ramp-Up Rate	+6°C/Second Maximum
Temperature @ 155 ± 15°C	120 Seconds Maximum
Temperature Above 180°C	70 – 180 Seconds
Maximum Temperature	240 +5/-0°C
Time at Maximum Temperature	20 – 40 Seconds
Ramp-Down Rate	+6°C/Second Maximum

FIGURE 2. Solder Reflow Temperature Profile

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FIGURE 3. Solder Reflow Temperature and Time Durations

THERMAL PERFORMANCE

A basic measure of a device's thermal performance is the junction-to-case thermal resistance, $R\theta_{jc},$ or the junction-to-foot thermal resistance, $R\theta_{\mbox{\scriptsize if}}.$ This parameter is measured for the device mounted to an infinite heat sink and is therefore a characterization of the device only, in other words, independent of the properties of the object to which the device is mounted. Table 1 shows the thermal performance of the TSOP-6.

TABLE 1.					
Equivalent Steady State Performance—TSOP-6					
Thermal Resistance $R\theta_{jf}$	30°C/W				

SYSTEM AND ELECTRICAL IMPACT OF TSOP-6

In any design, one must take into account the change in MOSFET r_{DS(on)} with temperature (Figure 4).

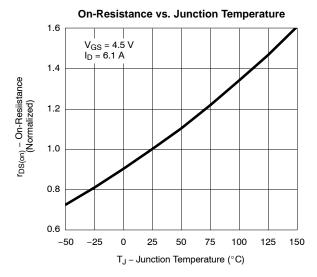


FIGURE 4. Si3434DV

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RECOMMENDED MINIMUM PADS FOR TSOP-6



Recommended Minimum Pads Dimensions in Inches/(mm)

Return to Index





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