

# MC74HC174A

## Hex D Flip-Flop with Common Clock and Reset

### High-Performance Silicon-Gate CMOS

The MC74HC174A is identical in pinout to the LS174. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

This device consists of six D flip-flops with common Clock and Reset inputs. Each flip-flop is loaded with a low-to-high transition of the Clock input. Reset is asynchronous and active-low.

#### Features

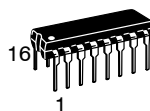
- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2.0 to 6.0 V
- Low Input Current: 1.0  $\mu$ A
- In Compliance with the Requirements Defined by JEDEC Standard No. 7 A
- Chip Complexity: 162 FETs or 40.5 Equivalent Gates
- NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant



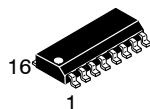
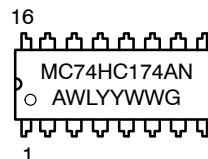
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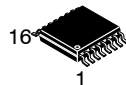
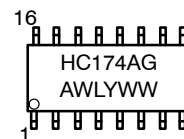
#### MARKING DIAGRAMS



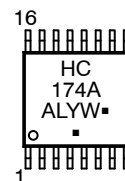
PDIP-16  
N SUFFIX  
CASE 648



SOIC-16  
D SUFFIX  
CASE 751B



TSSOP-16  
DT SUFFIX  
CASE 948F



A = Assembly Location  
L, WL = Wafer Lot  
Y, YY = Year  
W, WW = Work Week  
G or ■ = Pb-Free Package

(Note: Microdot may be in either location)

#### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 2 of this data sheet.

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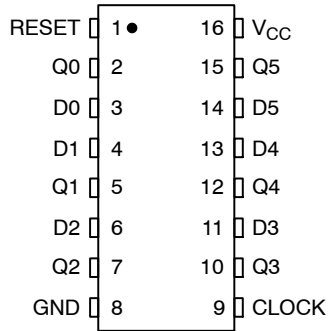


Figure 1. Pin Assignment

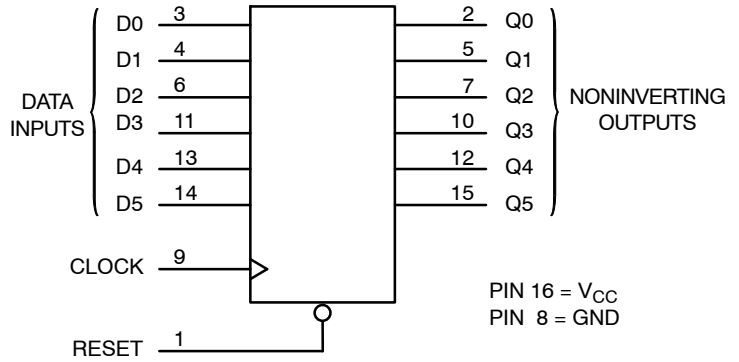


Figure 2. Logic Diagram

## FUNCTION TABLE

| Inputs |       |   | Output    |
|--------|-------|---|-----------|
| Reset  | Clock | D | Q         |
| L      | X     | X | L         |
| H      | ↗     | H | H         |
| H      | ↘     | L | L         |
| H      | L     | X | No Change |
| H      | ↖     | X | No Change |

## DESIGN/VALUE TABLE

| Design Criteria                 | Value  | Units |
|---------------------------------|--------|-------|
| Internal Gate Count*            | 40.5   | ea.   |
| Internal Gate Propagation Delay | 1.5    | ns    |
| Internal Gate Power Dissipation | 5.0    | μW    |
| Speed Power Product             | 0.0075 | pJ    |

\*Equivalent to a two-input NAND gate.

## ORDERING INFORMATION

| Device            | Package               | Shipping†          |
|-------------------|-----------------------|--------------------|
| MC74HC174ANG      | PDIP-16<br>(Pb-Free)  | 500 Units / Rail   |
| MC74HC174ADG      | SOIC-16<br>(Pb-Free)  | 48 Units / Rail    |
| MC74HC174ADR2G    | SOIC-16<br>(Pb-Free)  | 2500 / Tape & Reel |
| MC74HC174ADTR2G   | TSSOP-16<br>(Pb-Free) | 2500 / Tape & Reel |
| NLV74HC174ADG*    | SOIC-16<br>(Pb-Free)  | 55 Units / Rail    |
| NLV74HC174ADR2G*  | SOIC-16<br>(Pb-Free)  | 2500 / Tape & Reel |
| NLV74HC174ADTR2G* | TSSOP-16<br>(Pb-Free) | 2500 / Tape & Reel |
| NLV74HC174ANG*    | PDIP-16<br>(Pb-Free)  | 25 Units / Rail    |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

\*NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable

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## MAXIMUM RATINGS

| Symbol        | Parameter                                                                                                  | Value                    | Unit |
|---------------|------------------------------------------------------------------------------------------------------------|--------------------------|------|
| $V_{CC}$      | DC Supply Voltage (Referenced to GND)                                                                      | – 0.5 to + 7.0           | V    |
| $V_{IN}$      | DC Input Voltage (Referenced to GND)                                                                       | – 1.5 to $V_{CC}$ + 1.5  | V    |
| $V_{OUT}$     | DC Output Voltage (Referenced to GND) (Note 1)                                                             | – 0.5 to $V_{CC}$ + 0.5  | V    |
| $I_{IN}$      | DC Input Current, per Pin                                                                                  | ± 20                     | mA   |
| $I_{OUT}$     | DC Output Current, per Pin                                                                                 | ± 25                     | mA   |
| $I_{CC}$      | DC Supply Current, $V_{CC}$ and GND Pins                                                                   | ± 50                     | mA   |
| $T_{STG}$     | Storage Temperature Range                                                                                  | – 65 to + 150            | °C   |
| $T_L$         | Lead Temperature, 1 mm from Case for 10 Seconds PDIP, SOIC, TSSOP                                          | 260                      | °C   |
| $T_J$         | Junction Temperature Under Bias                                                                            | + 150                    | °C   |
| $\theta_{JA}$ | Thermal Resistance PDIP<br>SOIC<br>TSSOP                                                                   | 78<br>112<br>148         | °C/W |
| $P_D$         | Power Dissipation in Still Air at 85°C PDIP<br>SOIC<br>TSSOP                                               | 750<br>500<br>450        | mW   |
| MSL           | Moisture Sensitivity                                                                                       | Level 1                  |      |
| $F_R$         | Flammability Rating Oxygen Index: 30% – 35%                                                                | UL 94 V–0 @ 0.125 in.    |      |
| $V_{ESD}$     | ESD Withstand Voltage Human Body Model (Note 2)<br>Machine Model (Note 3)<br>Charged Device Model (Note 4) | > 2000<br>> 100<br>> 500 | V    |
| $I_{LATCHUP}$ | Latchup Performance Above $V_{CC}$ and Below GND at 85°C (Note 5)                                          | ± 300                    | mA   |

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1.  $I_O$  absolute maximum rating must be observed.
2. Tested to EIA/JESD22–A114–A.
3. Tested to EIA/JESD22–A115–A.
4. Tested to JESD22–C101–A.
5. Tested to EIA/JESD78.

## RECOMMENDED OPERATING CONDITIONS

| Symbol                  | Parameter                                                                                                                 | Min              | Max                       | Unit |
|-------------------------|---------------------------------------------------------------------------------------------------------------------------|------------------|---------------------------|------|
| $V_{CC}$                | DC Supply Voltage (Referenced to GND)                                                                                     | 2.0              | 6.0                       | V    |
| $V_{IN}$ ,<br>$V_{OUT}$ | DC Input Voltage, Output Voltage (Referenced to GND) (Note 6)                                                             | 0                | $V_{CC}$                  | V    |
| $T_A$                   | Operating Temperature, All Package Types                                                                                  | – 55             | + 125                     | °C   |
| $t_r$ , $t_f$           | CLOCK Input Rise and Fall Time (Figure 4)<br>$V_{CC} = 2.0$ V<br>$V_{CC} = 3.3$ V<br>$V_{CC} = 4.5$ V<br>$V_{CC} = 6.0$ V | 0<br>0<br>0<br>0 | 1000<br>700<br>500<br>400 | ns   |

6. Unused inputs may not be left open. All inputs must be tied to a high– or low–logic input voltage level.

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## DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

| Symbol          | Parameter                                      | Test Conditions                                                                                                      | V <sub>CC</sub><br>V | Guaranteed Limit   |                    |                    | Unit |
|-----------------|------------------------------------------------|----------------------------------------------------------------------------------------------------------------------|----------------------|--------------------|--------------------|--------------------|------|
|                 |                                                |                                                                                                                      |                      | –55°C to 25°C      | ≤85°C              | ≤125°C             |      |
| V <sub>IH</sub> | Minimum High-Level Input Voltage               | V <sub>OUT</sub> = 0.1 V or V <sub>CC</sub> – 0.1 V<br> I <sub>OUT</sub>   ≤ 20 μA                                   | 2.0<br>4.5<br>6.0    | 1.5<br>3.15<br>4.2 | 1.5<br>3.15<br>4.2 | 1.5<br>3.15<br>4.2 | V    |
| V <sub>IL</sub> | Maximum Low-Level Input Voltage                | V <sub>OUT</sub> = 0.1 V or V <sub>CC</sub> – 0.1 V<br> I <sub>OUT</sub>   ≤ 20 μA                                   | 2.0<br>4.5<br>6.0    | 0.5<br>1.35<br>1.8 | 0.5<br>1.35<br>1.8 | 0.5<br>1.35<br>1.8 | V    |
| V <sub>OH</sub> | Minimum High-Level Output Voltage              | V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub><br> I <sub>OUT</sub>   ≤ 20 μA                                  | 2.0<br>4.5<br>6.0    | 1.9<br>4.4<br>5.9  | 1.9<br>4.4<br>5.9  | 1.9<br>4.4<br>5.9  | V    |
|                 |                                                | V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub><br> I <sub>OUT</sub>   ≤ 4.0 mA<br> I <sub>OUT</sub>   ≤ 5.2 mA | 4.5<br>6.0           | 3.98<br>5.48       | 3.84<br>5.34       | 3.7<br>5.2         |      |
| V <sub>OL</sub> | Maximum Low-Level Output Voltage               | V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub><br> I <sub>OUT</sub>   ≤ 20 μA                                  | 2.0<br>4.5<br>6.0    | 0.1<br>0.1<br>0.1  | 0.1<br>0.1<br>0.1  | 0.1<br>0.1<br>0.1  | V    |
|                 |                                                | V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub><br> I <sub>OUT</sub>   ≤ 4.0 mA<br> I <sub>OUT</sub>   ≤ 5.2 mA | 4.5<br>6.0           | 0.26<br>0.26       | 0.33<br>0.33       | 0.4<br>0.4         |      |
| I <sub>IN</sub> | Maximum Input Leakage Current                  | V <sub>IN</sub> = V <sub>CC</sub> or GND                                                                             | 6.0                  | ±0.1               | ±1.0               | ±1.0               | μA   |
| I <sub>CC</sub> | Maximum Quiescent Supply Current (per Package) | V <sub>IN</sub> = V <sub>CC</sub> or GND<br>I <sub>OUT</sub> = 0 μA                                                  | 6.0                  | 4.0                | 40                 | 160                | μA   |

## AC ELECTRICAL CHARACTERISTICS (C<sub>L</sub> = 50 pF, Input t<sub>r</sub> = t<sub>f</sub> = 6.0 ns)

| Symbol                               | Parameter                                                       | V <sub>CC</sub><br>V | Guaranteed Limit |                 |                 | Unit |
|--------------------------------------|-----------------------------------------------------------------|----------------------|------------------|-----------------|-----------------|------|
|                                      |                                                                 |                      | –55°C to 25°C    | ≤85°C           | ≤125°C          |      |
| f <sub>max</sub>                     | Maximum Clock Frequency (50% Duty Cycle)<br>(Figures 4 and 7)   | 2.0<br>4.5<br>6.0    | 6.0<br>30<br>35  | 4.8<br>24<br>28 | 4.0<br>20<br>24 | MHz  |
| t <sub>PLH</sub><br>t <sub>PHL</sub> | Maximum Propagation Delay, Clock to Q<br>(Figures 5 and 7)      | 2.0<br>4.5<br>6.0    | 110<br>22<br>19  | 140<br>28<br>24 | 165<br>33<br>28 | ns   |
| t <sub>PLH</sub><br>t <sub>PHL</sub> | Maximum Propagation Delay, Reset to Q<br>(Figures 2 and 7)      | 2.0<br>4.5<br>6.0    | 110<br>21<br>19  | 140<br>28<br>24 | 160<br>32<br>27 | ns   |
| t <sub>TLH</sub><br>t <sub>THL</sub> | Maximum Output Transition Time, Any Output<br>(Figures 4 and 7) | 2.0<br>4.5<br>6.0    | 75<br>15<br>13   | 95<br>19<br>16  | 110<br>22<br>19 | ns   |
| C <sub>in</sub>                      | Maximum Input Capacitance                                       |                      | 10               | 10              | 10              | pF   |

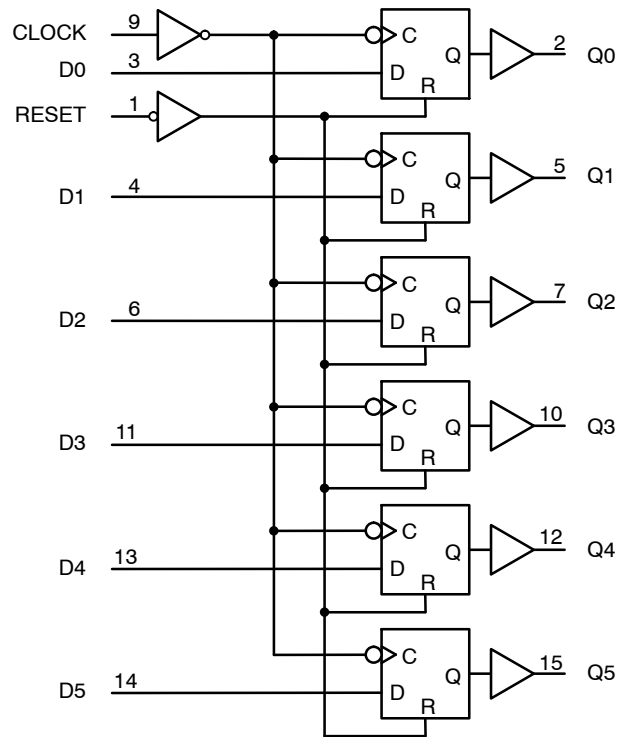
| C <sub>PD</sub> | Power Dissipation Capacitance, per Enabled Output (Note 7) | Typical @ 25°C, V <sub>CC</sub> = 5.0 V | pF |
|-----------------|------------------------------------------------------------|-----------------------------------------|----|
|                 |                                                            | 62                                      |    |

7. Used to determine the no-load dynamic power consumption:  $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ .

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**TIMING REQUIREMENTS** ( $C_L = 50$  pF, Input  $t_r = t_f = 6.0$  ns)

| Symbol                          | Parameter                                         | Figure | V <sub>CC</sub><br>V | Guaranteed Limit  |                    |                   |                    |                   |                    | Unit |
|---------------------------------|---------------------------------------------------|--------|----------------------|-------------------|--------------------|-------------------|--------------------|-------------------|--------------------|------|
|                                 |                                                   |        |                      | −55°C to 25°C     |                    | ≤85°C             |                    | ≤125°C            |                    |      |
|                                 |                                                   |        |                      | Min               | Max                | Min               | Max                | Min               | Max                |      |
| t <sub>su</sub>                 | Minimum Setup Time, Data to Clock                 | 6      | 2.0<br>4.5<br>6.0    | 50<br>10<br>9.0   |                    | 65<br>13<br>11    |                    | 75<br>15<br>13    |                    | ns   |
| t <sub>h</sub>                  | Minimum Hold Time, Clock to Data                  | 6      | 2.0<br>4.5<br>6.0    | 5.0<br>5.0<br>5.0 |                    | 5.0<br>5.0<br>5.0 |                    | 5.0<br>5.0<br>5.0 |                    | ns   |
| t <sub>rec</sub>                | Minimum Recovery Time,<br>Reset Inactive to Clock | 5      | 2.0<br>4.5<br>6.0    | 5.0<br>5.0<br>5.0 |                    | 5.0<br>5.0<br>5.0 |                    | 5.0<br>5.0<br>5.0 |                    | ns   |
| t <sub>w</sub>                  | Minimum Pulse Width, Clock                        | 4      | 2.0<br>4.5<br>6.0    | 75<br>15<br>13    |                    | 95<br>19<br>16    |                    | 110<br>22<br>19   |                    | ns   |
| t <sub>w</sub>                  | Minimum Pulse Width, Reset                        | 5      | 2.0<br>4.5<br>6.0    | 75<br>15<br>13    |                    | 95<br>19<br>16    |                    | 110<br>22<br>19   |                    | ns   |
| t <sub>r</sub> , t <sub>f</sub> | Maximum Input Rise and Fall Times                 | 4      | 2.0<br>4.5<br>6.0    |                   | 1000<br>500<br>400 |                   | 1000<br>500<br>400 |                   | 1000<br>500<br>400 | ns   |



**Figure 3. Expanded Logic Diagram**

# MC74HC174A

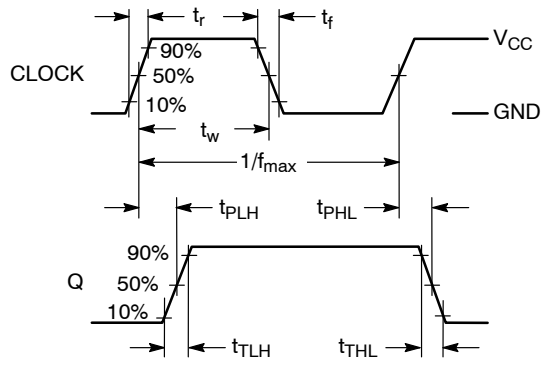


Figure 4. Switching Waveform

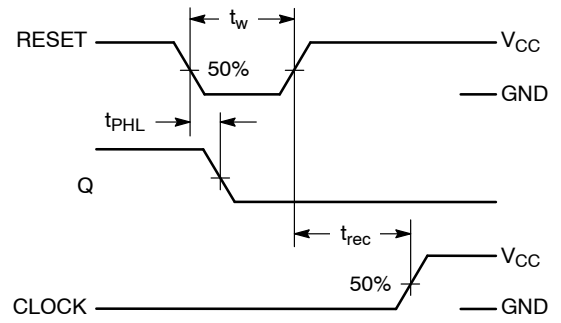


Figure 5. Switching Waveform

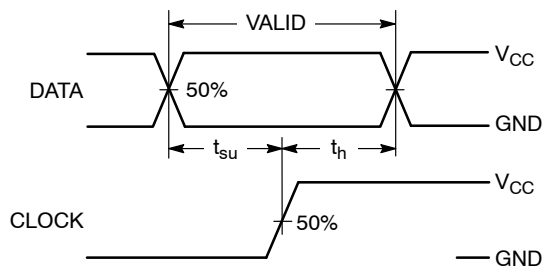
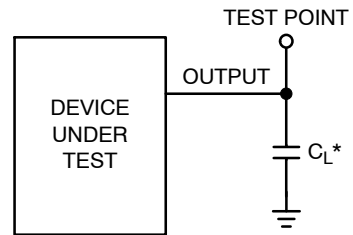


Figure 6. Switching Waveform



\*Includes all probe and jig capacitance

Figure 7. Test Circuit

# MC74HC174A

## PACKAGE DIMENSIONS

PDIP-16  
CASE 648-08  
ISSUE T



### NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

| DIM | INCHES    |       | MILLIMETERS |       |
|-----|-----------|-------|-------------|-------|
|     | MIN       | MAX   | MIN         | MAX   |
| A   | 0.740     | 0.770 | 18.80       | 19.55 |
| B   | 0.250     | 0.270 | 6.35        | 6.85  |
| C   | 0.145     | 0.175 | 3.69        | 4.44  |
| D   | 0.015     | 0.021 | 0.39        | 0.53  |
| F   | 0.040     | 0.70  | 1.02        | 1.77  |
| G   | 0.100 BSC |       | 2.54 BSC    |       |
| H   | 0.050 BSC |       | 1.27 BSC    |       |
| J   | 0.008     | 0.015 | 0.21        | 0.38  |
| K   | 0.110     | 0.130 | 2.80        | 3.30  |
| L   | 0.295     | 0.305 | 7.50        | 7.74  |
| M   | 0° 10°    |       | 0° 10°      |       |
| S   | 0.020     | 0.040 | 0.51        | 1.01  |

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## PACKAGE DIMENSIONS

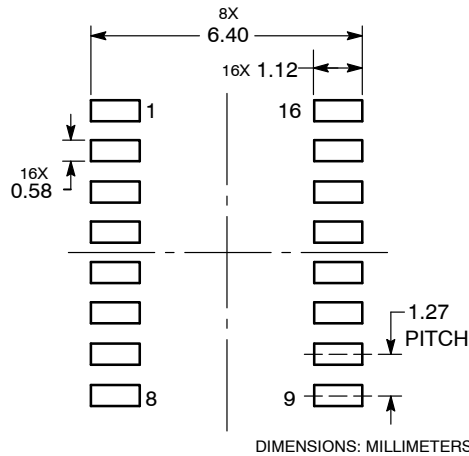
SOIC-16  
CASE 751B-05  
ISSUE K



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: MILLIMETER.
  3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
  4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
  5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

| DIM | MILLIMETERS |       | INCHES    |       |
|-----|-------------|-------|-----------|-------|
|     | MIN         | MAX   | MIN       | MAX   |
| A   | 9.80        | 10.00 | 0.386     | 0.393 |
| B   | 3.80        | 4.00  | 0.150     | 0.157 |
| C   | 1.35        | 1.75  | 0.054     | 0.068 |
| D   | 0.35        | 0.49  | 0.014     | 0.019 |
| F   | 0.40        | 1.25  | 0.016     | 0.049 |
| G   | 1.27 BSC    |       | 0.050 BSC |       |
| J   | 0.19        | 0.25  | 0.008     | 0.009 |
| K   | 0.10        | 0.25  | 0.004     | 0.009 |
| M   | 0°          | 7°    | 0°        | 7°    |
| P   | 5.80        | 6.20  | 0.229     | 0.244 |
| R   | 0.25        | 0.50  | 0.010     | 0.019 |

## SOLDERING FOOTPRINT\*



\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.



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На всех этапах разработки и производства наши партнеры могут получить квалифицированную поддержку опытных инженеров.

Система менеджмента качества компании отвечает требованиям в соответствии с ГОСТ Р ИСО 9001, ГОСТ РВ 0015-002 и ЭС РД 009

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