NBC12439, NBC12439A

3.3V/5V Programmable PLL Synthesized Clock Generator

50 MHz to 800 MHz

ON Semiconductor®

http://onsemi.com

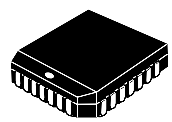
Description

The NBC12439 and NBC12439A are general purpose, PLL based synthesized clock sources. The VCO will operate over a frequency range of 400 MHz to 800 MHz. The VCO frequency is sent to the N-output divider, where it can be configured to provide division ratios of 1, 2, 4 or 8. The VCO and output frequency can be programmed using the parallel or serial interfaces to the configuration logic. Output frequency steps of 16 MHz, 8 MHz, 4 MHz, or 2 MHz can be achieved using a 16 MHz crystal, depending on the output divider settings. The PLL loop filter is fully integrated and does not require any external components.

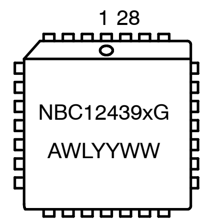
Features

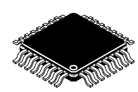
- Best-in-Class Output Jitter Performance, ±20 ps Peak-to-Peak
- 50 MHz to 800 MHz Programmable Differential PECL Outputs
- Fully Integrated Phase-Lock-Loop with Internal Loop Filter
- Parallel Interface for Programming Counter and Output Dividers During Powerup
- Minimal Frequency Overshoot
- Serial 3-Wire Programming Interface
- Crystal Oscillator Inputs 10 MHz to 20 MHz
- Operating Range: V_{CC} = 3.135 V to 5.25 V
- CMOS and TTL Compatible Control Inputs
- Pin and Function Compatible with Motorola MC12439 and MPC9239
- Powerdown of PECL Outputs (÷ 16)
- 0°C to 70°C Ambient Operating Temperature (NBC12439)
- -40°C to 85°C Ambient Operating Temperature (NBC12439A)
- Pb-Free Packages are Available

MARKING DIAGRAMS

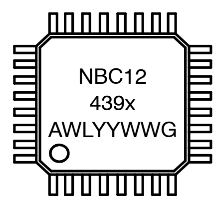


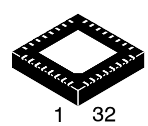
PLCC-28
FN SUFFIX
CASE 776



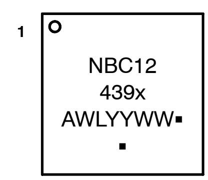


LQFP-32
FA SUFFIX
CASE 873A





QFN32
MN SUFFIX
CASE 488AM



x	= Blank or A
A	= Assembly Location
WL, L	= Wafer Lot
YY, Y	= Year
WW, W	= Work Week
G or ▪	= Pb-Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 16 of this data sheet.

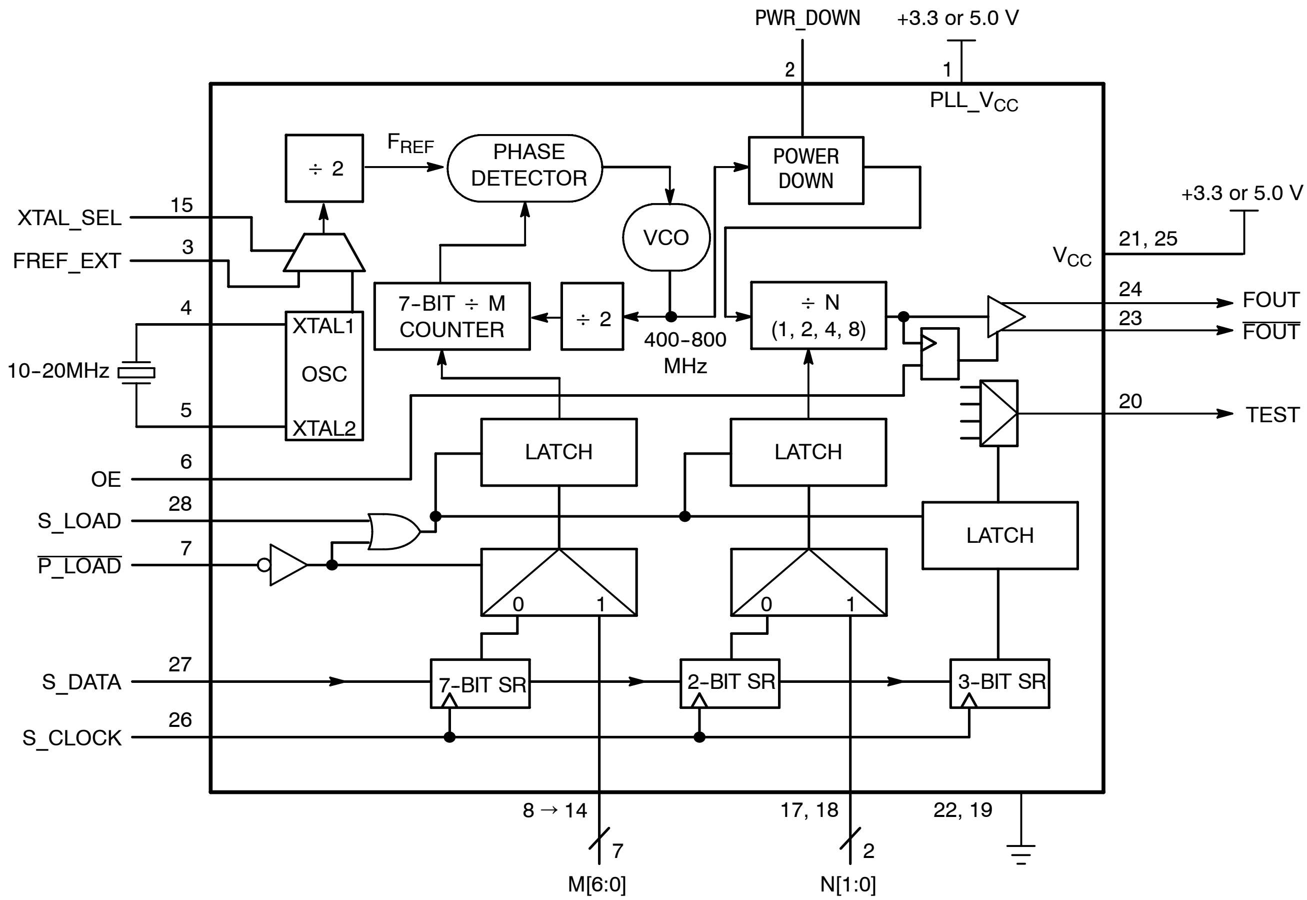


Figure 1. Block Diagram (28-Lead PLCC)

Table 1. Output Division

N [1:0]	Output Division
0 0	2
0 1	4
1 0	8
1 1	1

Table 2. XTAL_SEL And OE

Input	0	1
PWR_DOWN	F_{OUT}	F_{OUT} ÷ 16
XTAL_SEL	FREF_EXT	XTAL
OE	Outputs Disabled	Outputs Enabled

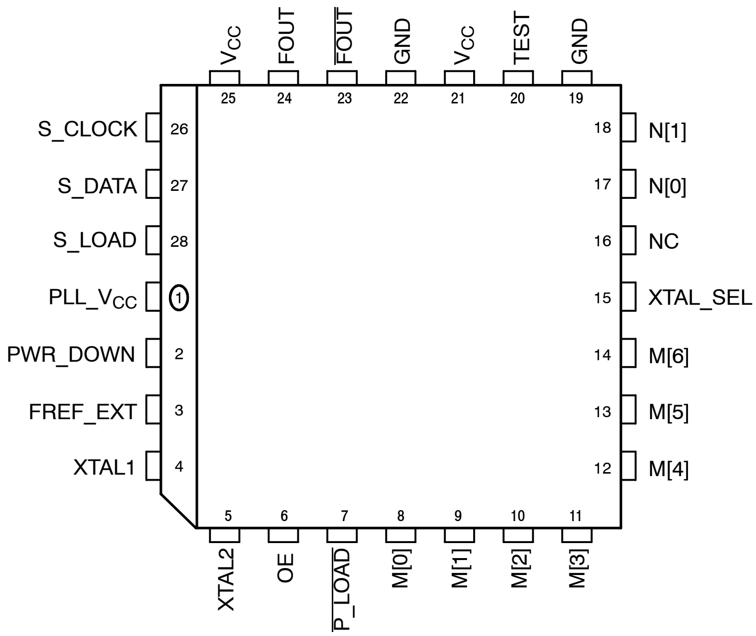


Figure 2. 28-Lead PLCC (Top View)

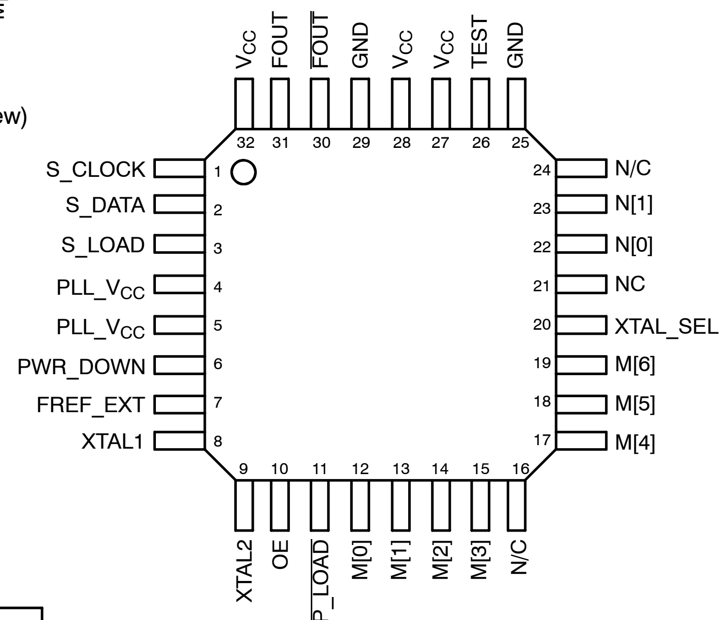


Figure 3. 32-Lead LQFP (Top View)

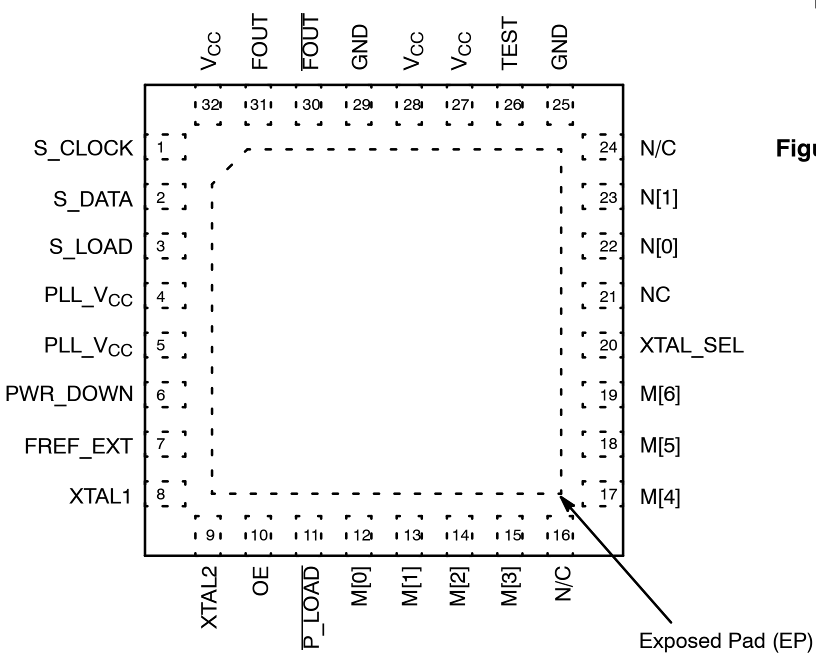


Figure 4. 32-Lead QFN (Top View)

The following gives a brief description of the functionality of the NBC12439 and NBC12349A Inputs and Outputs. Unless explicitly stated, all inputs are CMOS/TTL compatible with either pull-up or pulldown resistors. The PECL outputs are capable of driving two series terminated 50 Ω transmission lines on the incident edge.

Table 3. PIN FUNCTION DESCRIPTION

Pin Name	Function	Description
INPUTS		
XTAL1, XTAL2	Crystal Inputs	These pins form an oscillator when connected to an external series-resonant crystal.
S_LOAD*	CMOS/TTL Serial Latch Input (Internal Pulldown Resistor)	This pin loads the configuration latches with the contents of the shift registers. The latches will be transparent when this signal is HIGH; thus, the data must be stable on the HIGH-to-LOW transition of S_LOAD for proper operation.
S_DATA*	CMOS/TTL Serial Data Input (Internal Pulldown Resistor)	This pin acts as the data input to the serial configuration shift registers.
S_CLOCK*	CMOS/TTL Serial Clock Input (Internal Pulldown Resistor)	This pin serves to clock the serial configuration shift registers. Data from S_DATA is sampled on the rising edge.
$\overline{\mathrm{P\_LOAD}}$**	CMOS/TTL Parallel Latch Input (Internal Pullup Resistor)	This pin loads the configuration latches with the contents of the parallel inputs .The latches will be transparent when this signal is LOW; therefore, the parallel data must be stable on the LOW-to-HIGH transition of $\overline{\mathrm{P\_LOAD}}$ for proper operation.
M[6:0]**	CMOS/TTL PLL Loop Divider Inputs (Internal Pullup Resistor)	These pins are used to configure the PLL loop divider. They are sampled on the LOW-to-HIGH transition of $\overline{\mathrm{P\_LOAD}}$. M[6] is the MSB, M[0] is the LSB.
N[1:0]**	CMOS/TTL Output Divider Inputs (Internal Pullup Resistor)	These pins are used to configure the output divider modulus. They are sampled on the LOW-to-HIGH transition of $\overline{\mathrm{P\_LOAD}}$.
OE**	CMOS/TTL Output Enable Input (Internal Pullup Resistor)	Active HIGH Output Enable. The Enable is synchronous to eliminate possibility of runt pulse generation on the FOUT output.
FREF_EXT*	CMOS/TTL Input (Internal Pulldown Resistor)	This pin can be used as the PLL Reference
XTAL_SEL**	CMOS/TTL Input (Internal Pullup Resistor)	This pin selects between the crystal and the FREF_EXT source for the PLL reference signal. A HIGH selects the crystal input.
PWR_DOWN	CMOS/TTL Input (Internal Pulldown Resistor)	PWR_DOWN forces the FOUT outputs to synchronously reduce frequency by a factor of 16.
OUTPUTS		
FOUT, $\overline{\mathrm{FOUT}}$	PECL Differential Outputs	These differential, positive-referenced ECL signals (PECL) are the outputs of the synthesizer.
TEST	CMOS/TTL Output	The function of this output is determined by the serial configuration bits T[2:0].
POWER		
V_{CC}	Positive Supply for the Logic	The positive supply for the internal logic and output buffer of the chip, and is connected to +3.3 V or +5.0 V.
PLL_V_{CC}	Positive Supply for the PLL	This is the positive supply for the PLL and is connected to +3.3 V or +5.0 V.
GND	Negative Power Supply	These pins are the negative supply for the chip and are normally all connected to ground.
-	Exposed Pad for QFN-32 only	The Exposed Pad (EP) on the QFN-32 package bottom is thermally connected to the die for improved heat transfer out of package. The exposed pad must be attached to a heat-sinking conduit. The pad is electrically connected to GND.

* When left Open, these inputs will default LOW.
** When left Open, these inputs will default HIGH.

Table 4. ATTRIBUTES

Characteristics		Value	
Internal Input Pulldown Resistor		75 kΩ	
Internal Input Pullup Resistor		37.5 kΩ	
ESD Protection	Human Body Model Machine Model Charged Device Model	> 2 kV > 150 V > 1 kV	
Moisture Sensitivity (Note 1)		Pb Pkg	Pb-Free Pkg
	PLCC LQFP QFN	Level 1 Level 2 Level 1	Level 1 Level 2 Level 1
Flammability Rating	Oxygen Index: 28 to 34	UL 94 V-0 @ 0.125 in	
Transistor Count		2269	
Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test			

1. For additional information, see Application Note AND8003/D.

Table 5. MAXIMUM RATINGS

Symbol	Parameter	Condition 1	Condition 2	Rating	Unit
V_{CC}	Positive Supply	GND = 0 V		6	V
V_I	Input Voltage	GND = 0 V	$V_I \leq V_{CC}$	6	V
I_{out}	Output Current	Continuous Surge		50 100	mA mA
T_A	Operating Temperature Range NB12439 NB12439A			0 to 70 -40 to +85	°C
T_{stg}	Storage Temperature Range			-65 to +150	°C
θ_{JA}	Thermal Resistance (Junction-to-Ambient)	0 lfpm 500 lfpm	PLCC-28 PLCC-28	63.5 43.5	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction-to-Case)	Standard Board	PLCC-28	22 to 26	°C/W
θ_{JA}	Thermal Resistance (Junction-to-Ambient)	0 lfpm 500 lfpm	LQFP-32 LQFP-32	80 55	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction-to-Case)	Standard Board	LQFP-32	12 to 17	°C/W
θ_{JA}	Thermal Resistance (Junction-to-Ambient)	0 lfpm 500 lfpm	QFN-32 QFN-32	31 27	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction-to-Case)	2S2P	QFN-32	12	°C/W
T_{sol}	Wave Solder Pb Pb-Free	<3 sec @ 248°C <3 sec @ 260°C		265 265	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

Table 6. DC CHARACTERISTICS (V_{CC} = 3.3 V ± 5%; T_A = 0°C to 70°C (NBC12439), T_A = −40°C to 85°C (NBC12439A))

Symbol	Characteristic	Condition	Min	Typ	Max	Unit
V_{IH} LVCMOS/ LVTTL	Input HIGH Voltage	V_{CC} = 3.3 V	2.0			V
V_{IL} LVCMOS/ LVTTL	Input LOW Voltage	V_{CC} = 3.3 V			0.8	V
I_{IN}	Input Current				1.0	mA
V_{OH}	Output HIGH Voltage TEST	I_{OH} = −0.8 mA	2.5			V
V_{OL}	Output LOW Voltage TEST	I_{OL} = 0.8 mA			0.4	V
V_{OH} PECL	Output HIGH Voltage FOUT $\overline{FOUT}$	V_{CC} = 3.3 V (Notes 2, 3)	2.155		2.405	V
V_{OL} PECL	Output LOW Voltage FOUT $\overline{FOUT}$	V_{CC} = 3.3 V (Notes 2, 3)	1.355		1.675	V
I_{CC}	Power Supply Current V_{CC} PLL_V_{CC}		 44 19	 58 23	 80 28	 mA mA

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

2. $F_{OUT}/\overline{F_{OUT}}$ output levels will vary 1:1 with V_{CC} variation.
3. $F_{OUT}/\overline{F_{OUT}}$ outputs are terminated through a 50 Ω resistor to V_{CC} − 2.0 volts.

Table 7. DC CHARACTERISTICS (V_{CC} = 5.0 V ± 5%; T_A = 0°C to 70°C (NBC12439), T_A = −40°C to 85°C (NBC12439A))

Symbol	Characteristic	Condition	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
V_{IH} CMOS/ TTL	Input HIGH Voltage	V_{CC} = 5.0 V	2.0			2.0			2.0			V
V_{IL} CMOS/ TTL	Input LOW Voltage	V_{CC} = 5.0 V			0.8			0.8			0.8	V
I_{IN}	Input Current				1.0			1.0			1.0	mA
V_{OH}	Output HIGH Voltage TEST	I_{OH} = −0.8 mA	2.5			2.5			2.5			V
V_{OL}	Output LOW Voltage TEST	I_{OL} = 0.8 mA			0.4			0.4			0.4	V
V_{OH} PECL	Output HIGH Voltage FOUT $\overline{FOUT}$	V_{CC} = 5.0 V (Notes 4, 5)	3.855		4.105	3.855		4.105	3.855		4.105	V
V_{OL} PECL	Output LOW Voltage FOUT $\overline{FOUT}$	V_{CC} = 5.0 V (Notes 4, 5)	3.055		3.305	3.055		3.305	3.055		3.305	V
I_{CC}	Power Supply Current V_{CC} PLL_V_{CC}		 47 19	 58 24	 85 28	 47 19	 60 24	 85 28	 47 19	 60 24	 85 28	 mA mA

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

4. $F_{OUT}/\overline{F_{OUT}}$ output levels will vary 1:1 with V_{CC} variation.
5. $F_{OUT}/\overline{F_{OUT}}$ outputs are terminated through a 50 Ω resistor to V_{CC} − 2.0 volts.

Table 8. AC CHARACTERISTICS (V_{CC} = 3.135 V to 5.25 V ± 5%; T_A = 0°C to 70°C (NBC12439), T_A = −40°C to 85°C (NBC12439A)) (Note 7)

Symbol	Characteristic		Condition	Min	Max	Unit
F_{IN}	Input Frequency	S_CLOCK Xtal Oscillator FREF_EXT (Note 8)	(Note 6)	– 10 10	10 20 100	MHz
F_{OUT}	Output Frequency	VCO (Internal) F_{OUT}		400 50	800 800	MHz
t_{LOCK}	Maximum PLL Lock Time				10	ms
$t_{jitter(pd)}$	Period Jitter (RMS)	(1σ)	50 MHz ≤ f_{OUT} < 100 MHz 100 MHz ≤ f_{OUT} < 800 MHz		8 5	ps
$t_{jitter(cyc-cyc)}$	Cycle-to-Cycle Jitter (Peak-to-Peak)	(8σ)	50 MHz ≤ f_{OUT} < 100 MHz 100 MHz ≤ f_{OUT} < 800 MHz		±40 ±20	ps
t_s	Setup Time	S_DATA to S_CLOCK S_CLOCK to $\overline{\text{S\_LOAD}}$ M, N to $\overline{\text{P\_LOAD}}$		20 20 20	– – –	ns
t_h	Hold Time	S_DATA to S_CLOCK S_CLOCK to $\overline{\text{S\_LOAD}}$ M, N to $\overline{\text{P\_LOAD}}$		20 20 20	– – –	ns
tpw_{MIN}	Minimum Pulse Width	S_LOAD $\overline{\text{P\_LOAD}}$		50 50	– –	ns
DCO	Output Duty Cycle			47.5	52.5	%
t_r, t_f	Output Rise/Fall	FOUT	20%-80%	175	425	ps

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

6. 10 MHz is the maximum frequency to load the feedback divide registers. S_CLOCK can be switched at higher frequencies when used as a test clock in TEST_MODE 6.
7. $F_{OUT}/\overline{F_{OUT}}$ outputs are terminated through a 50 Ω resistor to V_{CC} – 2.0 V. Internal phase detector can handle up to 100 MHz on it's input.
8. Maximum frequency on FREF_EXT is a function of setting the appropriate M counter value, 20 ≤ M ≤ 80, for the VCO to operate within the valid range of 400 MHz ≤ f_{VCO} ≤ 800 MHz. (See Table 11)
9. See applications information section.

FUNCTIONAL DESCRIPTION

The internal oscillator uses the external quartz crystal as the basis of its frequency reference. The output of the reference oscillator is divided by 2 before being sent to the phase detector. With a 16 MHz crystal, this provides a reference frequency of 8 MHz. Although this data sheet illustrates functionality only for a 16 MHz crystal, Table 9, any crystal in the 10 - 20 MHz range can be used, Table 11.

The VCO within the PLL operates over a range of 400 to 800 MHz. Its output is scaled by a divider, M divider, that is configured by either the serial or parallel interfaces. The output of this loop divider is also applied to the phase detector.

The phase detector and the loop filter force the VCO output frequency to be M times the reference frequency by adjusting the VCO control voltage. Note that for some values of M (either too high or too low), the PLL will not achieve loop lock.

The output of the VCO is also passed through an output divider before being sent to the PECL output driver. This N output divider is configured through either the serial or the parallel interfaces and can provide one of four division ratios (1, 2, 4, or 8). This divider extends the performance of the part while providing a 50% duty cycle.

The output driver is driven differentially from the output divider and is capable of driving a pair of transmission lines terminated into 50 Ω to V_{CC} - 2.0 V. The positive reference for the output driver and the internal logic is separated from the power supply for the phase-locked loop to minimize noise induced jitter.

The configuration logic has two sections: serial and parallel. The parallel interface uses the values at the M[6:0] and N[1:0] inputs to configure the internal counters. Normally upon system reset, the $\overline{\text{P\_LOAD}}$ input is held LOW until sometime after power becomes valid. On the LOW-to-HIGH transition of $\overline{\text{P\_LOAD}}$, the parallel inputs are captured. The parallel interface has priority over the serial interface. Internal pullup resistors are provided on the M[6:0] and N[1:0] inputs to reduce component count in the application of the chip.

The serial interface logic is implemented with a fourteen bit shift register scheme. The register shifts once per rising edge of the S_CLOCK input. The serial input S_DATA must meet setup and hold timing as specified in the AC Characteristics section of this document. With P_LOAD held high, the configuration latches will capture the value of the shift register on the HIGH-to-LOW edge of the S_LOAD input. See the programming section for more information.

The TEST output reflects various internal node values and is controlled by the T[2:0] bits in the serial data stream. See the programming section for more information.

Table 9. Programming VCO Frequency Function Table with 16 MHz Crystal

VCO Frequency (MHz)	M Count Divisor	64	32	16	8	4	2	1
		M6	M5	M4	M3	M2	M1	M0
400	25	0	0	1	1	0	0	1
416	26	0	0	1	1	0	1	0
432	27	0	0	1	1	0	1	1
448	28	0	0	1	1	1	0	0
•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•
752	47	0	1	0	1	1	1	1
768	48	0	1	1	0	0	0	0
784	49	0	1	1	0	0	0	1
800	50	0	1	1	0	0	1	0

PROGRAMMING INTERFACE

Programming the NBC12439 and NBC12439A is accomplished by properly configuring the internal dividers to produce the desired frequency at the outputs. The output frequency can by represented by this formula:

$$F_{OUT} = \left((F_{XTAL} \text{ or } FREF\_EXT \div 2) \times 2\,M\right) \div N \qquad \text{(eq. 1)}$$

This can be simplified to:

$$F_{OUT} = \left((F_{XTAL} \text{ or } FREF\_EXT) \times M\right) \div N \qquad \text{(eq. 2)}$$

where F_{XTAL} is the crystal frequency, M is the loop divider modulus, and N is the output divider modulus. Note that it is possible to select values of M such that the PLL is unable to achieve loop lock. To avoid this, always make sure that M is selected to be 25 ≤ M ≤ 50 for a 16 MHz input reference. See Table 11.

Assuming that a 16 MHz reference frequency is used the above equation reduces to:

$$F_{OUT} = 16M \div N \qquad \text{(eq. 3)}$$

Substituting the four values for N (1, 2, 4, 8) yields:

Table 10. Programmable Output Divider Function Table

N1	N0	N Divider	F_{OUT}	Output Frequency Range (MHz)*	F_{OUT} Step
1	1	÷1	M × 16	400-800	16 MHz
0	0	÷2	M × 8	200-400	8 MHz
0	1	÷4	M × 4	100-200	4 MHz
1	0	÷8	M × 2	50-100	2 MHz

*For crystal frequency of 16 MHz.

The user can identify the proper M and N values for the desired frequency from the above equations. The four output frequency ranges established by N are 400-800 MHz, 200 - 400 MHz, 100 - 200 MHz and 50 - 100 MHz, respectively. From these ranges, the user will establish the value of N required. The value of M can then be calculated based on Equation 1. For example, if an output frequency of 384 MHz was desired, the following steps would be taken to identify the appropriate M and N values. 384 MHz falls within the frequency range set by an N value of 2; thus, N [1:0] = 00. For N = 2, F_{OUT} = 8M and M = F_{OUT} ÷ 8. Therefore, M = 384 ÷ 8 = 48, so M[6:0] = 0110000. Following this same procedure, a user can generate a selected frequency. The size of the programmable frequency steps of F_{OUT} will be equal to F_{XTAL} ÷ N.

For input reference frequencies other than 16 MHz, see Table 11, which shows the usable VCO frequency and M divider range.

The input frequency and the selection of the feedback divider M is limited by the VCO frequency range and fXTAL. M must be configured to match the VCO frequency range of 400 to 800 MHz in order to achieve stable PLL operation.

$$M_{min} = f_{VCOmin} \div F_{XTAL} \text{ and} \qquad \text{(eq. 4)}$$

$$M_{max} = f_{VCOmax} \div F_{XTAL} \qquad \text{(eq. 5)}$$

The value for M falls within the constraints set for PLL stability. If the value for M fell outside of the valid range, a different N value would be selected to move M in the appropriate direction.

The M and N counters can be loaded either through a parallel or serial interface. The parallel interface is controlled via the $\overline{\text{P\_LOAD}}$ signal such that a LOW to HIGH transition will latch the information present on the M[6:0] and N[1:0] inputs into the M and N counters. When the $\overline{\text{P\_LOAD}}$ signal is LOW, the input latches will be transparent and any changes on the M[6:0] and N[1:0] inputs will affect the FOUT output pair. To use the serial port, the S_CLOCK signal samples the information on the S_DATA line and loads it into a 12 bit shift register. Note that the $\overline{\text{P\_LOAD}}$ signal must be HIGH for the serial load operation to function. The Test register is loaded with the first three bits, the N register with the next two, and the M register with the final nine bits of the data stream on the S_DATA input. For each register, the most significant bit is loaded first (T2, N1, and M6). The HIGH to LOW transition on the S_LOAD input will latch the new divide values into the counters. A pulse on the S_LOAD pin after the shift register is fully loaded will transfer the divide values into the counters. Figures 5 and 6 illustrate the timing diagram for both a parallel and a serial load of the device synthesizer.

M[6:0] and N[1:0] are normally specified after power-up through the parallel interface, and then possibly, fine tuned again through the serial interface. This approach allows the application to ramp up at one frequency and then change or fine-tune the clock as the ability to control the serial interface becomes available.

The TEST output provides visibility for one of the several internal nodes as determined by the T[2:0] bits in the serial configuration stream. It is not configurable through the parallel interface. The T2, T1, and T0 control bits are preset to '000' when $\overline{\text{P\_LOAD}}$ is LOW so that the PECL FOUT outputs are as jitter-free as possible. Any active signal on the TEST output pin will have detrimental affects on the jitter of the PECL output pair. In normal operations, jitter specifications are only guaranteed if the TEST output is static. The serial configuration port can be used to select one of the alternate functions for this pin.

Table 11. Frequency Operating Range

VCO Frequency (MHz) Range for a Crystal Frequency (MHz) of:								Output Frequency (MHz) for fXTAL = 16 MHz and for N =			
M	**M[6:0]**	**10**	**12**	**14**	**16**	**18**	**20**	**÷ 1**	**÷ 2**	**÷ 4**	**÷ 8**
20	0010100						400				
21	0010101						420				
22	0010110						440				
23	0010111					414	460				
24	0011000					432	480				
25	0011001				400	450	500	400	200	100	50
26	0011010				416	468	520	416	208	104	52
27	0011011				432	486	540	432	216	108	54
28	0011100				448	504	560	448	224	112	56
29	0011101			406	464	522	580	464	232	116	58
30	0011110			420	480	540	600	480	240	120	60
31	0011111			434	496	558	620	496	248	124	62
32	0100000			448	512	576	640	512	256	128	64
33	0100001			462	528	594	660	528	264	132	66
34	0100010		408	476	544	612	680	544	272	136	68
35	0100011		420	490	560	630	700	560	280	140	70
36	0100100		432	504	576	648	720	576	288	144	72
37	0100101		444	518	592	666	740	592	296	148	74
38	0100110		456	532	608	684	760	608	304	152	76
39	0100111		468	546	624	702	780	624	312	156	78
40	0101000	400	480	560	640	720	800	640	320	160	80
41	0101001	410	492	574	656	738		656	328	164	82
42	0101010	420	504	588	672	756		672	336	168	84
43	0101011	430	516	602	688	774		688	344	172	86
44	0101100	440	528	616	704	792		704	352	176	88
45	0101101	450	540	630	720			720	360	180	90
46	0101110	460	552	644	736			736	368	184	92
47	0101111	470	564	658	752			752	376	188	94
48	0110000	480	576	672	768			768	384	192	96
49	0110001	490	588	686	784			784	392	196	98
50	0110010	500	600	700	800			800	400	200	100
51	0110011	510	612	714							
52	0110100	520	624	728							
53	0110101	530	636	742							
54	0110110	540	648	756							
55	0110111	550	660	770							
56	0111000	560	672	784							
57	0111001	570	684	798							
58	0111010	580	696								
59	0111011	590	708								
60	0111100	600	720								
61	0111101	610	732								
62	0111110	620	744								
63	0111111	630	756								
64	1000000	640	768								
65	1000001	650	780								
66	1000010	660	792								
67	1000011	670									
68	1000100	680									
69	1000101	690									
70	1000110	700									
71	1000111	710									
72	1001000	720									
73	1001001	730									
74	1001010	740									
75	1001011	750									
76	1001100	760									
77	1001101	770									
78	1001110	780									
79	1001111	790									
80	1010000	800									

Most of the signals available on the TEST output pin are useful only for performance verification of the device itself. However, the PLL bypass mode may be of interest at the board level for functional debug. When T[2:0] is set to 110, the device is placed in PLL bypass mode. In this mode the S_CLOCK input is fed directly into the M and N dividers. The N divider drives the FOUT differential pair and the M counter drives the TEST output pin. In this mode the S_CLOCK input could be used for low speed board level functional test or debug. Bypassing the PLL and driving FOUT directly gives the user more control on the test clocks sent through the clock tree. Figure 7 shows the functional setup of the PLL bypass mode. Because the S_CLOCK is a CMOS level the input frequency is limited to 250 MHz or less. This means the fastest the FOUT pin can be toggled via the S_CLOCK is 250 MHz as the minimum divide ratio of the N counter is 1. Note that the M counter output on the TEST output will not be a 50% duty cycle due to the way the divider is implemented.

T2	T1	T0	TEST OUTPUT
0	0	0	SHIFT REGISTER OUT
0	0	1	HIGH
0	1	0	FREF
0	1	1	M COUNTER OUT
1	0	0	FOUT
1	0	1	LOW
1	1	0	PLL BYPASS
1	1	1	FOUT ÷ 4

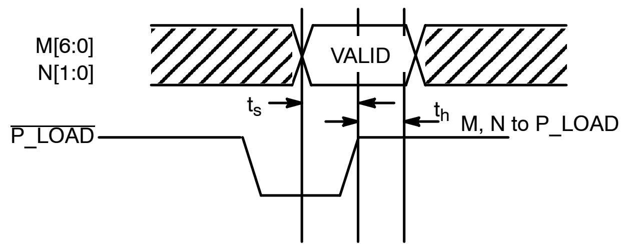


Figure 5. Parallel Interface Timing Diagram

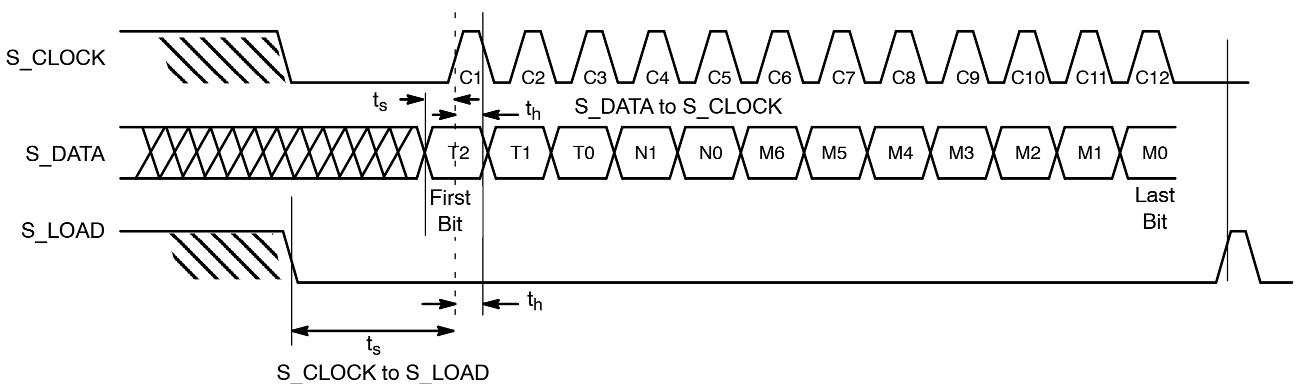
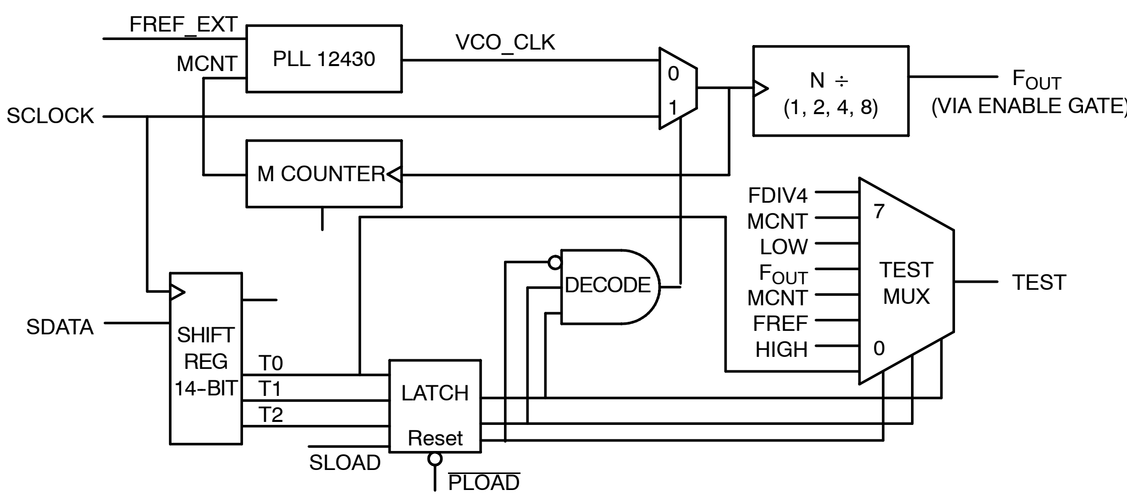


Figure 6. Serial Interface Timing Diagram



- T2=T1=1, T0=0: Test Mode
- SCLOCK is selected, MCNT is on TEST output, SCLOCK ÷ N is on FOUT pin.

PLOAD acts as reset for test pin latch. When latch reset, T2 data is shifted out TEST pin.

Figure 7. Serial Test Clock Block Diagram

APPLICATIONS INFORMATION

Using the On-Board Crystal Oscillator

The NBC12439 and NBC12439A feature a fully integrated on-board crystal oscillator to minimize system implementation costs. The oscillator is a series resonant, multivibrator type design as opposed to the more common parallel resonant oscillator design. The series resonant design provides better stability and eliminates the need for large on chip capacitors. The oscillator is totally self contained so that the only external component required is the crystal. As the oscillator is somewhat sensitive to loading on its inputs, the user is advised to mount the crystal as close to the device as possible to avoid any board level parasitics. To facilitate co-location, surface mount crystals are recommended, but not required. Because the series resonant design is affected by capacitive loading on the crystal terminals, loading variation introduced by crystals from different vendors could be a potential issue. For crystals with a higher shunt capacitance, it may be required to place a resistance across the terminals to suppress the third harmonic. Although typically not required, it is a good idea to layout the PCB with the provision of adding this external resistor. The resistor value will typically be between 500 Ω and 1 KΩ.

The oscillator circuit is a series resonant circuit and thus, for optimum performance, a series resonant crystal should be used. Unfortunately, most crystals are characterized in a parallel resonant mode. Fortunately, there is no physical difference between a series resonant and a parallel resonant crystal. The difference is purely in the way the devices are characterized. As a result, a parallel resonant crystal can be used with the device with only a minor error in the desired frequency. A parallel resonant mode crystal used in a series resonant circuit will exhibit a frequency of oscillation a few hundred ppm lower than specified (a few hundred ppm translates to kHz inaccuracy). Table 12 below specifies the performance requirements of the crystals to be used with the device.

Table 12. Crystal Specifications

Parameter	Value
Crystal Cut	Fundamental AT Cut
Resonance	Series Resonance*
Frequency Tolerance	±75 ppm at 25°C
Frequency/Temperature Stability	±150 ppm 0 to 70°C
Operating Range	0 to 70°C
Shunt Capacitance	5-7 pF
Equivalent Series Resistance (ESR)	50 to 80 Ω
Correlation Drive Level	100 μW
Aging	5 ppm/Yr (First 3 Years)

* See accompanying text for series versus parallel resonant discussion.

Power Supply Filtering

The NBC12439 and NBC12439A are mixed analog/digital products and as such, exhibit some sensitivities that would not necessarily be seen on a fully digital product. Analog circuitry is naturally susceptible to random noise, especially if this noise is seen on the power supply pins. The NBC12439 and NBC1239A provide separate power supplies for the digital circuitry (V_{CC}) and the internal PLL (PLL_V_{CC}) of the device. The purpose of this design technique is to try and isolate the high switching noise of the digital outputs from the relatively sensitive internal analog phase-locked loop. In a controlled environment such as an evaluation board, this level of isolation is sufficient. However, in a digital system environment where it is more difficult to minimize noise on the power supplies, a second level of isolation may be required. The simplest form of isolation is a power supply filter on the PLL_V_{CC} pin for the NBC12439 and NBC12349A.

Figure 8 illustrates a typical power supply filter scheme. The NBC12439 and NBC12439A are most susceptible to noise with spectral content in the 1 KHz to 1 MHz range. Therefore, the filter should be designed to target this range. The key parameter that needs to be met in the final filter design is the DC voltage drop that will be seen between the V_{CC} supply and the PLL_V_{CC} pin of the NBC12439 and NBC12439A. From the data sheet, the PLL_V_{CC} current (the current sourced through the PLL_V_{CC} pin) is typically 23 mA (28 mA maximum). Assuming that a minimum of 2.8 V must be maintained on the PLL_V_{CC} pin, very little DC voltage drop can be tolerated when a 3.3 V V_{CC} supply is used. The resistor shown in Figure 8 must have a resistance of 10-15 Ω to meet the voltage drop criteria. The RC filter pictured will provide a broadband filter with approximately 100:1 attenuation for noise whose spectral content is above 20 KHz. As the noise frequency crosses the series resonant point of an individual capacitor, it's overall impedance begins to look inductive and thus increases with increasing frequency. The parallel capacitor combination shown ensures that a low impedance path to ground exists for frequencies well above the bandwidth of the PLL.

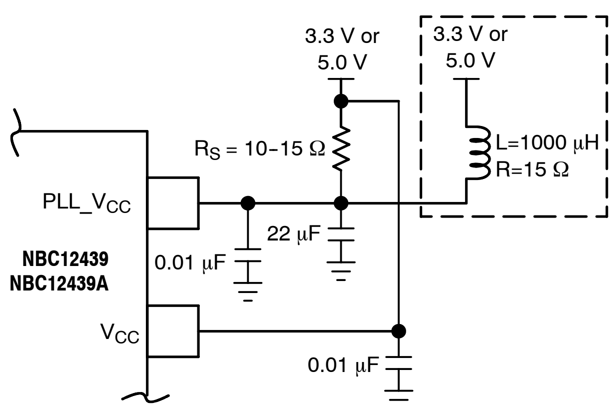


Figure 8. Power Supply Filter

A higher level of attenuation can be achieved by replacing the resistor with an appropriate valued inductor. Figure 8 shows a 1000 μH choke. This value choke will show a significant impedance at 10 KHz frequencies and above. Because of the current draw and the voltage that must be maintained on the PLL_V_{CC} pin, a low DC resistance inductor is required (less than 15 Ω). Generally, the resistor/capacitor filter will be cheaper, easier to implement, and provide an adequate level of supply filtering.

The NBC12439 and NBC12439A provide sub-nanosecond output edge rates and therefore a good power supply bypassing scheme is a must. Figure 9 shows a representative board layout for the NBC12439. There exists many different potential board layouts and the one pictured is but one. The important aspect of the layout in Figure 9 is the low impedance connections between V_{CC} and GND for the bypass capacitors. Combining good quality general purpose chip capacitors with good PCB layout techniques will produce effective capacitor resonances at frequencies adequate to supply the instantaneous switching current for the NBC12439 and NBC12439A outputs. It is imperative that low inductance chip capacitors are used. It is equally important that the board layout not introduce any of the inductance saved by using the leadless capacitors. Thin interconnect traces between the capacitor and the power plane should be avoided and multiple large vias should be used to tie the capacitors to the buried power planes. Fat interconnect and large vias will help to minimize layout induced inductance and thus maximize the series resonant point of the bypass capacitors.

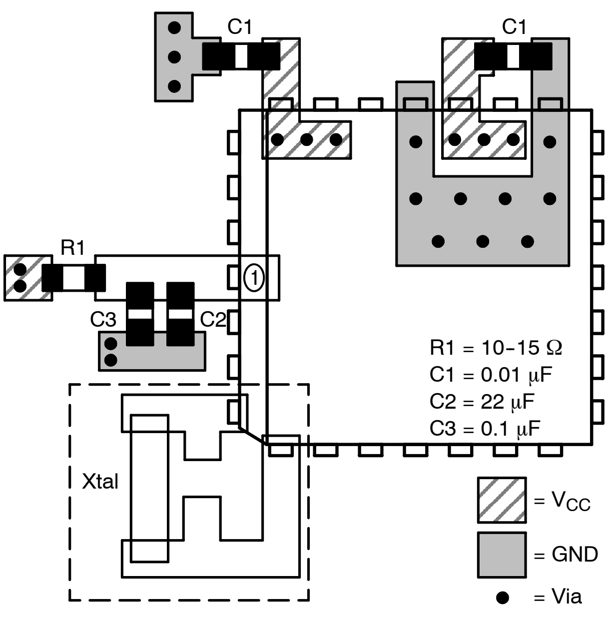


Figure 9. PCB Board Layout for (PLCC-28)

Note the dotted lines circling the crystal oscillator connection to the device. The oscillator is a series resonant circuit and the voltage amplitude across the crystal is relatively small. It is imperative that no actively switching signals cross under the crystal as crosstalk energy coupled to these lines could significantly impact the jitter of the device. Special attention should be paid to the layout of the crystal to ensure a stable, jitter free interface between the crystal and the on-board oscillator. Note the provisions for placing a resistor across the crystal oscillator terminals as discussed in the crystal oscillator section of this data sheet.

Although the NBC12439 and NBC12439A have several design features to minimize the susceptibility to power supply noise (isolated power and grounds and fully differential PLL), there still may be applications in which overall performance is being degraded due to system power supply noise. The power supply filter and bypass schemes discussed in this section should be adequate to eliminate power supply noise-related problems in most designs.

Jitter Performance

Jitter is a common parameter associated with clock generation and distribution. Clock jitter can be defined as the deviation in a clock's output transition from its ideal position.

Cycle-to-Cycle Jitter (short-term) is the period variation between adjacent periods over a defined number of observed cycles. The number of cycles observed is application dependent but the JEDEC specification is 1000 cycles. See Figure 10.

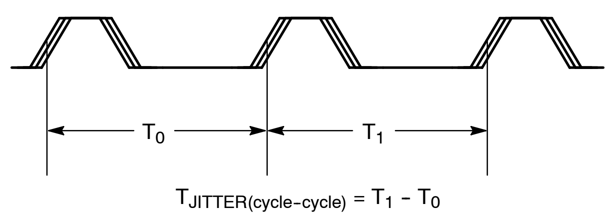


Figure 10. Cycle-to-Cycle Jitter

Random Peak-to-Peak Jitter is the difference between the highest and lowest acquired value and is represented as the width of the Gaussian base. See Figure 11.

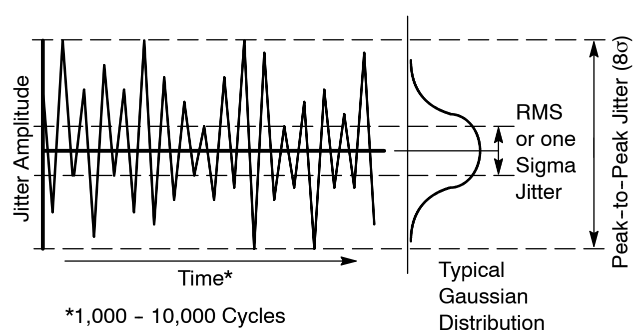


Figure 11. Random Peak-to-Peak and RMS Jitter

There are different ways to measure jitter and often they are confused with one another. An earlier method of measuring jitter is to look at the timing signal with an oscilloscope and observe the variations in period-to-period or cycle-to-cycle. If the scope is set up to trigger on every rising or falling edge, set to infinite persistence mode and allowed to trace sufficient cycles, it is possible to determine the maximum and minimum periods of the timing signal. Digital scopes can accumulate a large number of cycles, create a histogram of the edge placements and record peak-to-peak as well as standard deviations of the jitter. Care must be taken that the measured edge is the edge immediately following the trigger edge. These scopes can also store a finite number of period durations and post-processing software can analyze the data to find the maximum and minimum periods.

Recent hardware and software developments have resulted in advanced jitter measurement techniques. The Tektronix TDS-series oscilloscopes have superb jitter analysis capabilities on non-contiguous clocks with their histogram and statistics capabilities. The Tektronix TDSJIT2/3 Jitter Analysis software provides many key timing parameter measurements and will extend that capability by making jitter measurements on contiguous clock and data cycles from single-shot acquisitions.

M1 by Amherst was used as well and both test methods correlated.

This test process can be correlated to earlier test methods and are more accurate. All of the jitter data reported on the NBC12439 and NBC12439A was collected in this manner. Figure 12 shows the RMS jitter performance as a function of the VCO frequency range. The general trend is that as the VCO frequency is increased, the RMS output jitter will decrease.

Figure 13 illustrates the RMS jitter performance versus the output frequency. Note the jitter is a function of both the output frequency as well as the VCO frequency. However, the VCO frequency shows a much stronger dependence.

Long-Term Period Jitter is the maximum jitter observed at the end of a period's edge when compared to the position of the perfect reference clock's edge and is specified by the number of cycles over which the jitter is measured. The number of cycles used to look for the maximum jitter varies by application but the JEDEC spec is 10,000 observed cycles.

The NBC12439 and NBC12439A exhibit long term and cycle-to-cycle jitter, which rivals that of SAW based oscillators. This jitter performance comes with the added flexibility associated with a synthesizer over a fixed frequency oscillator. The jitter data presented should provide users with enough information to determine the effect on their overall timing budget. The jitter performance meets the needs of most system designs while adding the flexibility of frequency margining and field upgrades. These features are not available with a fixed frequency SAW oscillator.

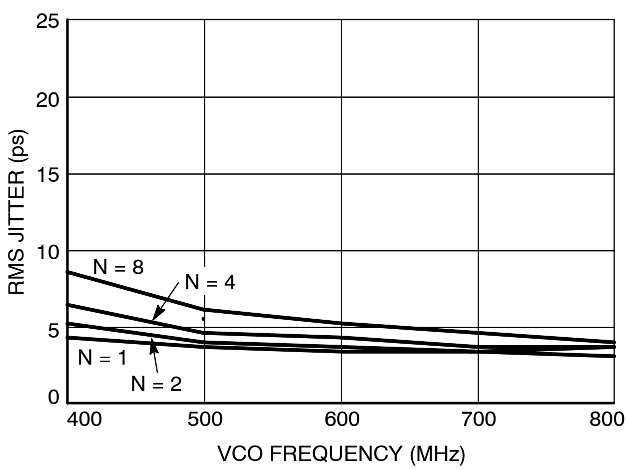


Figure 12. Cycle-to-Cycle RMS Jitter vs. VCO Frequency

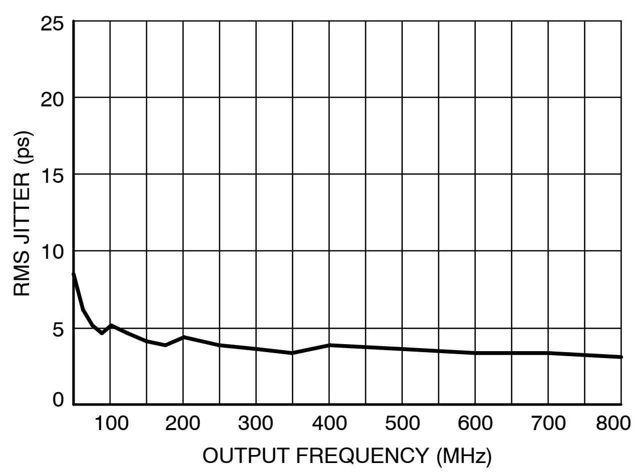


Figure 13. Cycle-to-Cycle RMS Jitter vs. Output Frequency

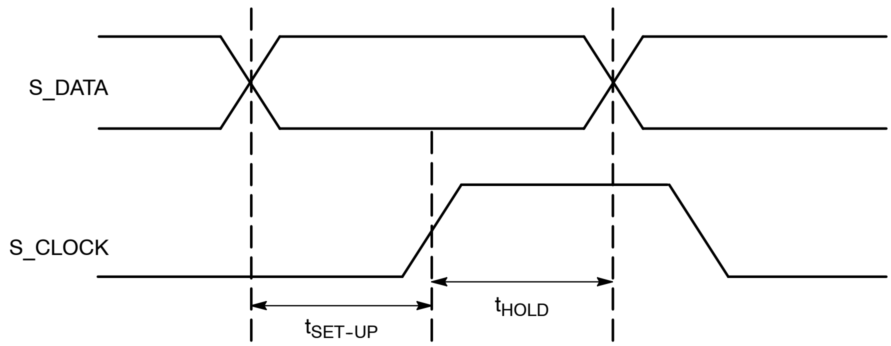


Figure 14. Setup and Hold

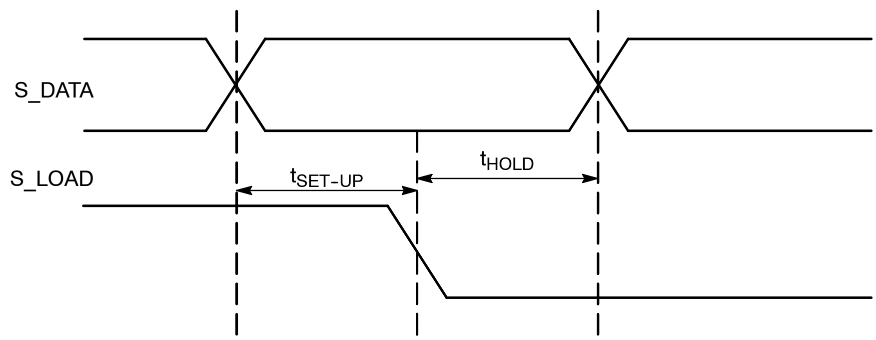


Figure 15. Setup and Hold

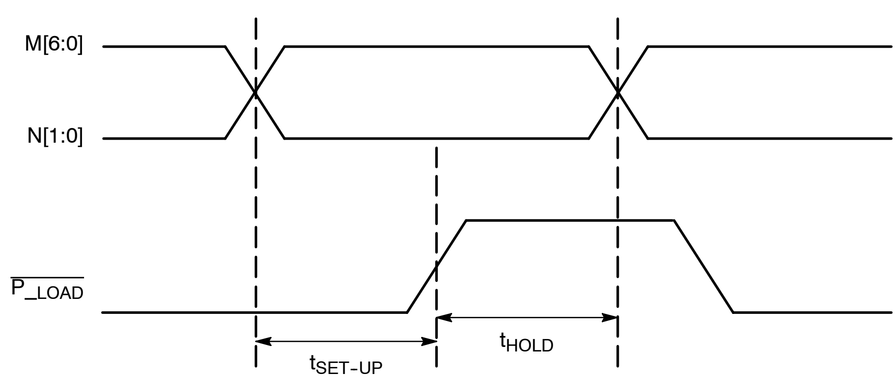


Figure 16. Setup and Hold

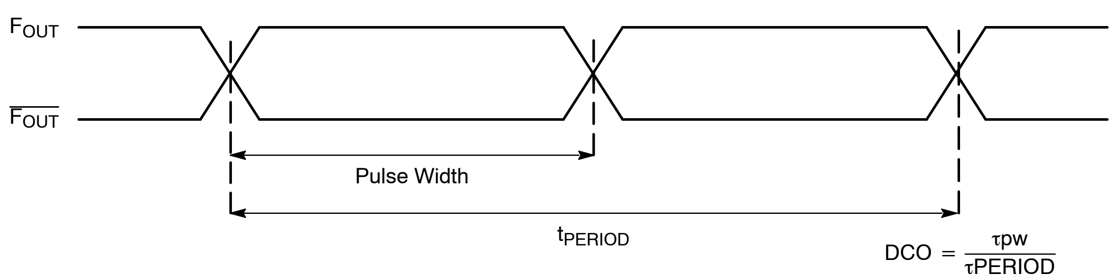


Figure 17. Output Duty Cycle

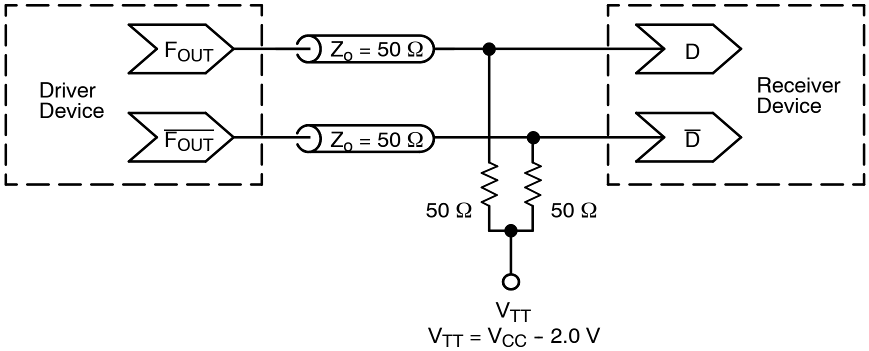


Figure 18. Typical Termination for Output Driver and Device Evaluation (See Application Note AND8020/D − Termination of ECL Logic Devices.)

ORDERING INFORMATION

Device	Package	Shipping†
NBC12439FA	LQFP−32	250 Units / Tray
NBC12439FAG	LQFP−32 (Pb−Free)	250 Units / Tray
NBC12439FAR2	LQFP−32	2000 / Tape & Reel
NBC12439FAR2G	LQFP−32 (Pb−Free)	2000 / Tape & Reel
NBC12439FN	PLCC−28	37 Units / Rail
NBC12439FNG	PLCC−28 (Pb−Free)	37 Units / Rail
NBC12439FNR2	PLCC−28	500 / Tape & Reel
NBC12439FNR2G	PLCC−28 (Pb−Free)	500 / Tape & Reel
NBC12439AFA	LQFP−32	250 Units / Tray
NBC12439AFAG	LQFP−32 (Pb−Free)	250 Units / Tray
NBC12439AFAR2	LQFP−32	2000 / Tape & Reel
NBC12439AFAR2G	LQFP−32 (Pb−Free)	2000 / Tape & Reel
NBC12439AFN	PLCC−28	37 Units / Rail
NBC12439AFNG	PLCC−28 (Pb−Free)	37 Units / Rail
NBC12439AFNR2	PLCC−28	500 / Tape & Reel
NBC12439AFNR2G	PLCC−28 (Pb−Free)	500 / Tape & Reel
NBC12439AMNG	QFN−32 (Pb−Free)	74 Units / Rail
NBC12439AMNR4G	QFN−32 (Pb−Free)	1000 / Tape & Reel

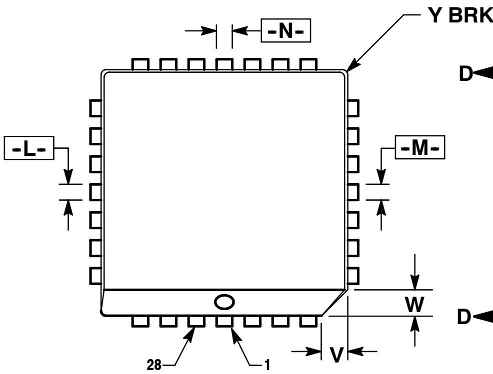
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

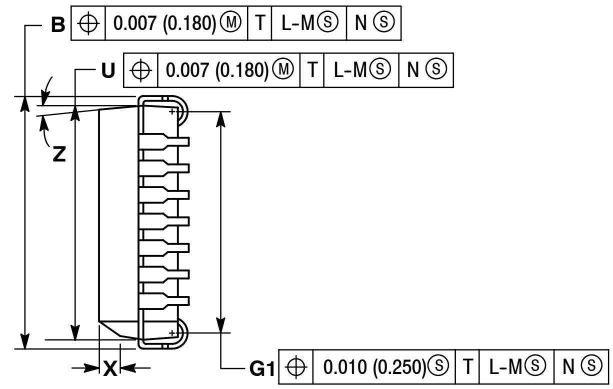
Resource Reference of Application Notes

AN1405/D	–	ECL Clock Distribution Techniques
AN1406/D	–	Designing with PECL (ECL at +5.0 V)
AN1503/D	–	ECLinPS™ I/O SPiCE Modeling Kit
AN1504/D	–	Metastability and the ECLinPS Family
AN1568/D	–	Interfacing Between LVDS and ECL
AN1672/D	–	The ECL Translator Guide
AND8001/D	–	Odd Number Counters Design
AND8002/D	–	Marking and Date Codes
AND8020/D	–	Termination of ECL Logic Devices
AND8066/D	–	Interfacing with ECLinPS
AND8090/D	–	AC Characteristics of ECL Devices

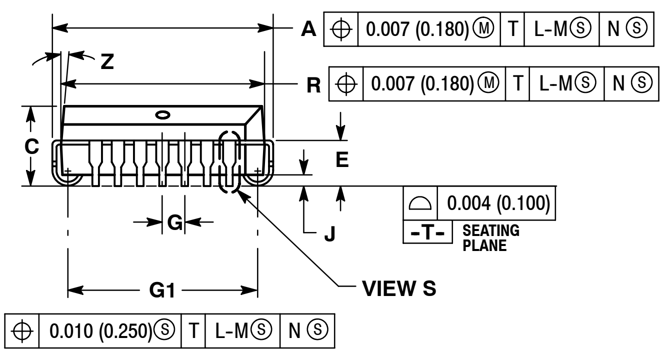
PACKAGE DIMENSIONS

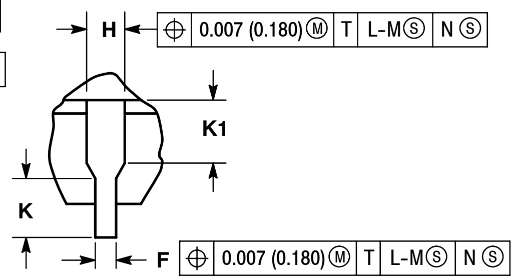
PLCC-28
FN SUFFIX
PLASTIC PLCC PACKAGE
CASE 776-02
ISSUE E





VIEW D-D





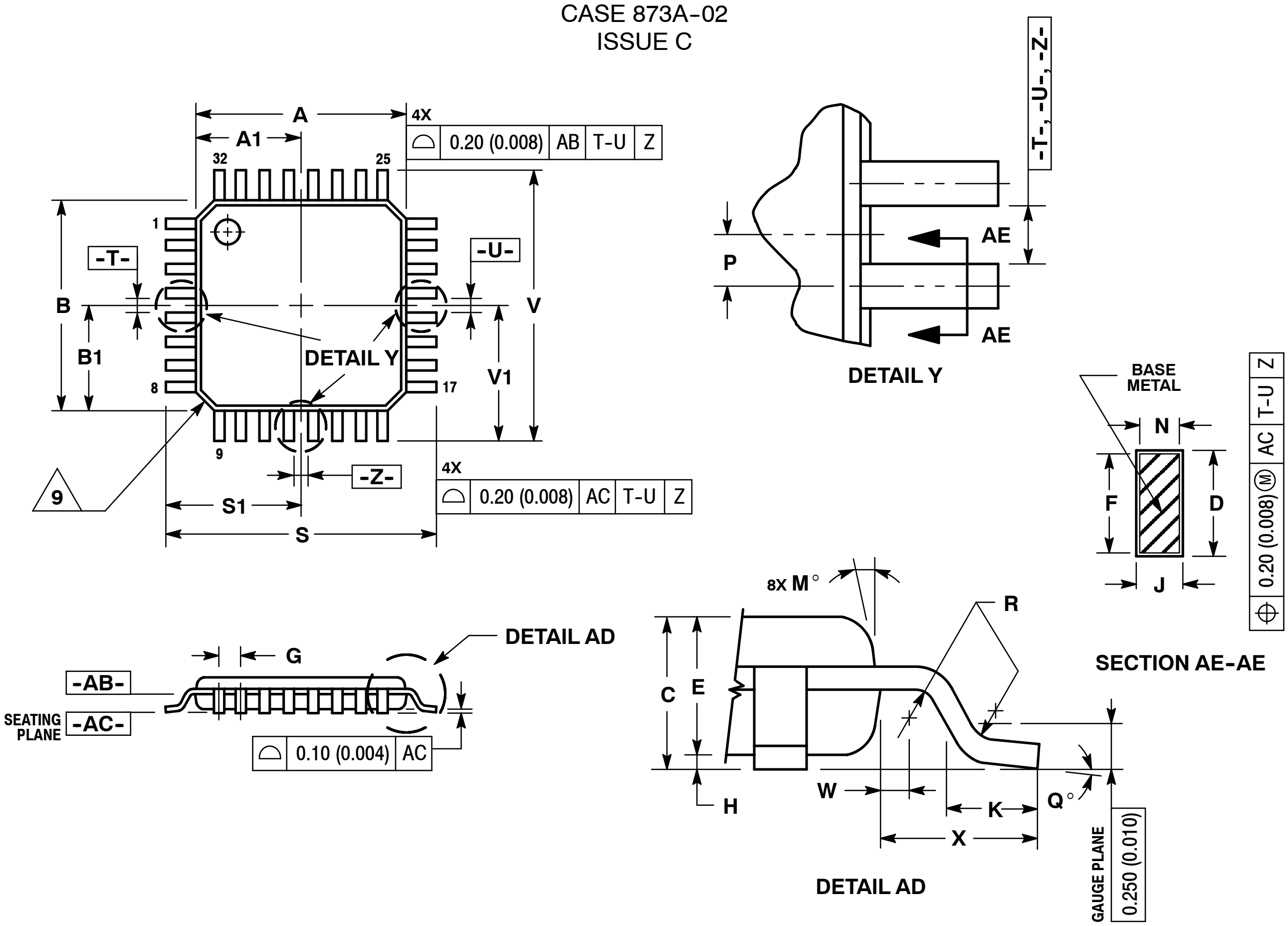
VIEW S

NOTES:
1. DATUMS -L-, -M-, AND -N- DETERMINED WHERE TOP OF LEAD SHOULDER EXITS PLASTIC BODY AT MOLD PARTING LINE.
2. DIMENSION G1, TRUE POSITION TO BE MEASURED AT DATUM -T-, SEATING PLANE.
3. DIMENSIONS R AND U DO NOT INCLUDE MOLD FLASH. ALLOWABLE MOLD FLASH IS 0.010 (0.250) PER SIDE.
4. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
5. CONTROLLING DIMENSION: INCH.
6. THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM BY UP TO 0.012 (0.300). DIMENSIONS R AND U ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTERLEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.
7. DIMENSION H DOES NOT INCLUDE DAMBAR PROTRUSION OR INTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE GREATER THAN 0.037 (0.940). THE DAMBAR INTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE SMALLER THAN 0.025 (0.635).

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.485	0.495	12.32	12.57
B	0.485	0.495	12.32	12.57
C	0.165	0.180	4.20	4.57
E	0.090	0.110	2.29	2.79
F	0.013	0.019	0.33	0.48
G	0.050 BSC		1.27 BSC	
H	0.026	0.032	0.66	0.81
J	0.020	---	0.51	---
K	0.025	---	0.64	---
R	0.450	0.456	11.43	11.58
U	0.450	0.456	11.43	11.58
V	0.042	0.048	1.07	1.21
W	0.042	0.048	1.07	1.21
X	0.042	0.056	1.07	1.42
Y	---	0.020	---	0.50
Z	2°	10°	2°	10°
G1	0.410	0.430	10.42	10.92
K1	0.040	---	1.02	---

PACKAGE DIMENSIONS

32 LEAD LQFP
CASE 873A-02
ISSUE C

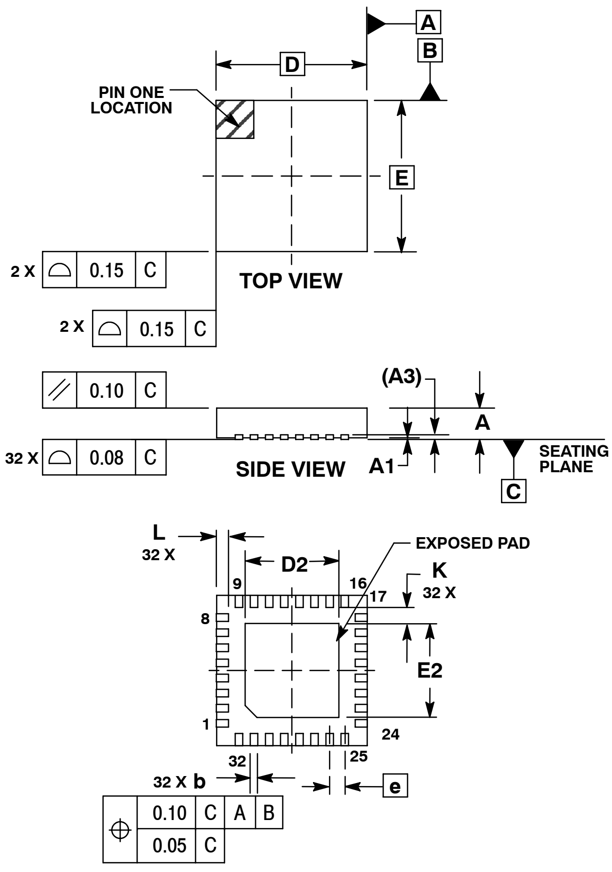


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DATUM PLANE -AB- IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS -T-, -U-, AND -Z- TO BE DETERMINED AT DATUM PLANE -AB-.
5. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE -AC-.
6. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.250 (0.010) PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE -AB-.
7. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL NOT CAUSE THE D DIMENSION TO EXCEED 0.520 (0.020).
8. MINIMUM SOLDER PLATE THICKNESS SHALL BE 0.0076 (0.0003).
9. EXACT SHAPE OF EACH CORNER MAY VARY FROM DEPICTION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	7.000 BSC		0.276 BSC	
A1	3.500 BSC		0.138 BSC	
B	7.000 BSC		0.276 BSC	
B1	3.500 BSC		0.138 BSC	
C	1.400	1.600	0.055	0.063
D	0.300	0.450	0.012	0.018
E	1.350	1.450	0.053	0.057
F	0.300	0.400	0.012	0.016
G	0.800 BSC		0.031 BSC	
H	0.050	0.150	0.002	0.006
J	0.090	0.200	0.004	0.008
K	0.450	0.750	0.018	0.030
M	12° REF		12° REF	
N	0.090	0.160	0.004	0.006
P	0.400 BSC		0.016 BSC	
Q	1°	5°	1°	5°
R	0.150	0.250	0.006	0.010
S	9.000 BSC		0.354 BSC	
S1	4.500 BSC		0.177 BSC	
V	9.000 BSC		0.354 BSC	
V1	4.500 BSC		0.177 BSC	
W	0.200 REF		0.008 REF	
X	1.000 REF		0.039 REF	

PACKAGE DIMENSIONS

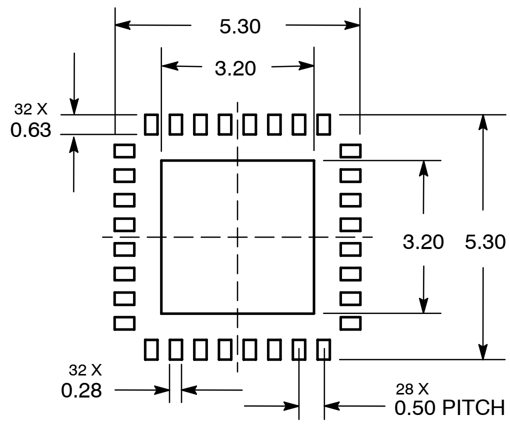
QFN32 5*5*1 0.5 P
CASE 488AM-01
ISSUE O



NOTES:
1. DIMENSIONS AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30 MM TERMINAL
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS		
DIM	MIN	NOM	MAX
A	0.800	0.900	1.000
A1	0.000	0.025	0.050
A3	0.200 REF		
b	0.180	0.250	0.300
D	5.00 BSC		
D2	2.950	3.100	3.250
E	5.00 BSC		
E2	2.950	3.100	3.250
e	0.500 BSC		
K	0.200	---	---
L	0.300	0.400	0.500

SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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