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**April 2013** 

## **FDMS8090**

# PowerTrench® Symmetrical Dual 100 V N-Channel MOSFET

#### **Features**

- Max  $r_{DS(on)} = 13 \text{ m}\Omega$  at  $V_{GS} = 10 \text{ V}$ ,  $I_D = 10 \text{ A}$
- Max  $r_{DS(on)} = 20 \text{ m}\Omega$  at  $V_{GS} = 6 \text{ V}$ ,  $I_D = 8 \text{ A}$
- Low inductance packaging shortens rise/fall times, resulting in lower switching losses
- MOSFET integration enables optimum layout for lower circuit inductance and reduced switch node ringing
- 100% UIL tested
- RoHS Compliant

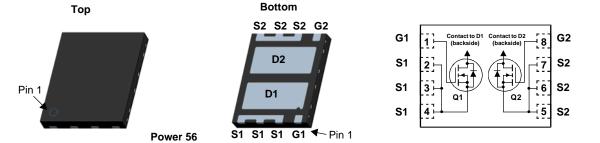


#### **General Description**

This device includes two fast switching (Qgd minimized) 100V N-Channel MOSFETs in a dual Power 56 (5 mm X 6 mm MLP) package. The package is enhanced for exceptional thermal performance.

### **Applications**

- Bridge Topologies
- Synchronous Rectifier Pair
- Motor Drives



## **MOSFET Maximum Ratings** T<sub>A</sub> = 25 °C unless otherwise noted

Symbol	Parame		Ratings	Units	
V <sub>DS</sub>	Drain to Source Voltage			100	V
$V_{GS}$	Gate to Source Voltage			±20	V
	Drain Current -Continuous	T <sub>C</sub> = 25 °C		40	
$I_D$	-Continuous	T <sub>A</sub> = 25 °C	(Note 1a)	10	Α
	-Pulsed		(Note 4)	120	
E <sub>AS</sub>	Single Pulse Avalanche Energy		(Note 3)	253	mJ
D	Power Dissipation	T <sub>C</sub> = 25 °C		59	W
$P_{D}$	Power Dissipation	T <sub>A</sub> = 25 °C	(Note 1a)	2.2	VV
T <sub>J</sub> , T <sub>STG</sub>	Operating and Storage Junction Temperature Range			-55 to +150	°C

#### Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction to Case	2.1	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	55	C/VV

#### **Package Marking and Ordering Information**

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDMS8090	FDMS8090	Power 56	13 "	12 mm	3000 units

## Electrical Characteristics T<sub>J</sub> = 25 °C unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Тур	Max	Units
Off Chara	acteristics					
BV <sub>DSS</sub>	Drain to Source Breakdown Voltage	$I_D = 250 \mu A, V_{GS} = 0 V$	100			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D$ = 250 $\mu$ A, referenced to 25 °C		70		mV/°C
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> = 80 V, V <sub>GS</sub> = 0 V			1	μΑ
I <sub>GSS</sub>	Gate to Source Leakage Current	V <sub>GS</sub> = ±20 V, V <sub>DS</sub> = 0 V			±100	nA

#### On Characteristics

V <sub>GS(th)</sub>	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}, I_{D} = 250 \mu A$	2.0	3.0	4.0	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D$ = 250 $\mu$ A, referenced to 25 °C		-10		mV/°C
		V <sub>GS</sub> = 10 V, I <sub>D</sub> = 10 A		11	13	
r <sub>DS(on)</sub>	r <sub>DS(on)</sub> Static Drain to Source On Resistance	V <sub>GS</sub> = 6 V, I <sub>D</sub> = 8 A		15	20	mΩ
` ,	$V_{GS} = 10 \text{ V}, I_D = 10 \text{ A}, T_J = 125 ^{\circ}\text{C}$		18	20		
9 <sub>FS</sub>	Forward Transconductance	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 10 A		24		S

#### **Dynamic Characteristics**

C <sub>iss</sub>	Input Capacitance			1285	1800	pF
C <sub>oss</sub>	Output Capacitance	$V_{DS} = 50 \text{ V}, V_{GS} = 0 \text{ V},$ f = 1  MHz		301	400	pF
C <sub>rss</sub>	Reverse Transfer Capacitance	1 - 1 1/11/12		16	28	pF
$R_{g}$	Gate Resistance		0.1	1.7	3.5	Ω

### **Switching Characteristics**

t <sub>d(on)</sub>	Turn-On Delay Time				10.6	21	ns
t <sub>r</sub>	Rise Time		$V_{DD} = 50 \text{ V, } I_{D} = 10 \text{ A,}$ $V_{GS} = 10 \text{ V, } R_{GEN} = 6 \Omega$		4.6	10	ns
t <sub>d(off)</sub>	Turn-Off Delay Time	V <sub>GS</sub> = 10 V, R <sub>GEN</sub> :			17.4	31	ns
t <sub>f</sub>	Fall Time				4	10	ns
$Q_g$	Total Gate Charge	V <sub>GS</sub> = 0 V to 10 V			19	27	nC
$Q_g$	Total Gate Charge	$V_{GS} = 0 V to 5 V$	$V_{DD} = 50 \text{ V},$		10	15	nC
Q <sub>gs</sub>	Gate to Source Charge		I <sub>D</sub> = 10 A		6.1		nC
$Q_{gd}$	Gate to Drain "Miller" Charge				4.1		nC

#### **Drain-Source Diode Characteristics**

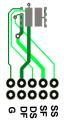
1705 Source-Drain Dione Forward Voltage	Source Drain Diode Ferward Voltage	$V_{GS} = 0 \text{ V}, I_{S} = 2 \text{ A}$ (Note 2)	0.	7 1.2	V
	$V_{GS} = 0 \text{ V, } I_S = 10 \text{ A}$ (Note 2)	0.	8 1.3	v	
t <sub>rr</sub>	Reverse Recovery Time	I <sub>E</sub> = 10 A, di/dt = 100 A/μs	4:	9 78	ns
Q <sub>rr</sub>	Reverse Recovery Charge	T <sub>F</sub> = 10 A, α/αι = 100 Α/μs	5-	4 86	nC

#### Notes

<sup>1.</sup> R<sub>0JA</sub> is determined with the device mounted on a 1 in<sup>2</sup> pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material. R<sub>0JC</sub> is guaranteed by design while R<sub>0CA</sub> is determined by the user's board design.



a. 55 °C/W when mounted on a 1 in² pad of 2 oz copper.



b. 138 °C/W when mounted on a minimum pad of 2 oz copper.

- 2. Pulse Test: Pulse Width < 300  $\mu\text{s},$  Duty cycle < 2.0%.
- 3.  $E_{AS}$  of 253 mJ is based on starting  $T_J$  = 25 °C; N-ch: L = 3 mH,  $I_{AS}$  = 13 A,  $V_{DD}$  = 100 V,  $V_{GS}$  = 10 V. 100% test at L = 0.3 mH,  $I_{AS}$  = 29 A.
- 4. Pulsed Id limited by junction temperature,td<=10uS. Please refer to SOA curve for more details.

### Typical Characteristics T<sub>J</sub> = 25 °C unless otherwise noted

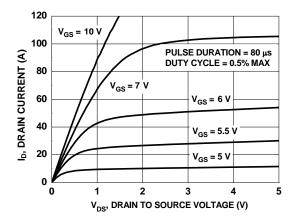


Figure 1. On Region Characteristics

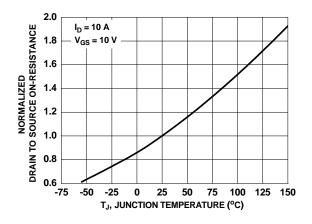


Figure 3. Normalized On Resistance vs Junction Temperature

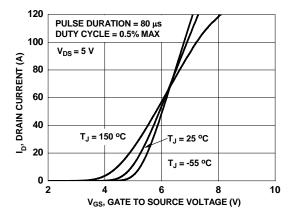


Figure 5. Transfer Characteristics

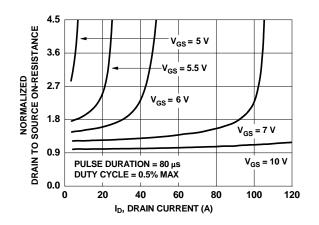


Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

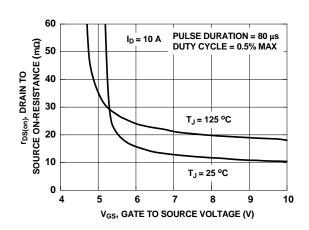


Figure 4. On-Resistance vs Gate to Source Voltage

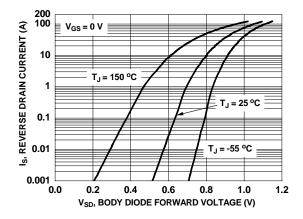


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

## **Typical Characteristics** $T_J = 25$ °C unless otherwise noted

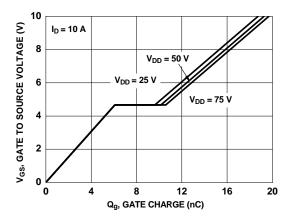


Figure 7. Gate Charge Characteristics

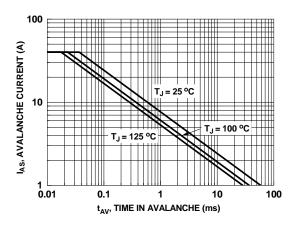


Figure 9. Unclamped Inductive Switching Capability

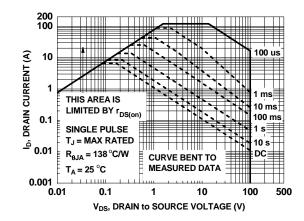


Figure 11. Forward Bias Safe Operating Area

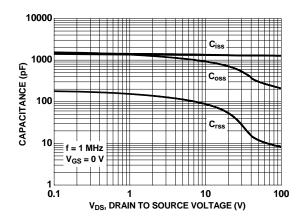


Figure 8. Capacitance vs Drain to Source Voltage

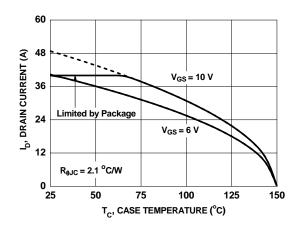


Figure 10. Maximum Continuous Drain Current vs Case Temperature

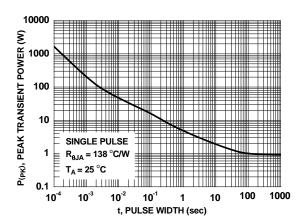


Figure 12. Single Pulse Maximum Power Dissipation

## **Typical Characteristics** $T_J = 25$ °C unless otherwise noted

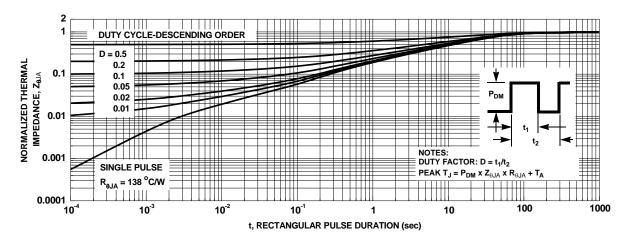
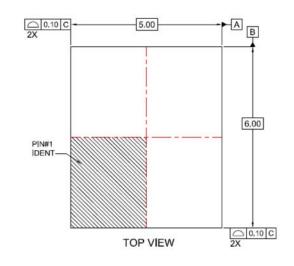
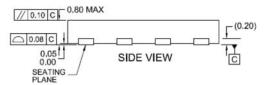
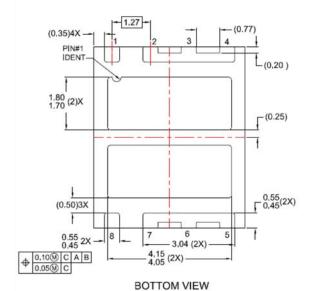


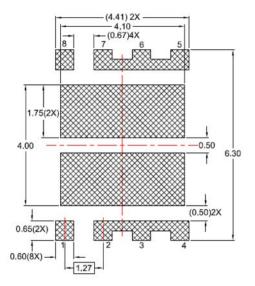
Figure 13. Junction-to-Ambient Transient Thermal Response Curve

## **Dimensional Outline and Pad Layout**









RECOMMENDED LAND PATTERN

#### NOTES:

- A. DOES NOT FULLY CONFORM TO JEDEC REGISTRATION, MO-229.
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 2009.
- D. LAND PATTERN RECOMMENDATION IS BASED ON FSC DESIGN ONLY.
- E. DRAWING FILENAME; MKT-MLP08Zrev1,





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