**Features** 



# Pin-Selectable, Hex Power-Supply **Supervisory Circuit**

#### **General Description**

The MAX6886 pin-selectable, multivoltage supply supervisor monitors six voltage-detector inputs and one watchdog input, asserting a RESET when inputs drop below the selected voltage thresholds or the watchdog timer expires. Manual reset and margin disable inputs offer additional flexibility.

Five logic inputs select the MAX6886 thresholds. Logic inputs select a supply tolerance (5% or 10%) and 1 of 32 factory-set threshold settings. Connect external capacitors or use the factory default setting to set the watchdog timeout periods and reset time delay.

The MAX6886 is available in a 20-pin TQFN (5mm x 5mm x 0.8mm) package and operates over the extended -40°C to +85°C temperature range.

### **Applications**

Multivoltage Systems

Telecom

Networking

Servers/Workstations/Storage Systems

#### ♦ 32 Pin-Selectable Undervoltage Detector Thresholds

- ♦ Capacitor-Adjustable Reset and Watchdog **Timeout Periods**
- ◆ Factory Default Reset and Watchdog Timeout
- **♦ Margining Disable and Manual Reset Controls**
- ♦ -40°C to +85°C Operating Temperature Range
- ♦ Small 5mm x 5mm 20-Pin Thin QFN Package
- **♦ Few External Components**
- ♦ ±1% Threshold Accuracy

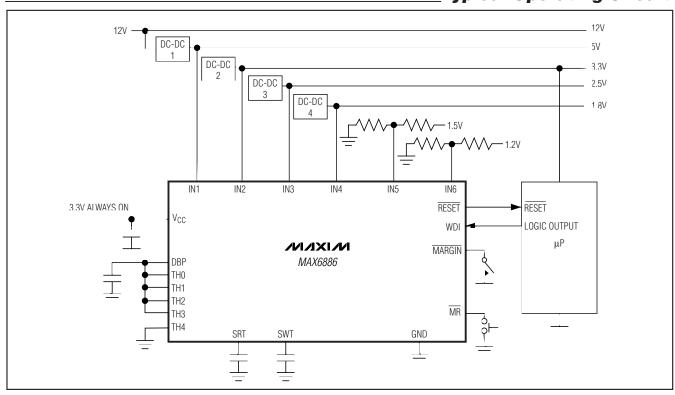
#### **Ordering Information**

PART	TEMP RANGE	PIN-PACKAGE
MAX6886ETP+	-40°C to +85°C	20 TQFN-EP*

<sup>+</sup>Denotes a lead(Pb)-free/RoHS-compliant package.

#### Pin Configuration appears at end of data sheet.

## Typical Operating Circuit



MIXIM

Maxim Integrated Products 1

#### **ABSOLUTE MAXIMUM RATINGS**

(All voltages referenced to GND.)		Maximum Junction Temperature	+150°C
IN1-IN6, V <sub>CC</sub> , RESET, SRT, SWT0.	3V to +6V	Operating Temperature Range	40°C to +85°C
TH0-TH4, WDI, MR, MARGIN0.	3V to +6V	Storage Temperature Range	65°C to +150°C
DBP0.:	3V to +3V	Lead Temperature (soldering, 10s)	+300°C
Input/Output Current (all pins)	±20mA	, ,	
Continuous Power Dissipation (T <sub>A</sub> = +70°C)			
20-Pin 5mm x 5mm Thin QFN			
(derate 21.3mW/°C above +70°C)	1702mW		

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

#### **ELECTRICAL CHARACTERISTICS**

 $(V_{IN1}-V_{IN4} \text{ or } V_{CC}=2.7V \text{ to } 5.8V, \text{WDI}=\text{GND}, \text{TH0-TH4}=\overline{\text{MARGIN}}=\overline{\text{MR}}=\text{DBP}, \text{T}_{A}=-40^{\circ}\text{C} \text{ to } +85^{\circ}\text{C}, \text{ unless otherwise noted.}$  Typical values are at T<sub>A</sub>=+25°C.) (Notes 1, 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Operating Voltage Range (Note 3)		Voltage on either one of IN1–IN4 or V <sub>CC</sub> to guarantee the part is fully operational		2.7		5.8	V
Supply Current	Icc	$V_{IN1} = 5.8V$ , IN2–IN6	= GND, no load		0.9	1.2	mA
Digital Bypass Voltage	V <sub>DBP</sub>			2.48	2.55	2.67	V
Threshold Accuracy (Table 2)	V <sub>TH</sub>	IN1-IN6, V <sub>IN</sub> _ falling	$T_A = +25^{\circ}\text{C to } +85^{\circ}\text{C}$ $T_A = -40^{\circ}\text{C to } +85^{\circ}\text{C}$	-1 -1.5		+1	% V <sub>TH</sub>
Threshold Hysteresis	V <sub>TH-H</sub> ys				0.3		% V <sub>TH</sub>
Threshold Tempco	ΔV <sub>TH</sub> /°C				10		ppm/°C
IN_ Input Impedance	R <sub>IN</sub>	For V <sub>IN_</sub> < highest V <sub>IN1-IN4</sub> and V <sub>IN_</sub> < V <sub>CC</sub> (not ADJ), thresholds are not set as adjustable			200	300	kΩ
IN_ Input Leakage Current	IIN	IN5, IN6 IN1–IN4 set as adjustable thresholds		-150		+150	nA
Power-Up Delay	t <sub>D-PO</sub>	V <sub>CC</sub> ≥ 2.5V				2.5	ms
IN_ to RESET Delay	t <sub>D-R</sub>	IN_ falling/rising, 100mV overdrive			20		μs
Reset Default Timeout Period	t <sub>RP</sub>	V <sub>SRT</sub> = V <sub>CC</sub>		180	200	220	ms
Reset Adjustable Timeout Period	t <sub>RP-ADJ</sub>	C <sub>SRT</sub> = 47nF		135	207	280	ms
SRT Adjustable Timeout Current	I <sub>SRT</sub>	V <sub>SRT</sub> = V <sub>GND</sub>		180	230	280	nA
SRT Default Timeout Threshold	V <sub>SRT-DEF</sub>	V <sub>SRT</sub> ≥ V <sub>SRT-DEF</sub> , sele	ects reset default	1.1	1.25	1.5	V
SRT Adjustable Timeout Threshold	VSRT-ADJ	(Note 4)			1.00	1.05	V
SRT Adjustable Timeout Discharge Threshold	V <sub>SRT-DIS</sub>	(Note 5)			100		mV
SRT Adjustable Timeout Output- Low Discharge Current	I <sub>SRT-DIS</sub>	V <sub>SRT</sub> = 0.3V		0.7			mA
RESET Output Low	Volreset	Isink = 4mA, output asserted				0.4	V
RESET Output Open-Drain Leakage Current	llkg	Output tri-stated				+1	μΑ

## **ELECTRICAL CHARACTERISTICS (continued)**

 $(V_{IN1}-V_{IN4} \text{ or } V_{CC}=2.7V \text{ to } 5.8V, \text{ WDI}=\text{GND}, \text{TH0-TH4}=\overline{\text{MARGIN}}=\overline{\text{MR}}=\text{DBP}, \text{T}_{A}=-40^{\circ}\text{C} \text{ to } +85^{\circ}\text{C}, \text{ unless otherwise noted.}$  Typical values are at T<sub>A</sub>=+25°C.) (Notes 1, 2)

PARAMETER	SYMBOL	CONI	DITIONS	MIN	TYP	MAX	UNITS
MR, MARGIN, TH0-TH4, WDI	VIL					0.6	V
Input Voltage	$V_{IH}$						V
MR Input Pulse Width	tMR			1			μs
MR Glitch Rejection					100		ns
MR to RESET Delay	t <sub>D-MR</sub>				200		ns
MR to Internal DBP Pullup Current	IMR	V <sub>MR</sub> = 1.4V		5	10	15	μΑ
MARGIN to Internal DBP Pullup Current	IMARGIN	V <sub>MARGIN</sub> = 1.4V		5	10	15	μΑ
TH0-TH4 Input Current				-100		+100	nA
WDI Pulldown Current	I <sub>WDI</sub>	V <sub>WDI</sub> = 0.6V		5	10	15	μΑ
WDI Input Pulse Width	twDI						ns
Watahdag Dafault Timeaut Pariod	÷	Vou. = Vo.	Initial mode	92.16	102.4	112.64	s
Watchdog Default Timeout Period	tw□	V <sub>SWT</sub> = V <sub>CC</sub>	Normal mode	1.44	1.6	1.76	S
Watchdog Adjustable Timeout	t	C <sub>SWT</sub> = 0.33µF	Initial mode	53.7	82.5	111.9	S
Period	twd-adj	CSW1 = 0.33μF	Normal mode	0.93	1.43	1.94	S
SWT Adjustable Timeout Current	Iswt	SWT = GND		180	230	280	nA
SWT Default Timeout Threshold	V <sub>SWT-DEF</sub>	V <sub>SWT</sub> ≥ V <sub>SWT-DEF</sub> , se timeout	V <sub>SWT</sub> ≥ V <sub>SWT-DEF</sub> , selects watchdog default timeout			1.5	V
SWT Adjustable Timeout Threshold	Vswt-adj	(Note 4)		0.95	1.00	1.05	V
SWT Adjustable Timeout Discharge Threshold	V <sub>SWT-DIS</sub>	(Note 5)		100		mV	
SWT Adjustable Timeout Output- Low Discharge Current	I <sub>SWT-DIS</sub>	V <sub>SWT</sub> = 0.3V		0.7			mA

Note 1: Device may be supplied from IN1-IN4 or V<sub>CC</sub>.

Note 2: 100% production tested at  $T_A = +25$ °C and  $T_A = +85$ °C. Specifications at  $T_A = -40$ °C are guaranteed by design.

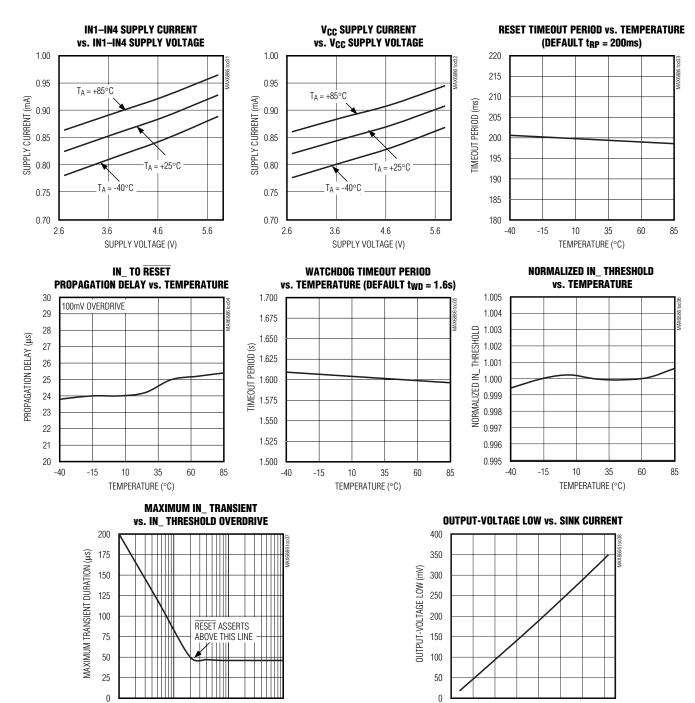
Note 3: The internal supply voltage, measured at  $V_{CC}$ , equals the maximum of IN1–IN4.

Note 4: External capacitor is charged by Is T when Vs T-DIS < Vs T < Vs T-ADJ.

Note 5: External capacitor is discharged by Is\_T-DIS down to Vs\_T-DIS after Vs\_T reaches Vs\_T-ADJ.

#### **Typical Operating Characteristics**

 $(V_{IN1}-V_{IN4} \text{ or } V_{CC} = 5V, WDI = GND, TH0-TH4 = \overline{MARGIN} = \overline{MR} = DBP, T_A = +25^{\circ}C, unless otherwise noted.)$ 



12 14

10

SINK CURRENT (mA)

2

4 6 8

0

10

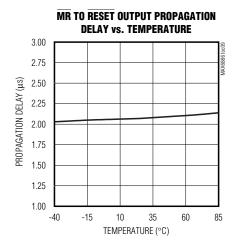
IN\_ THRESHOLD OVERDRIVE (mV)

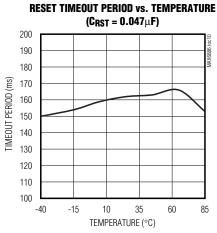
100

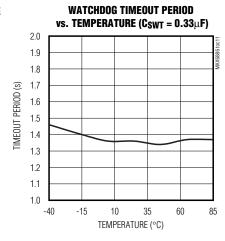
1000

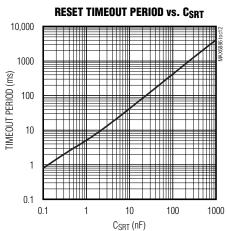
### **Typical Operating Characteristics (continued)**

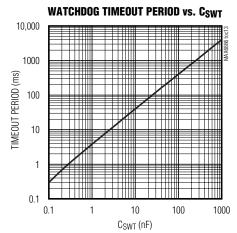
 $(V_{IN1}-V_{IN4} \text{ or } V_{CC} = 5V, WDI = GND, TH0-TH4 = \overline{MARGIN} = \overline{MR} = DBP, T_A = +25^{\circ}C, unless otherwise noted.)$ 











## **Pin Description**

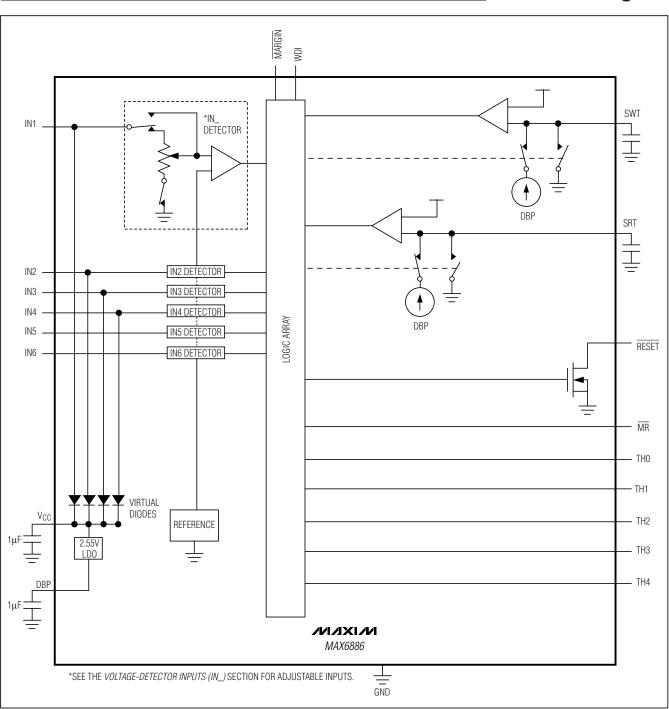
PIN	NAME	FUNCTION
1	RESET	Open-Drain, Active-Low Reset Output. RESET asserts when any input voltage falls below the selected threshold, the watchdog timer expires, or when MR is pulled low. RESET remains asserted for default (200ms) or adjustable reset timeout period after all assertion-causing conditions are cleared. An external pullup resister is required.
2	SRT	Reset Timeout Adjust Input. Connect an external capacitor between SRT and GND to set the reset timeout period. The timeout period is calculated by $t_{RP} = 4.348E6 \times C_{SRT}$ ( $t_{RP}$ in seconds and $t_{SRT}$ in Farads). To use the factory default period of 200ms connect SRT to $t_{CC}$ .
3	SWT	Watchdog Timeout Adjust Input. Connect an external capacitor between SWT and GND to set the watchdog timeout period. The adjustable timeout period is calculated by two = 4.348E6 x CswT (two in seconds and CswT in Farads). Disable the watchdog timer by connecting SWT to GND. Connect SWT to Vcc to use the factory-default normal and initial periods of 1.6s and 102.4s, respectively.

## Pin Description (continued)

PIN	NAME	FUNCTION				
4	GND	Ground				
5	WDI	Watchdog Timer Input. Logic input for the watchdog timer function. If WDI is not strobed with a valid low-to-high or high-to-low transition within the selected timeout period, RESET asserts. WDI is internally pulled down to GND through a 10µA current sink.				
6	Active-Low Manual Reset Input. Pull MR low to assert RESET. RESET will remain asserted preset/adjustable reset timeout period when MR is driven high. Leave MR unconnected DBP if unused. MR is internally pulled up to DBP through a 10µA current source.					
7	MARGIN	Margin Input. When MARGIN is pulled low, RESET is held in its existing state independent of subsequent changes in monitored input voltages or the watchdog timer expiration. MARGIN is internally pulled up to DBP through a 10µA current source. MARGIN overrides MR if both are asserted at the same time.				
8	TH4	Threshold Selection Input 4. Logic input to select desired threshold. Connect TH4 to GND or DBP. See Table 2 for available thresholds. Input has no internal pullup or pulldown.				
9	TH3	Threshold Selection Input 3. Logic input to select desired threshold. Connect TH3 to GND or DBP. See Table 2 for available thresholds. Input has no internal pullup or pulldown.				
10	TH2	Threshold Selection Input 2. Logic input to select desired threshold. Connect TH2 to GND or DBP. See Table 2 for available thresholds. Input has no internal pullup or pulldown.				
11	TH1	Threshold Selection Input 1. Logic input to select desired threshold. Connect TH1 to GND or DBP. See Table 2 for available thresholds. Input has no internal pullup or pulldown.				
12	THO	Threshold Selection Input 0. Logic input to select desired threshold. Connect TH0 to GND or DBP. See Table 2 for available thresholds. Input has no internal pullup or pulldown.				
13	Vcc	Internal Power-Supply Voltage. Bypass V <sub>CC</sub> to GND with a 1µF ceramic capacitor as close to the device as possible. V <sub>CC</sub> supplies power to the internal circuitry. V <sub>CC</sub> is internally powered from the highest of the monitored IN1–IN4 voltages. Do not use V <sub>CC</sub> to supply power to external circuitry. To externally supply V <sub>CC</sub> , see the <i>Powering the MAX6886</i> section.				
14	DBP	Digital Bypass Voltage. The internally generated voltage at DBP supplies power to internal logic and output RESET. Connect a 1µF capacitor from DBP to GND as close to the device as possible. Do not use DBP to supply power to external circuitry.				
15	IN6	Input Voltage Detector 6. Select the undervoltage threshold using TH0–TH4. See Table 2. IN6 cannot supply power to the device. For improved noise immunity, bypass IN6 to GND with a 0.1µF capacitor installed as close to the device as possible.				
16	IN5	Input Voltage Detector 5. Select the undervoltage threshold using TH0–TH4. See Table 2. IN5 cannot supply power to the device. For improved noise immunity, bypass IN5 to GND with a 0.1µF capacitor installed as close to the device as possible.				
17	IN4	Input Voltage Detector 4. Select the undervoltage threshold using TH0–TH4. See Table 2. For improved noise immunity, bypass IN4 to GND with a 0.1µF capacitor installed as close to the device as possible. Power the device through IN1–IN4 or V <sub>CC</sub> (see the <i>Powering the MAX6886</i> section).				
18	IN3	Input Voltage Detector 3. Select the undervoltage threshold using TH0–TH4. See Table 2. For improved noise immunity, bypass IN3 to GND with a 0.1µF capacitor installed as close to the device as possible. Power the device through IN1–IN4 or V <sub>CC</sub> (see the <i>Powering the MAX6886</i> section).				
19	IN2	Input Voltage Detector 2. Select the undervoltage threshold using TH0–TH4. See Table 2. For improved noise immunity, bypass IN2 to GND with a 0.1µF capacitor installed as close to the device as possible. Power the device through IN1–IN4 or V <sub>CC</sub> (see the <i>Powering the MAX6886</i> section).				
20	IN1	Input Voltage Detector 1. Select the undervoltage threshold using TH0–TH4. See Table 2. For improved noise immunity, bypass IN1 to GND with a 0.1µF capacitor installed as close to the device as possible. Power the device through IN1–IN4 or V <sub>CC</sub> (see the <i>Powering the MAX6886</i> section).				
_	EP	Exposed Paddle. Internally connected to GND. Connect EP to GND or leave unconnected.				

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## **Functional Diagram**



#### **Detailed Description**

The MAX6886 pin-selectable, multivoltage supply supervisor monitors six voltage-detector inputs and one watchdog input. RESET asserts when any of the configured input thresholds have been reached, MR is asserted, or the watchdog timer expires. MARGIN allows a system to be tested without RESET being asserted.

Logic inputs TH0-TH4 select 1 of 32 threshold sets for inputs IN1-IN6 (see Table 2, Threshold Options). Inputs in Table 2 that contain ADJ for inputs allow external resistor voltage-dividers to be connected to create additional thresholds.

RESET is an open-drain acitve-low output and asserts when MR is low, the watchdog timer expires, or any voltage at IN1-IN6 falls below its respective threshold. The default RESET time delay is 200ms and custom timeout periods are set by connecting an external capacitor from SRT to GND. The default watchdog normal and initial timeout periods are 1.6s and 102.4s, respectively. The normal and initial watchdog timeout periods can be adjusted by connecting an external capacitor from SWT to GND.

#### **Powering the MAX6886**

The MAX6886 derives power from the voltage-detector inputs IN1–IN4 or through an externally supplied V<sub>CC</sub>. A virtual diode-ORing scheme selects the positive input that supplies power to the device (see the *Functional Diagram*). The highest input voltage on IN1–IN4 supplies power to the device. One of IN1–IN4 must be at least 2.7V to ensure proper operation.

Internal hysteresis ensures that the supply input that initially powered the device continues to power the device when multiple input voltages are within 50mV of each other.

VCC powers the analog circuitry and is the bypass connection for the MAX6886 internal supply. Bypass VCC to GND with a 1µF ceramic capacitor installed as close to the device as possible. The internal supply voltage, measured at VCC, equals the maximum of IN1-IN4. If VCC is externally supplied, VCC must be at least 200mV higher than any voltage applied to IN1-IN4 and VCC must be brought up first. VCC always powers the device when all IN\_ are factory set as "ADJ." Do not use the internally generated VCC to provide power to external circuitry.

The MAX6886 generates a digital supply voltage at DBP for the internal logic circuitry and RESET. Bypass DBP to GND with a 1µF ceramic capacitor installed as close to the device as possible. The nominal DBP output voltage is 2.55V. Do not use DBP to provide power to external circuitry.

#### **Inputs**

The MAX6886 contains multiple logic and voltagedetector inputs. Each voltage-detector input is monitored for undervoltage thresholds.

#### Voltage-Detector Inputs (IN )

The MAX6886 offers several monitor options with both pin-selectable and adjustable reset thresholds. The threshold voltage at each adjustable IN\_ input is typically 0.6V. To monitor a voltage >0.6V, connect a resistor-divider network to the circuit as shown in Figure 1.

$$V_{IN\_TH} = V_{TH} (R_1 + R_2) / R_2$$
 (Equation 1)

where  $V_{IN\_TH}$  is the desired reset threshold voltage for the respective IN\_ and  $V_{TH}$  is the input threshold (0.6V).

Resistors  $R_1$  and  $R_2$  can have very high values to minimize current consumption due to low-leakage currents. Set  $R_2$  to some conveniently high value (10k $\Omega$ , for example) and calculate  $R_1$  based on the desired reset threshold voltage, using the following formula:

$$R_1 = R_2 \times (V_{IN} TH/V_{TH} - 1)$$

#### Threshold Logic Inputs (TH0-TH4)

The TH0-TH4 logic inputs select the undervoltage thresholds and tolerance of the IN1-IN6 voltage-detector inputs. TH0-TH4 define 32 unique options for the supervisor functionality. Connect the respective TH\_ to GND for a logic 0 or to DBP for a logic 1. Tables 1 and 2 show the 32 unique threshold options available. TH4 sets the threshold tolerance of the undervoltage threshold. A logic 1 selects a 5% supply tolerance and a logic 0 selects a 10% supply tolerance. The MAX6886 logic determines which thresholds should be used for

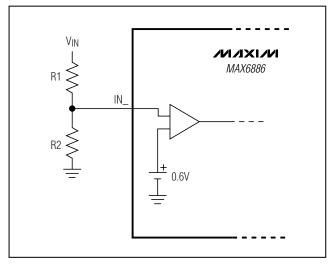


Figure 1. Adjusting the Monitored Threshold

the IN inputs only at power-up. Use the voltage-divider circuit of Figure 1 and Equation 1 to set the threshold for the user-adjustable inputs as described in the *Voltage-Detector Inputs (IN\_)* section.

#### Manual Reset (MR)

Many microprocessor-based (µP) products require manual reset capability to allow an operator or external logic circuitry to initiate a reset. The manual reset input

 $(\overline{MR})$  can be connected directly to a switch without an external pullup resistor or debouncing network.  $\overline{MR}$  is internally pulled up to DBP. Leave unconnected if not used.  $\overline{MR}$  is internally pulled up to DBP through a 10µA current source.  $\overline{MR}$  is designed to reject fast, falling transients (typically 100ns pulses) and must be held low for a minimum of 1µs to assert  $\overline{RESET}$ . After  $\overline{MR}$  transitions from low to high,  $\overline{RESET}$  remains asserted for the duration of its timeout period.

**Table 1. Nominal Monitored Supply Voltages** 

CEL ECTION	T114 T110*		NOI	MINAL SUPP	LY VOLTAGE	S (V)		SUPPLY
SELECTION	TH4-TH0*	IN1	IN2	IN3	IN4	IN5	IN6	TOLERANCE (%)
1	11111	5.0	3.3	2.5	1.8	ADJ	ADJ	5
2	11110	5.0	3.0	2.5	1.8	ADJ	ADJ	5
3	11101	5.0	3.3	2.5	ADJ	ADJ	ADJ	5
4	11100	5.0	3.0	2.5	ADJ	ADJ	ADJ	5
5	11011	5.0	3.3	1.8	ADJ	ADJ	ADJ	5
6	11010	5.0	3.0	1.8	ADJ	ADJ	ADJ	5
7	11001	5.0	3.3	ADJ	ADJ	ADJ	ADJ	5
8	11000	5.0	3.0	ADJ	ADJ	ADJ	ADJ	5
9	10111	3.3	2.5	1.8	ADJ	ADJ	ADJ	5
10	10110	3.0	2.5	1.8	ADJ	ADJ	ADJ	5
11	10101	3.3	2.5	ADJ	ADJ	ADJ	ADJ	5
12	10100	3.0	2.5	ADJ	ADJ	ADJ	ADJ	5
13	10011	3.3	1.8	ADJ	ADJ	ADJ	ADJ	5
14	10010	3.0	1.8	ADJ	ADJ	ADJ	ADJ	5
15	10001	3.3	2.5	1.8	1.5	ADJ	ADJ	5
16	10000	3.0	2.5	1.8	1.5	ADJ	ADJ	5
17	01111	5.0	3.3	2.5	1.8	ADJ	ADJ	10
18	01110	5.0	3.0	2.5	1.8	ADJ	ADJ	10
19	01101	5.0	3.3	2.5	ADJ	ADJ	ADJ	10
20	01100	5.0	3.0	2.5	ADJ	ADJ	ADJ	10
21	01011	5.0	3.3	1.8	ADJ	ADJ	ADJ	10
22	01010	5.0	3.0	1.8	ADJ	ADJ	ADJ	10
23	01001	5.0	3.3	ADJ	ADJ	ADJ	ADJ	10
24	01000	5.0	3.0	ADJ	ADJ	ADJ	ADJ	10
25	00111	3.3	2.5	1.8	ADJ	ADJ	ADJ	10
26	00110	3.0	2.5	1.8	ADJ	ADJ	ADJ	10
27	00101	3.3	2.5	ADJ	ADJ	ADJ	ADJ	10
28	00100	3.0	2.5	ADJ	ADJ	ADJ	ADJ	10
29	00011	3.3	1.8	ADJ	ADJ	ADJ	ADJ	10
30	00010	3.0	1.8	ADJ	ADJ	ADJ	ADJ	10
31	00001	3.3	2.5	1.8	1.5	ADJ	ADJ	10
32	00000	ADJ	ADJ	ADJ	ADJ	ADJ	ADJ	_

**Table 2. Threshold Options** 

OF LEGISON	THA THOS	THRESHOLD VOLTAGES (V)						
SELECTION	TH4-TH0*	IN1	IN2	IN3	IN4	IN5	IN6	
1	11111	4.62	3.06	2.31	1.67	0.60	0.60	
2	11110	4.62	2.78	2.31	1.67	0.60	0.60	
3	11101	4.62	3.06	2.31	0.60	0.60	0.60	
4	11100	4.62	2.78	2.31	0.60	0.60	0.60	
5	11011	4.62	3.06	1.67	0.60	0.60	0.60	
6	11010	4.62	2.78	1.67	0.60	0.60	0.60	
7	11001	4.62	3.06	0.60	0.60	0.60	0.60	
8	11000	4.62	2.78	0.60	0.60	0.60	0.60	
9	10111	3.06	2.31	1.67	0.60	0.60	0.60	
10	10110	2.78	2.31	1.67	0.60	0.60	0.60	
11	10101	3.06	2.31	0.60	0.60	0.60	0.60	
12	10100	2.78	2.31	0.60	0.60	0.60	0.60	
13	10011	3.06	1.67	0.60	0.60	0.60	0.60	
14	10010	2.78	1.67	0.60	0.60	0.60	0.60	
15	10001	3.06	2.31	1.67	1.39	0.60	0.60	
16	10000	2.78	2.31	1.67	1.39	0.60	0.60	
17	01111	4.38	2.88	2.19	1.58	0.60	0.60	
18	01110	4.38	2.62	2.19	1.58	0.60	0.60	
19	01101	4.38	2.88	2.19	0.60	0.60	0.60	
20	01100	4.38	2.62	2.19	0.60	0.60	0.60	
21	01011	4.38	2.88	1.58	0.60	0.60	0.60	
22	01010	4.38	2.62	1.58	0.60	0.60	0.60	
23	01001	4.38	2.88	0.60	0.60	0.60	0.60	
24	01000	4.38	2.62	0.60	0.60	0.60	0.60	
25	00111	2.88	2.19	1.58	0.60	0.60	0.60	
26	00110	2.62	2.19	1.58	0.60	0.60	0.60	
27	00101	2.88	2.19	0.60	0.60	0.60	0.60	
28	00100	2.62	2.19	0.60	0.60	0.60	0.60	
29	00011	2.88	1.58	0.60	0.60	0.60	0.60	
30	00010	2.62	1.58	0.60	0.60	0.60	0.60	
31	00001	2.88	2.19	1.58	1.31	0.60	0.60	
32	00000	0.60	0.60	0.60	0.60	0.60	0.60	

<sup>\*</sup>TH4 = '1' selects 7.5% threshold tolerance, TH4 = '0' selects 12.5% threshold tolerance.

Contact factory for alternative thresholds.

10 /V/XI/M

#### Margin Output Disable (MARGIN)

MARGIN allows system-level testing while power supplies exceed the normal operating ranges. Drive MARGIN low to hold RESET in its existing state while system-level testing occurs. Leave MARGIN unconnected or connect to DBP if unused. An internal 10µA current source pulls MARGIN to DBP. MARGIN overrides MR if both are asserted at the same time.

#### **Watchdog Timer**

The MAX6886's watchdog circuit monitors the  $\mu P$ 's activity. If the  $\mu P$  does not toggle the watchdog input (WDI) within the watchdog timeout period, RESET asserts. The internal watchdog timer is cleared by a reset, or by a transition at WDI (which can detect pulses as short as 50ns.) The watchdog timer remains cleared while RESET is asserted. The timer starts counting as soon as RESET goes high (see Figure 2).

The MAX6886 features two modes of watchdog timer operation: normal and initial modes. At power-up, after a reset event, or after the watchdog timer expires, the initial watchdog timeout is active (twd). After the first transition on WDI, the normal watchdog timeout is active (twd). The initial and normal watchdog timeouts are determined by the value of the capacitor connected between SWT and ground. The initial watchdog timeout is approximately 64 times the normal watchdog timeout.

Connect a capacitor from SWT to GND to determine the normal watchdog timeout period according to the following equation:

$$C_{SWT} = \frac{t_{WD}}{4.348 \times 10^6}$$

where  $t_{WD}$  is in seconds and  $C_{SWT}$  is in Farads. As an example, a  $1\mu F$  capacitor gives a normal timeout period of 4.68s and an initial watchdog timeout period of approximately 4.5 minutes. Connect SWT to  $V_{CC}$  to use the factory-default watchdog normal and initial timeouts of 1.6s and 102.4s, respectively. Choose a low-leakage capacitor for  $C_{SWT}$ . Disable the watchdog timer by connecting SWT to GND. WDI is internally pulled down to GND through a  $10\mu A$  current sink.

#### **RESET** Output

The reset output is typically connected to the reset input of a  $\mu P$ . A  $\mu P$ 's reset input starts or restarts the  $\mu P$  in a known state. RESET goes low whenever one or more input voltage (IN1-IN6) monitors drop below their respective thresholds, when  $\overline{MR}$  is pulled low for a minimum of  $1\mu s$ , or when the watchdog timer expires. RESET remains low for its reset timeout period (tRP) after all assertion-causing conditions have been cleared (see Figure 2).

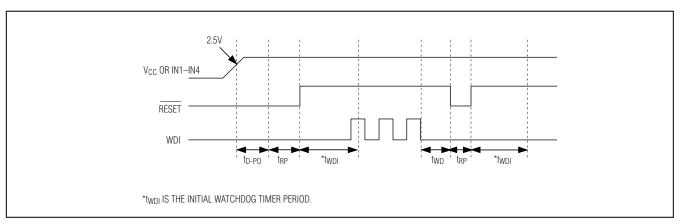


Figure 2. Watchdog, Reset, and Power-Up Timing Diagram

Set the RESET time delay by connecting a capacitor from SRT to GND using the following equation:

$$C_{SRT} = \frac{t_{WD}}{4.348 \times 10^6}$$

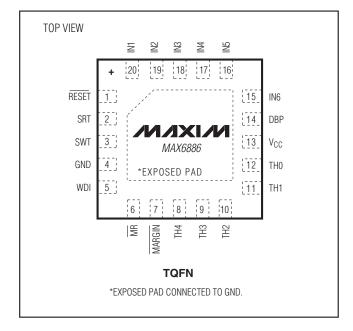
where t<sub>RP</sub> is in seconds and C<sub>SRT</sub> is in Farads. Connect SRT to V<sub>CC</sub> for a factory-default reset timeout of 200ms. RESET is open-drain and requires an external pullup resistor. RESET remains low for  $1V \le V_{CC} \le 2.5V$ .

### \_Applications Information

#### **Layout and Bypassing**

For better noise immunity, bypass each of the voltage-detector inputs to GND with  $0.1\mu F$  capacitors installed as close to the device as possible. Bypass V<sub>CC</sub> and DBP to GND with  $1\mu F$  capacitors installed as close to the device as possible.

## Pin Configuration



**Chip Information** 

PROCESS: BiCMOS

## **Package Information**

For the latest package outline information and land patterns (footprints), go to **www.maxim-ic.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE	PACKAGE	OUTLINE	LAND
TYPE	CODE	NO.	PATTERN NO.
20 TQFN-EP	T2055+5	<u>21-0140</u>	

### **Revision History**

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	2/05	Initial release	_
1	1/12	Updated Table 2.	10

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многоканальный

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