



## N-Channel 8 V (D-S) MOSFET

| PRODUCT SUMMARY     |                                      |                                    |                       |  |  |  |  |
|---------------------|--------------------------------------|------------------------------------|-----------------------|--|--|--|--|
| V <sub>DS</sub> (V) | $R_{DS(on)}\left(\Omega\right)$ Max. | I <sub>D</sub> (A) <sup>a, e</sup> | Q <sub>g</sub> (Typ.) |  |  |  |  |
| 8                   | 0.043 at V <sub>GS</sub> = 4.5 V     | 5.4                                |                       |  |  |  |  |
|                     | 0.046 at V <sub>GS</sub> = 2.5 V     | 5.2                                | 6.8 nC                |  |  |  |  |
|                     | 0.060 at V <sub>GS</sub> = 1.5 V     | 4.6                                | 0.6110                |  |  |  |  |
|                     | 0.090 at V <sub>GS</sub> = 1.2 V     | 3.0                                |                       |  |  |  |  |

### **FEATURES**

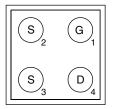
- TrenchFET® Power MOSFET
- Typical ESD protection 3000 V HBM
- Ultra-Small 1 mm x 1 mm maximum Outline
- Ultra-Thin 0.548 mm maximum height
- Material categorization: For definitions of compliance please see www.vishay.com/doc?99912



HALOGEN FREE

### **MICRO FOOT**

Bump Side View





**Device Marking: 8466** 

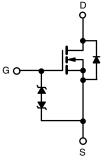
xxx = Date/Lot Traceability Code

### Ordering Information:

Si8466EDB-T2-E1 (Lead (Pb)-free and Halogen-free)

### **APPLICATIONS**

- Low On-Resistance Load Switch for Portable Devices
  - Low Power Consumption, Low Voltage Drop
  - Increased Battery Life
  - Space Savings on PCB



N-Channel MOSFET

| ABSOLUTE MAXIMUM RATINGS                           | $(T_A = 25  ^{\circ}C,  unlet)$   | ess otherwise n | oted)             |    |  |
|--|-----------------------------------|-----------------|-------------------|----|--|
| Parameter  | Symbol                            | Limit           | Unit              |    |  |
| Drain-Source Voltage                               | $V_{DS}$                          | 8               | V                 |    |  |
| Gate-Source Voltage                                |                                   | $V_{GS}$        | ± 5               | ľ  |  |
|  | T <sub>A</sub> = 25 °C            |                 | 5.4 <sup>a</sup>  |    |  |
| Continuous Drain Current (T <sub>J</sub> = 150 °C) | T <sub>A</sub> = 70 °C            | L               | 4.4 <sup>a</sup>  |    |  |
| Continuous Diam Current (1) = 130 °C)              | T <sub>A</sub> = 25 °C            | I <sub>D</sub>  | 3.6 <sup>b</sup>  |    |  |
|  | T <sub>A</sub> = 70 °C            |                 | 2.9 <sup>b</sup>  | Α  |  |
| Pulsed Drain Current (t = 300 μs)                  |                                   | I <sub>DM</sub> | 20                |    |  |
| Continuous Source-Drain Diode Current              | T <sub>C</sub> = 25 °C            |                 | 1.5 <sup>a</sup>  |    |  |
| Continuous Source-Diam Diode Current               | T <sub>A</sub> = 25 °C            | ls -            | 0.65 <sup>b</sup> |    |  |
|  | T <sub>A</sub> = 25 °C            |                 | 1.8 <sup>a</sup>  | W  |  |
| Maximum Power Dissipation                          | T <sub>A</sub> = 70 °C            | P <sub>D</sub>  | 1.1 <sup>a</sup>  |    |  |
| Maximum Fower Dissipation                          | T <sub>A</sub> = 25 °C            | r <sub>D</sub>  | 0.78 <sup>b</sup> | VV |  |
|  | T <sub>A</sub> = 70 °C            |                 | 0.5 <sup>b</sup>  |    |  |
| Operating Junction and Storage Temperature Range   | T <sub>J</sub> , T <sub>stg</sub> | - 55 to 150     |                   |    |  |
| Package Reflow Conditions <sup>c</sup>             | VPR                               |                 | 260               | °C |  |
| i acrage Hellow Conditions                         | IR/Convection                     |                 | 260               |    |  |

- a. Surface mounted on 1" x 1" FR4 board with full copper, t = 10 s.
- b. Surface mounted on 1" x 1" FR4 board with minimum copper, t = 10 s.
- c. Refer to IPC/JEDEC (J-STD-020), no manual or hand soldering.
- d. In this document, any reference to case represents the body of the MICRO FOOT device and foot is the bump.
- e. Based on  $T_A = 25$  °C.

## **Si8466EDB**

# Vishay Siliconix



| THERMAL RESISTANCE RATINGS                  |          |                   |         |      |      |  |  |
|---|----------|-------------------|---------|------|------|--|--|
| Parameter                                   | Symbol   | Typical           | Maximum | Unit |      |  |  |
| Maximum Junction-to-Ambient <sup>a, b</sup> | t = 10 s | R <sub>thJA</sub> | 55      | 70   | °C/W |  |  |
| Maximum Junction-to-Ambient <sup>c, d</sup> | t = 10 s | ' 'thJA           | 125     | 160  | C/VV |  |  |

### Notes:

- a. Surface mounted on 1" x 1" FR4 board with full copper.
- b. Maximum under steady state conditions is 100  $^{\circ}\text{C/W}$ .
- c. Surface mounted on  $1^{\circ}$  x  $1^{\circ}$  FR4 board with minimum copper.
- d. Maximum under steady state conditions is 190 °C/W.

| Parameter                                     | Symbol Test Conditions  |  | Min. | Тур.  | Max.  | Unit  |  |
|---|-------------------------|--|------|-------|-------|-------|--|
| Static  |                         |  | L    |       |       |       |  |
| Drain-Source Breakdown Voltage                | V <sub>DS</sub>         | $V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}$                        | 8    |       |       | V     |  |
| V <sub>DS</sub> Temperature Coefficient       | $\Delta V_{DS}/T_{J}$   | I <sub>D</sub> = 250 μA  |      | 3.5   |       | mV/°C |  |
| V <sub>GS(th)</sub> Temperature Coefficient   | $\Delta V_{GS(th)}/T_J$ | 1 <sub>D</sub> = 230 μΑ  |      | - 3   |       |       |  |
| Gate-Source Threshold Voltage                 | V <sub>GS(th)</sub>     | $V_{DS} = V_{GS}, I_D = 250 \mu A$                                   | 0.35 |       | 0.7   | V     |  |
| Gate-Source Leakage                           | I <sub>GSS</sub>        | $V_{DS} = 0 \text{ V}, V_{GS} = \pm 5 \text{ V}$                     |      |       | ± 3   | μΑ    |  |
| Zava Cata Valtaga Drain Current               | 1                       | V <sub>DS</sub> = 8 V, V <sub>GS</sub> = 0 V                         |      |       | 1     | μА    |  |
| Zero Gate Voltage Drain Current               | I <sub>DSS</sub>        | V <sub>DS</sub> = 8 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 70 °C |      |       | 10    |       |  |
| On-State Drain Current <sup>a</sup>           | I <sub>D(on)</sub>      | $V_{DS} \ge 5 \text{ V}, V_{GS} = 4.5 \text{ V}$                     | 10   |       |       | Α     |  |
|   |                         | $V_{GS} = 4.5 \text{ V}, I_D = 2 \text{ A}$                          |      | 0.035 | 0.043 |       |  |
|   | R <sub>DS(on)</sub>     | $V_{GS} = 2.5 \text{ V}, I_D = 1 \text{ A}$                          |      | 0.037 | 0.046 | Ω     |  |
| Drain-Source On-State Resistance <sup>a</sup> |                         | V <sub>GS</sub> = 1.5 V, I <sub>D</sub> = 1 A                        |      | 0.045 | 0.060 |       |  |
|   |                         | $V_{GS} = 1.2 \text{ V}, I_D = 0.5 \text{ A}$                        |      | 0.055 | 0.090 |       |  |
| Forward Transconductance <sup>a</sup>         | 9 <sub>fs</sub>         | V <sub>DS</sub> = 4 V, I <sub>D</sub> = 2 A                          |      | 30    |       | S     |  |
| Dynamic <sup>b</sup>                          |                         |  |      |       |       |       |  |
| Input Capacitance                             | C <sub>iss</sub>        |  |      | 710   |       | pF    |  |
| Output Capacitance                            | C <sub>oss</sub>        | $V_{DS} = 4 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHz}$      |      | 270   |       |       |  |
| Reverse Transfer Capacitance                  | C <sub>rss</sub>        |  |      | 192   |       |       |  |
| Total Gate Charge                             | Qg                      |  |      | 8.5   | 13    |       |  |
| Gate-Source Charge                            | Q <sub>gs</sub>         | $V_{DS} = 4 \text{ V}, V_{GS} = 4.5 \text{ V}, I_D = 2 \text{ A}$    |      | 0.9   |       | nC    |  |
| Gate-Drain Charge                             | Q <sub>gd</sub>         |  |      | 1.6   |       | 1     |  |
| Gate Resistance                               | R <sub>g</sub>          | V <sub>GS</sub> = 0.1 V, f = 1 MHz                                   |      | 6     |       | Ω     |  |
| Turn-On Delay Time                            | t <sub>d(on)</sub>      |  |      | 10    | 20    |       |  |
| Rise Time                                     | t <sub>r</sub>          | $V_{DD}$ = 4 V, $R_L$ = 2 $\Omega$                                   |      | 15    | 30    | ns    |  |
| Turn-Off Delay Time                           | t <sub>d(off)</sub>     | $I_D\cong$ 2 A, $V_{GEN}$ = 4.5 V, $R_g$ = 1 $\Omega$                |      | 40    | 80    |       |  |
| Fall Time                                     | t <sub>f</sub>          |  |      | 10    | 20    |       |  |



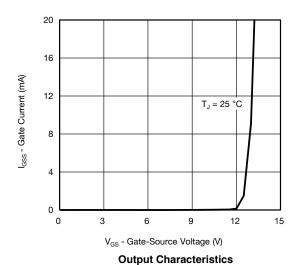
| SPECIFICATIONS (T <sub>J</sub> = 25 °C, unless otherwise noted) |                 |   |      |      |      |      |  |
|---|-----------------|---|------|------|------|------|--|
| Parameter   | Symbol          | Test Conditions   | Min. | Тур. | Max. | Unit |  |
| Drain-Source Body Diode Characteristics                         |                 |   |      |      |      |      |  |
| Continuous Source-Drain Diode Current                           | I <sub>S</sub>  | T <sub>A</sub> = 25 °C  |      |      | 1.5  | Α    |  |
| Pulse Diode Forward Current                                     | I <sub>SM</sub> |   |      |      | 20   | A    |  |
| Body Diode Voltage  | $V_{SD}$        | $I_S = 1.5 \text{ A}, V_{GS} = 0$                               |      | 0.7  | 1.2  | V    |  |
| Body Diode Reverse Recovery Time                                | t <sub>rr</sub> |   |      | 30   | 60   | ns   |  |
| Body Diode Reverse Recovery Charge                              | Q <sub>rr</sub> | I <sub>F</sub> = 2 A, dl/dt = 100 A/μs, T <sub>.l</sub> = 25 °C |      | 7    | 15   | nC   |  |
| Reverse Recovery Fall Time                                      | ta              | 1 1 - 2 Λ, αι/αι - 100 Λ/μο, 1 1 - 20 0                         |      | 15   |      | ns   |  |
| Reverse Recovery Rise Time                                      | t <sub>b</sub>  |   |      | 15   |      | 115  |  |

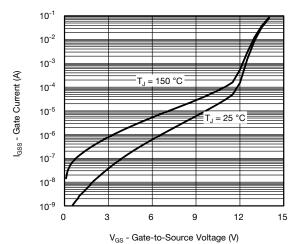
### Notes:

- a. Pulse test; pulse width  $\leq$  300  $\mu$ s, duty cycle  $\leq$  2 %.
- b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

### TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

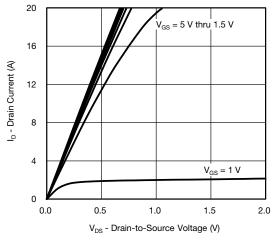




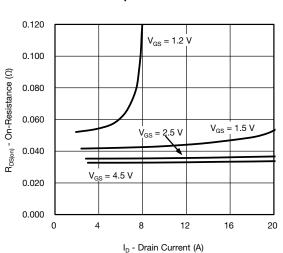
On-Resistance vs. Drain Current and Gate Voltage

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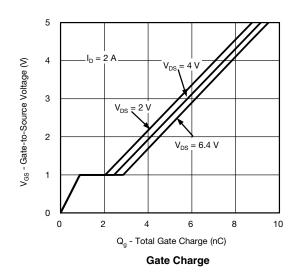
### TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

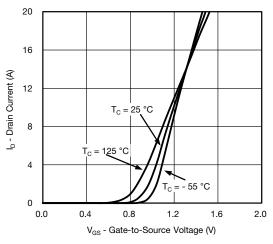


### **Output Characteristics**

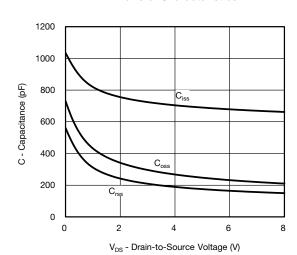


On-Resistance vs. Drain Current and Gate Voltage

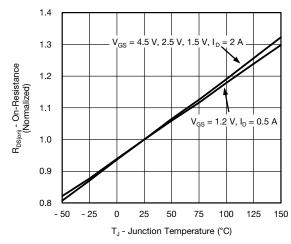




**Transfer Characteristics** 



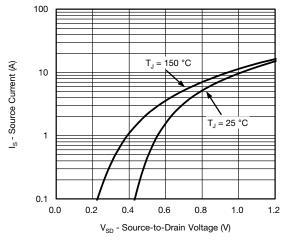
Capacitance



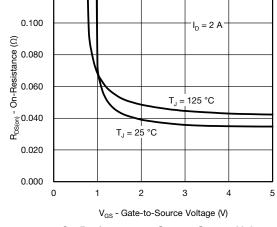
On-Resistance vs. Junction Temperature



### TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

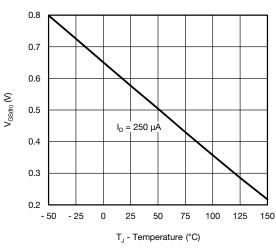


### Source-Drain Diode Forward Voltage

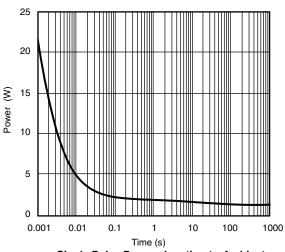


0.120

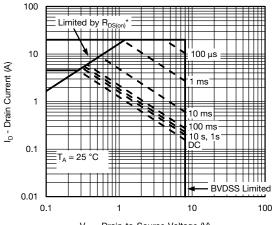
On-Resistance vs. Gate-to-Source Voltage



**Threshold Voltage** 



Single Pulse Power, Junction-to-Ambient

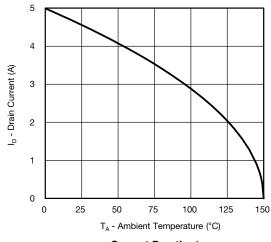


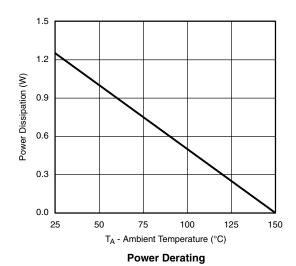
 $\rm V_{DS}$  - Drain-to-Source Voltage (V)  $^*$   $\rm V_{GS}$  > minimum  $\rm V_{GS}$  at which  $\rm R_{DS(on)}$  is specified

Safe Operating Area, Junction-to-Ambient

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### TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)





**Current Derating\*** 

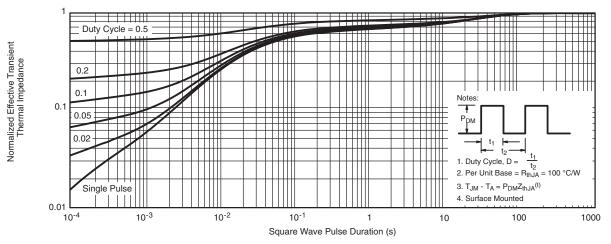
Note:

When Mounted on 1" x 1" FR4 with Full Copper.

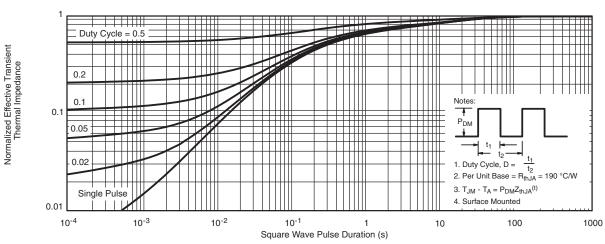
 $<sup>^*</sup>$  The power dissipation  $P_D$  is based on  $T_{J(max.)}$  = 150  $^{\circ}$ C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.



### TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Ambient (1" x 1" FR4 Board with Full Copper)

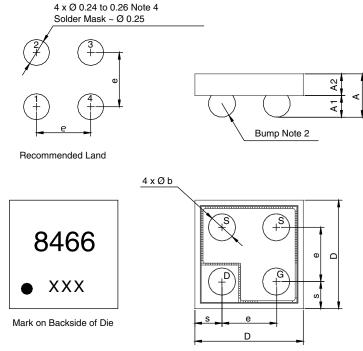


Normalized Thermal Transient Impedance, Junction-to-Ambient (1" x 1" FR4 Board with Minimum Copper)

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### **PACKAGE OUTLINE**

### MICRO FOOT 1 mm x 1 mm: 4-BUMP (2 x 2, 0.5 mm PITCH)



Notes (Unless otherwise specified):

- 1. All dimensions are in millimeters.
- 2. Four (4) solder bumps are lead (Pb)-free 95.5Sn/3.8Ag/0.7Cu with diameter Ø 0.30 mm to 0.32 mm.
- 3. Backside surface is coated with a Ti/Ni/Ag layer.
- 4. Non-solder mask defined copper landing pad.
- 5. is location of pin 1.

| Dim.           |       | Millimeters <sup>a</sup> |       | Inches |        |        |  |
|----------------|-------|--------------------------|-------|--------|--------|--------|--|
|                | Min.  | Nom.                     | Max.  | Min.   | Nom.   | Max.   |  |
| Α              | 0.462 | 0.505                    | 0.548 | 0.0181 | 0.0198 | 0.0215 |  |
| A <sub>1</sub> | 0.220 | 0.250                    | 0.280 | 0.0086 | 0.0098 | 0.0110 |  |
| A <sub>2</sub> | 0.242 | 0.255                    | 0.268 | 0.0095 | 0.0100 | 0.0105 |  |
| b              | 0.300 | 0.310                    | 0.320 | 0.0118 | 0.0122 | 0.0126 |  |
| е              | 0.500 |                          |       | 0.0197 |        |        |  |
| s              | 0.230 | 0.250                    | 0.270 | 0.0090 | 0.0098 | 0.0106 |  |
| D              | 0.920 | 0.960                    | 1.000 | 0.0362 | 0.0378 | 0.0394 |  |

a. Use millimeters as the primary measurement.

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?63683.



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Revision: 02-Oct-12 Document Number: 91000

## **ПОСТАВКА** ЭЛЕКТРОННЫХ КОМПОНЕНТОВ

многоканальный

Общество с ограниченной ответственностью «МосЧип» ИНН 7719860671 / КПП 771901001 Адрес: 105318, г.Москва, ул.Щербаковская д.3, офис 1107

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