SCH5617C

Desktop System Controller Hub with Advanced, 8051µC-Based Auto Fan Control

PRODUCT FEATURES

Data Brief

- ACPI 2.0 Compliant
- High Performance 8051
  - 2.5X average instruction execution speed improvement over the entire instruction set; i.e., typical 4-clock instruction cycle in high-performance 8051 vs. 12-clock instruction cycle in standard 8051.
  - Faster clock speed: 32 MHz vs. 16 MHz in standard 8051.
  - Dual Data Pointers
  - More Interrupts: Power-Fail, External Interrupt 2, External Interrupt 3, etc.
  - A set of External Memory/Mapped Control Registers provides the 80C51 core with the ability to directly control many functional blocks of the SCH5617C.
  - 384 Bytes of RAM as part of the 8051 core
  - 4k Bytes Data RAM (869 bytes may be used to patch ROM code)
  - Twelve Interrupt Sources
  - Watch Dog Timer (WDT)
- PECI Interface
  - Supports PECI REQUEST# and PECI AVAILABLE signalling
- Temperature Monitor
  - Monitoring of up to Two Remote Thermal Diodes
  - Supports temperature readings from -63 degrees to +192 degrees
    - Supports monitoring of discrete diodes (3904 type diodes)
    - Supports monitoring substrate diodes (45nm & 65nm processor diodes)
  - 1/8th degree temperature resolution
  - Internal Ambient Temperature Measurement
  - Limit Comparison of all Monitored Values
- PROCHOT_IN# Pin
  - Mapped into Temperature monitoring interrupt generation logic
  - May be used to adjust fan control limits
  - May be configured to force fans on full
- PROCHOT_OUT Pin
- Auto-Fan Control with ProcHot Features
  - PWM (Pulse width Modulation) Outputs (3)
    - Legacy PWM control dc fan outputs
  - High Frequency PWM Options (15kHz up to 30kHz)
  - 2 second delayed start-up for PWM outputs
  - Fan Tachometer or Lock Rotor Inputs (3)
  - Programmable linear automatic fan control based on temperature
  - Acoustic enhancement mode
  - ProcHot pins modulate Tmin
  - Fan PWM duty cycle is a function in linear mode of multiple temperatures and ProcHot signals
  - PWM Ramp Rate Closed Loop Control
- Internal Ring Oscillator for VTR Powered Logic
- Low Battery Warning
- LED Control
- SMBus Isolation Logic
- Programmable Wake-up Event Interface
- PC2001 Compliant
- General Purpose Input/Output Pins (30 Host controlled, 16 8051 controlled)
- 21 Dedicated Scratchpad registers
- ISA Plug-and-Play Compatible Register Set
- System Management Interrupt
- GLUE Logic
  - IDE Reset/Buffered PCI Reset Outputs
  - Power OK Signal Generation
  - Power Sequencing
  - Power Supply Turn On Circuitry
  - Resume Reset Signal Generation
  - Hard Drive Front Panel LED
- 2.88MB Super I/O Floppy Disk Controller
  - Licensed CMOS 765B Floppy Disk Controller
  - Software and Register Compatible with SMSC's Proprietary 82077AA Compatible Core
  - Supports Two Floppy Drives
  - Configurable Open Drain/Push-Pull Output Drivers
  - Supports Vertical Recording Format
  - 16-Byte Data FIFO
  - 100% IBM® Compatibility
  - Detects All Overrun and Underrun Conditions
  - Sophisticated Power Control Circuitry (PCC) Including Multiple Powerdown Modes for Reduced Power Consumption
  - DMA Enable Logic
  - Data Rate and Drive Control Registers
  - 480 Addresses, Up to Eight IRQs, and Four DMA Options
  - Enhanced Digital Data Separator
    - 2 Mbps, 1 Mbps, 500 Kbps, 300 Kbps, 250 Kbps Data Rates
    - Programmable Pre compensation Modes

- Keyboard Controller
  - 8042 Software Compatible
  - 8 Bit Microcomputer
  - 2k Bytes of Program ROM
  - 256 Bytes of Data RAM
  - Four Open Drain Outputs Dedicated for Keyboard/Mouse Interface
  - Asynchronous Access to Two Data Registers and One Status Register
  - Supports Interrupt and Polling Access
  - 8 Bit Counter Timer
  - Port 92 Support
  - Fast Gate A20 and KRESET Outputs
- Serial Ports
  - Two Full Function Serial Ports
  - High Speed NS16C550A Compatible UARTs with Send/Receive 16-Byte FIFOs
  - Programmable Baud Rate Generator
    - Supports all standard baud rates up to 115k bps
    - Supports non-standard baud rates of 230k and 460k bps
  - Modem Control Circuitry
  - 480 Address and 15 IRQ Options
- Infrared Port
  - Multi protocol Infrared Interface
  - IrDA 1.0 Compliant
  - SHARP ASK IR
  - 480 Addresses, Up to 15 IRQ
- Multi-Mode™ Parallel Port with ChiProtect™
  - Standard Mode IBM PC/XT®, PC/AT®, and PS/2™ Compatible Bi-directional Parallel Port
  - Enhanced Parallel Port (EPP) Compatible - EPP 1.7 and EPP 1.9 (IEEE 1284 Compliant)
  - IEEE 1284 Compliant Enhanced Capabilities Port (ECP)
  - ChiProtect Circuitry for Protection
  - 960 Address, Up to 15 IRQ and Four DMA Options
- LPC Interface
  - Multiplexed Command, Address and Data Bus
  - Serial IRQ Interface Compatible with Serialized IRQ Support for PCI Systems
  - PME Interface
- Power Good Output
- 3.3 Volt I/O
- 128 Pin QFP Lead-Free RoHS Compliant Package

ORDER NUMBER:

SCH5617C-NS FOR 128 PIN, QFP LEAD-FREE ROHS COMPLIANT PACKAGE

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General Description

The SCH5617C is a 3.3V PC 2001 compliant Super I/O controller with an LPC interface. All legacy drivers used for Super I/O components are supported making this interface transparent to the supporting software. The LPC bus also supports power management, such as wake-up and sleep modes.

The SCH5617C provides temperature monitoring with auto fan control. The temperature monitor is capable of monitoring two external diodes, one internal ambient temperature sensor or retrieving temperatures from external processors that implement the PECI Interface. This includes support for the PECI REQUEST# and PECI AVAILABLE signals that are used to assure correct operation of PECI when processors enter the C3/C4 sleep states. This device offers programmable automatic fan control support based on one or more of these measured temperatures. There are three pulse width modulation (PWM) outputs with high frequency support as well as three fan tachometer inputs. In addition, there is support for a PROCHOT_IN# pin that may be used to generate an interrupt, adjust the programmed temperature limits in the auto fan control logic, or force the PWM outputs on full. There is also a separate PROCHOT_OUT output pin.

The GLUE Logic includes various power management logic including generation of RSMRST# and Power OK signal generation. There are also four LEDs to indicate power status and hard drive activity. Also included is SMBus Isolation logic, which can be used to isolate SMBus signals during power down modes.

The part provides 45 General Purpose I/O control pins, which offer flexibility to the system designer. There are 21 Scratchpad read/write runtime registers for custom use.

The SCH5617C incorporates the following Super I/O components: a parallel port that is compatible with IBM PC/AT architecture, as well as the IEEE 1284 EPP and ECP; two serial ports that are 16C550A UART compatible; a keyboard/mouse controller that uses an 8042 micro controller; two floppy controllers, which use SMSC's true CMOS 765B core; one infrared port that is IrDA 1.0 compliant. The true CMOS 765B core provides 100% compatibility with IBM PC/XT and PC/AT architectures and is software and register compatible with SMSC's proprietary 82077AA core. The part also provides a low battery warning circuit.

The SCH5617C is ACPI 1.0b/2.0 compatible supports multiple low power-down modes. It incorporates sophisticated power control circuitry (PCC), which includes keyboard and mouse wake-up events.

The SCH5617C supports the ISA Plug-and-Play Standard register set (Version 1.0a). The I/O Address, DMA Channel and hardware IRQ of each logical device in the SCH5617C may be reprogrammed through the internal configuration registers. There are up to 480 (960 for Standard Mode Parallel Port) I/O address location options, a Serialized IRQ interface, and four DMA channels.

Block Diagram

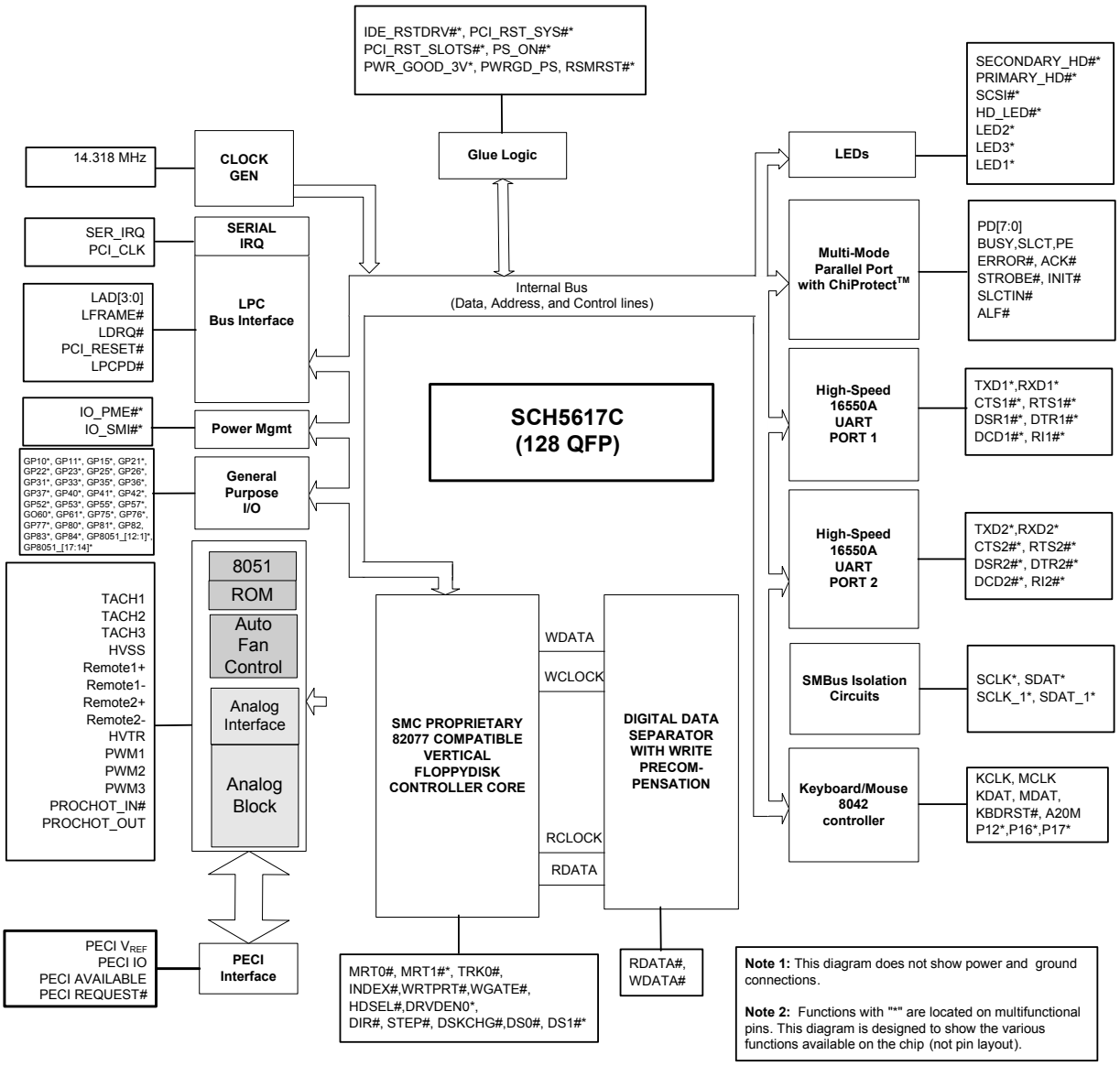

Figure 1 SCH5617C Block Diagram

Package Outline

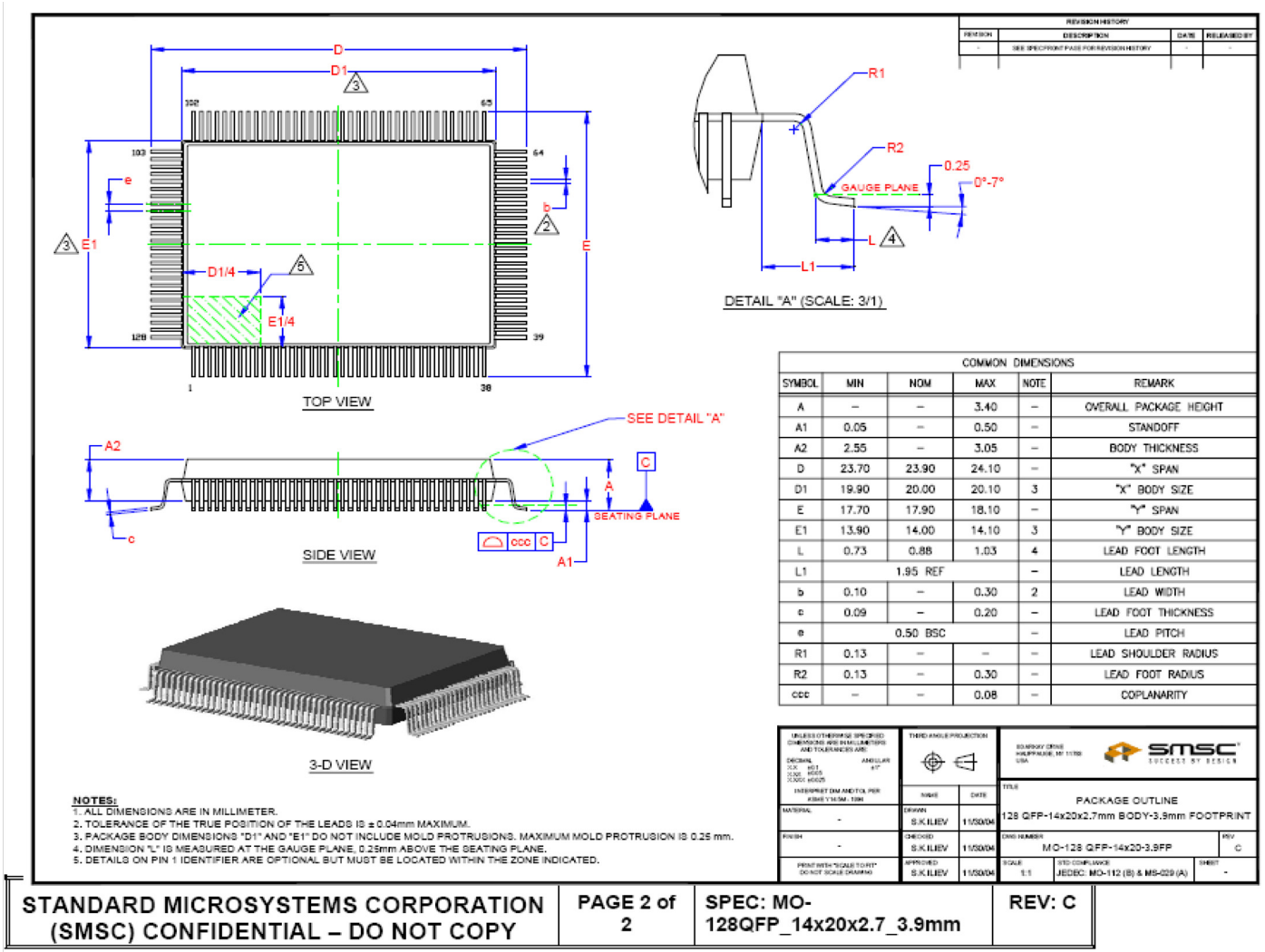

Figure 2 128-Pin QFP Package Outline (3.9mm footprint)

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