MAX35102

Time-to-Digital Converter Without RTC

General Description

The MAX35102 is a time-to-digital converter with built-in amplifier and comparator targeted as a low-cost, analog front-end solution for the ultrasonic heat meter and flow meter markets. It is similar to the MAX35101, but with a reduced feature set and without a real-time clock (RTC). The package size has been reduced to 4mm x 4mm x 0.75mm with 0.4mm pin pitch.

With a time measurement accuracy of 20ps and automatic differential time-of-flight (ToF) measurement, this device makes for simplified computation of liquid flow.

Power consumption is the lowest available with ultra-low 5.5μA ToF measurement and < 125nA duty-cycled temperature measurement.

Applications

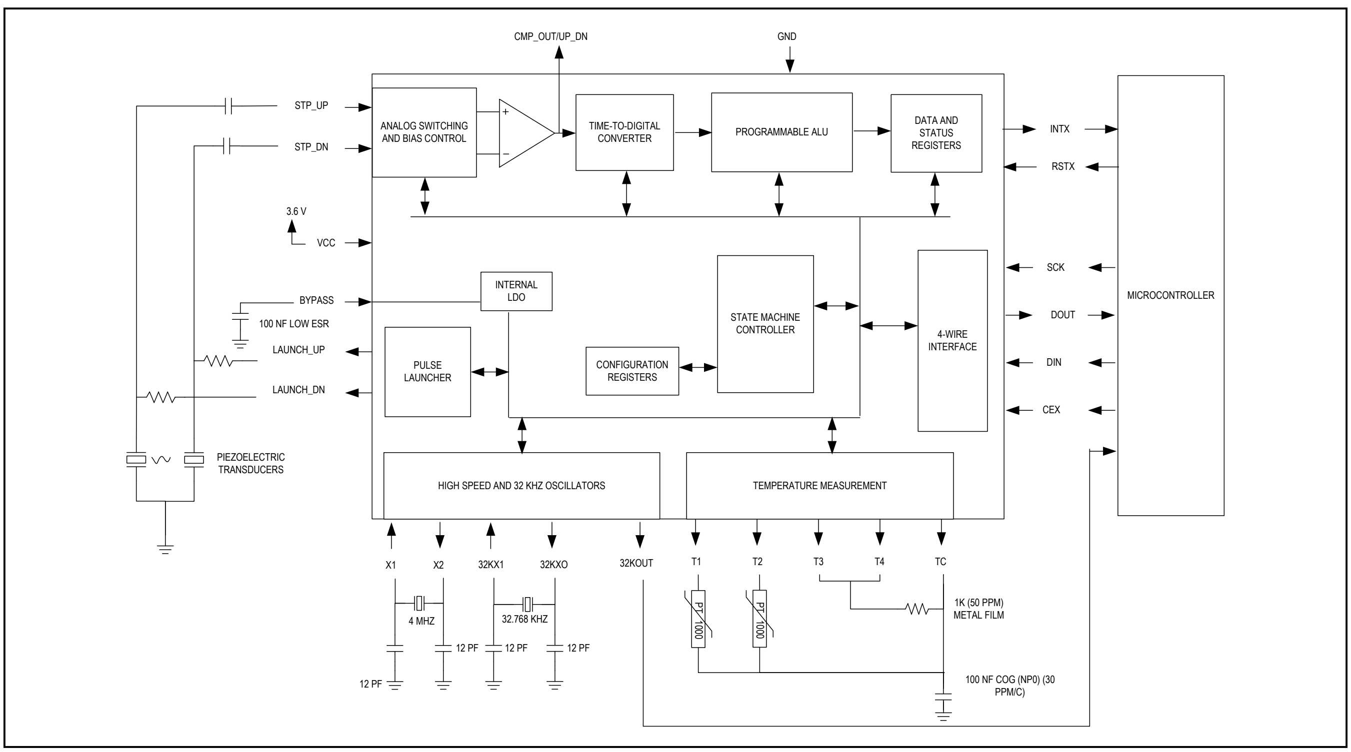
- Ultrasonic Heat Meters
- Ultrasonic Water Meters
- Ultrasonic Gas Meters

***Ordering Information* appears at end of data sheet.**

Features and Benefits

- High-Accuracy Flow Measurement for Billing and Leak Detection
  - Time-to-Digital Accuracy Down to 20ps
  - Measurement Range Up to 8ms
  - 2 Channels—Single-Stop Channel
- High-Accuracy Temperature Measurement for Precise Heat and Flow Calculations
  - Up to Four 2-Wire Sensors
  - PT1000 and PT500 RTD Support
  - 40mK Accuracy
- Maximizes Battery Life with Low Device and Overall System Power
  - Ultra-Low 5.5μA ToF measurement and < 125nA Duty-Cycled Temperature Measurement
  - 2.3V to 3.6V Single-Supply Operation
- High-Integration Solution Minimizes Parts Count and Reduces BOM Cost
  - Small, 4mm x 4mm, 32-Pin TQFN Package
  - -40°C to +85°C Operation

System Block Diagram



19-7442; Rev 0; 11/14

maxim integrated™

Absolute Maximum Ratings

(Voltages relative to ground.)
Voltage Range on V_{CC} Pins................................-0.5V to +4.0V
Voltage Range on All Other Pins
(not to exceed 4.0V)............................ -0.5V to (V_{CC} + 0.5V)
Continuous Power Dissipation (T_A = +70°C)
TQFN (derate 29.40mW/ºC above +70°C)...........2352.90mW
Operating Temperature Range.......................... -40°C to +85°C
Junction Temperature...+150°C
Storage Temperature Range........................... -55°C to +125°C
Lead Temperature (soldering, 10s) ....+300°C
Soldering Temperature (reflow).......................................+260°C
ESD Protection (All Pins, Human Body Model) ....±2kV

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Thermal Characteristics (Note 1)

TQFN
Junction-to-Ambient Thermal Resistance (θ_{JA}) ....34°C/W
Junction-to-Case Thermal Resistance (θ_{JC}).....................3°C/W

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

Recommended Operating Conditions

(T_A = -40°C to +85°C, unless otherwise noted.) (Notes 2, 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage	V_{CC}		2.3	3.0	3.6	V
Input Logic 1 ($\overline{RST}$, SCK, DIN, $\overline{CE}$)	V_{IH}		V_{CC} x 0.7		V_{CC} + 0.3	V
Input Logic 0 ($\overline{RST}$, SCK, DIN, $\overline{CE}$)	V_{IL}		-0.3		V_{CC} x 0.3	V
Input Logic 1 (32KX1)	$V_{IH32KX1}$		V_{CC} x 0.85		V_{CC} + 0.3	V
Input Logic 0 (32KX1)	$V_{IL32KX1}$		-0.3		V_{CC} x 0.15	V

Electrical Characteristics

(V_{CC} = 2.3V to 3.6V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{CC} = 3.0V and T_A = +25°C.) (Notes 2, 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Leakage ($\overline{RST}$, SCK, DIN, $\overline{CE}$)	I_L		-0.1		+0.1	µA
Output Leakage ($\overline{INT}$, T1,T2,T3,T4)	O_L		-0.1		+0.1	µA
Output Voltage Low (32KOUT)	V_{OL32K}	2mA			0.2 x V_{CC}	V
Output Voltage High (32KOUT)	V_{OH32K}	-1mA	0.8 x V_{CC}			V
Output Voltage High (DOUT, CMP_OUT/UP_DN)	V_{OH}	-4mA	0.8 x V_{CC}			V
Output Voltage High (TC)	V_{OHTC}	V_{CC} = 3.3V, I_{OUT} = -4mA	2.9	3.1		V
Output Voltage High (Launch_UP, Launch_DN)	$V_{OHLAUCH}$	V_{CC} = 3.3V, I_{OUT} = -50mA	2.8	3.0		V
Output Voltage Low ($\overline{INT}$, DOUT, CMP_OUT/UP_DN)	V_{OL}	4mA			0.2 x V_{CC}	V

Electrical Characteristics (continued)

(V_{CC} = 2.3V to 3.6V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{CC} = 3.0V and T_A = +25°C.) (Notes 2, 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Pulldown Resistance (TC)	R_{TC}		650	1000	1500	Ω
Input Voltage Low (TC)	V_{ILTC}			0.36 x V_{CC}		V
Output Voltage Low (Launch_UP, Launch_DN)	$V_{OLLAUCH}$	V_{CC} = 3.3V, I_{OUT} = 50mA		0.2	0.4	V
Resistance (T1, T2, T3, T4)	R_{ON}			1		Ω
Input Capacitance ($\overline{CE}$, SCK, DIN, $\overline{RST}$)	C_{IN}	Not tested		7		pF
$\overline{RST}$ Low Time	t_{RST}				100	ns
CURRENT						
Standby Current	I_{DDQ}	No oscillators running, T_A = +25°C		0.1	1	µA
32kHz OSC Current	I_{32KHZ}	32kHz oscillator only (Note 4)		0.5	0.9	µA
4MHz OSC Current	I_{4MHZ}	4MHz oscillator only (Note 4)		40	85	µA
LDO Bias Current	I_{CCLDO}	I_{CCCPU} = 0 (Note 4)		15	50	µA
Time Measurement Unit Current	I_{CCTMU}	(Note 4)		4.5	8	mA
Calculator Current	I_{CCCPU}			0.75	1.7	mA
Device Current Drain	I_{CC3}	TOF_DIFF = 2 per second (3 hits), temperature = 1 per 30s		5.5		µA
ANALOG RECEIVER						
Analog Input Voltage (STOP_UP, STOP_DN)	V_{ANA}		10	700	2 x V_{CC} x (3/8)	mV_{P-P}
Input Offset Step Size	V_{STEP}			1		mV
STOP_UP/STOP_DN Bias Voltage	V_{BIAS}			V_{CC} x (3/8)		V
Receiver Sensitivity	V_{ANA}	Stop hit detect level (Note 5)	10			mV_{P-P}
TIME MEASUREMENT UNIT						
Measurement Range	t_{MEAS}	Time of flight	8		8000	µs
Time Measurement Accuracy	t_{ACC}	Differential time measurement		20		ps
Time Measurement Resolution	t_{RES}			3.8		ps
EXECUTION TIMES						
Power-On-Reset Time	t_{RESET}	Reset to POR INT		275		µs
INIT Command Time	t_{INIT}	Command received when INIT bit set		2.5		ms
CAL Command Time	t_{CAL}	Command received when CAL bit set		1.25		ms

Electrical Characteristics (continued)

(V_{CC} = 2.3V to 3.6V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{CC} = 3.0V and T_A = +25°C.) (Notes 2, 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SERIAL PERIPHERAL INTERFACE						
DIN to SCK Setup	t_{DC}				20	ns
SCK to DIN Hold	t_{CDH}			2	20	ns
SCK to DOUT Delay	t_{CDD}			5	20	ns
SCK Low Time	t_{CL}	V_{CC} ≥ 3.0V	25	4		ns
		V_{CC} = 2.3V	50	30		
SCK High Time	t_{CH}		25	4		ns
SCK Frequency	t_{CLK}	V_{CC} ≥ 3.0V			20	MHz
		V_{CC} = 2.3V			10	
$\overline{CE}$ to SCK Setup	t_{CC}			5	40	ns
SCK to $\overline{CE}$ Hold	t_{CCH}				20	ns
$\overline{CE}$ Inactive Time	t_{CWH}			2	40	ns
$\overline{CE}$ to DOUT High Impedance	t_{CCZ}			5	20	ns

Recommended External Crystal Characteristics

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
32kHz Nominal Frequency	f_{32K}			32.768		kHz
32kHz Frequency Tolerance	$\Delta f_{32K}/f_{32K}$	T_A = +25°C	-20		+20	ppm
32kHz Load Capacitance	C_{L32K}			12.5		pF
32kHz Series Resistance	R_{S32K}				70	kΩ
4MHz Crystal Nominal Frequency	F_{4M}			4.000		MHz
4MHz Crystal Frequency Tolerance	$\Delta f_{4M}/f_{4M}$	T_A = +25°C	-30		+30	ppm
4MHz Crystal Load Capacitance	C_{L4M}			12.0		pF
4MHz Crystal Series Resistance	R_{S4M}				120	Ω
4MHz Ceramic Nominal Frequency				4.000		MHz
4MHz Ceramic Frequency Tolerance		T_A = +25°C	-0.5		+0.5	%
4MHz Ceramic Load Capacitance				30		pF
4MHz Ceramic Series Resistance					30	Ω

Note 2: All voltages are referenced to ground. Current entering the device are specified as positive and currents exiting the device are negative.

Note 3: Limits are 100% production tested at T_A = +25°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization.

Note 4: Currents are specified as individual block currents. Total current for a point in time can be calculated by taking the standby current and adding any block currents that are active at that time.

Note 5: Receiver sensitivity includes performance degradation contributed by STOP_UP and STOP_DN device pin input offset voltage and common mode drift.

Timing Diagrams

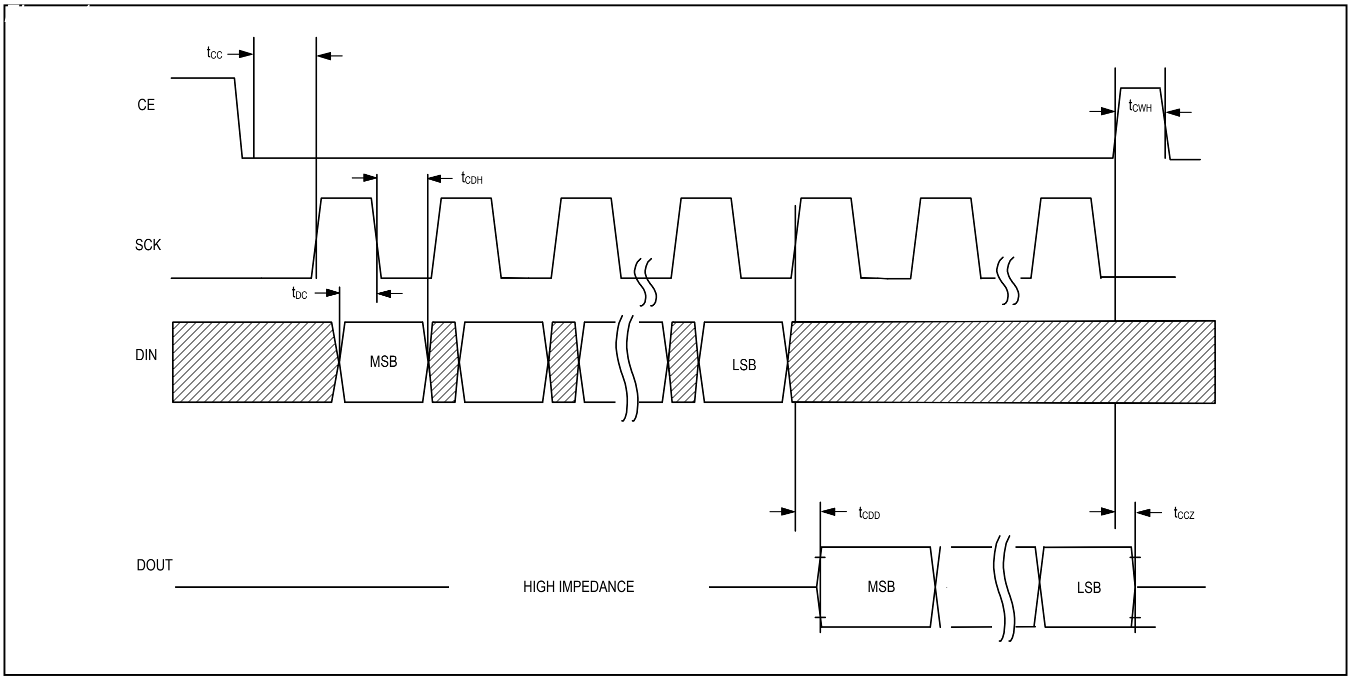


Figure 1. SPI Timing Diagram Read

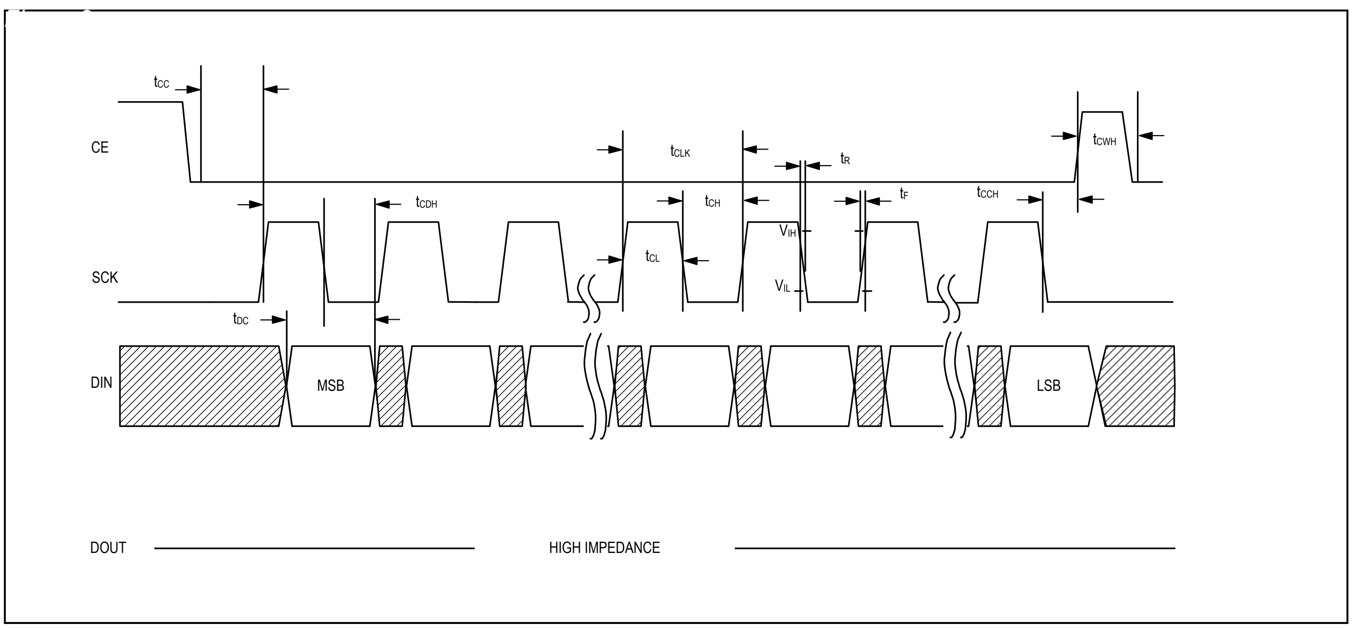
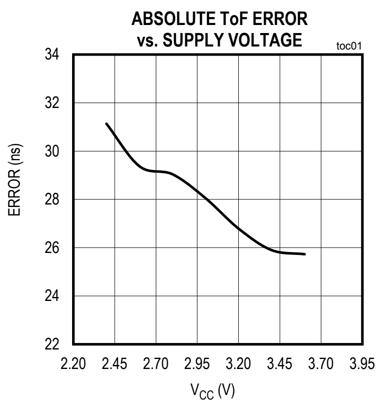
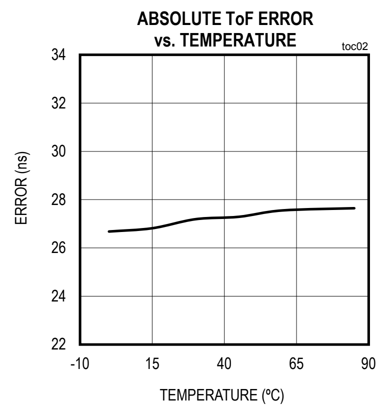


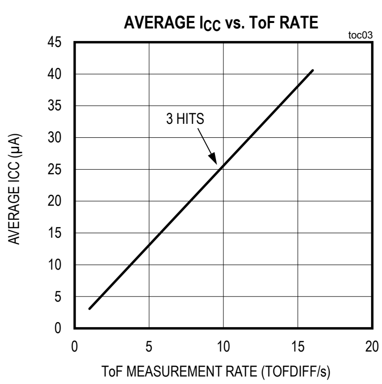
Figure 2. SPI Timing Diagram Write

Typical Operating Characteristics

(V_{CC} = 3.3V and T_A = +25°C, unless otherwise noted.)







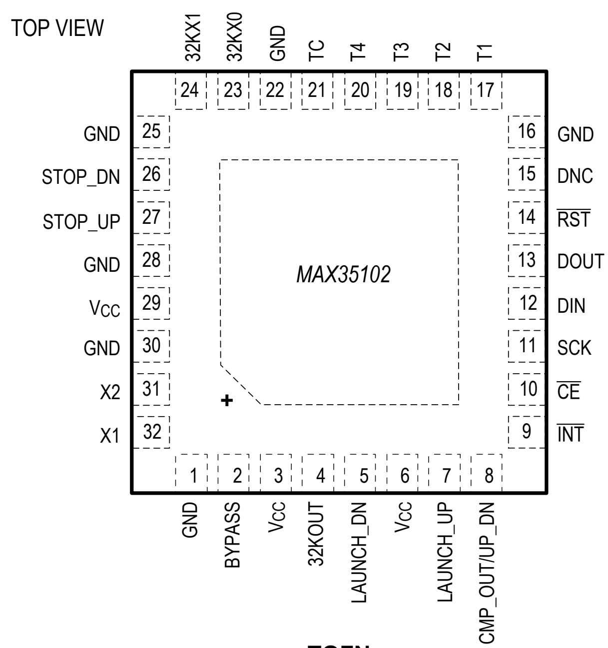
Average ICC vs. TOF Rate Configuration Settings

CONTOL BIT(S)	3 HIT SETTINGS	
	VALUE	**BIT SETTINGS**
Clock Settling Time	488µs	CLK_S[2:0] = 000
Bias Charge Time	61µs	CT[1:0] = 00
Pulse Launch Frequency	1MHz	DPL[3:0] = 0001
Pulse Launcher Size	15	PL[7:0] = 00001111
TOF Duty Cycle	19.97ms	TOF_CYC[2:0] = 111
Stop Hits	3	STOP[1:0] = 010
T2 Wave Selector	Wave 2	T2WV[5:0] = 000110
Temperature Port Number	4	TP[1:0] = 11
Preamble Temperature Cycle Number	1	PRECYC[2:0] = 001
Port Cycle Time	256µs	PORTCYC[1:0] = 01

Notes

1. This data is valid for the ceramic resonator.
2. Crystal oscillator startup adds ~0.5µA per TOFDiff.
3. Since the TOF cycle time is long the 4MHz oscillator powers up twice.

Pin Configuration



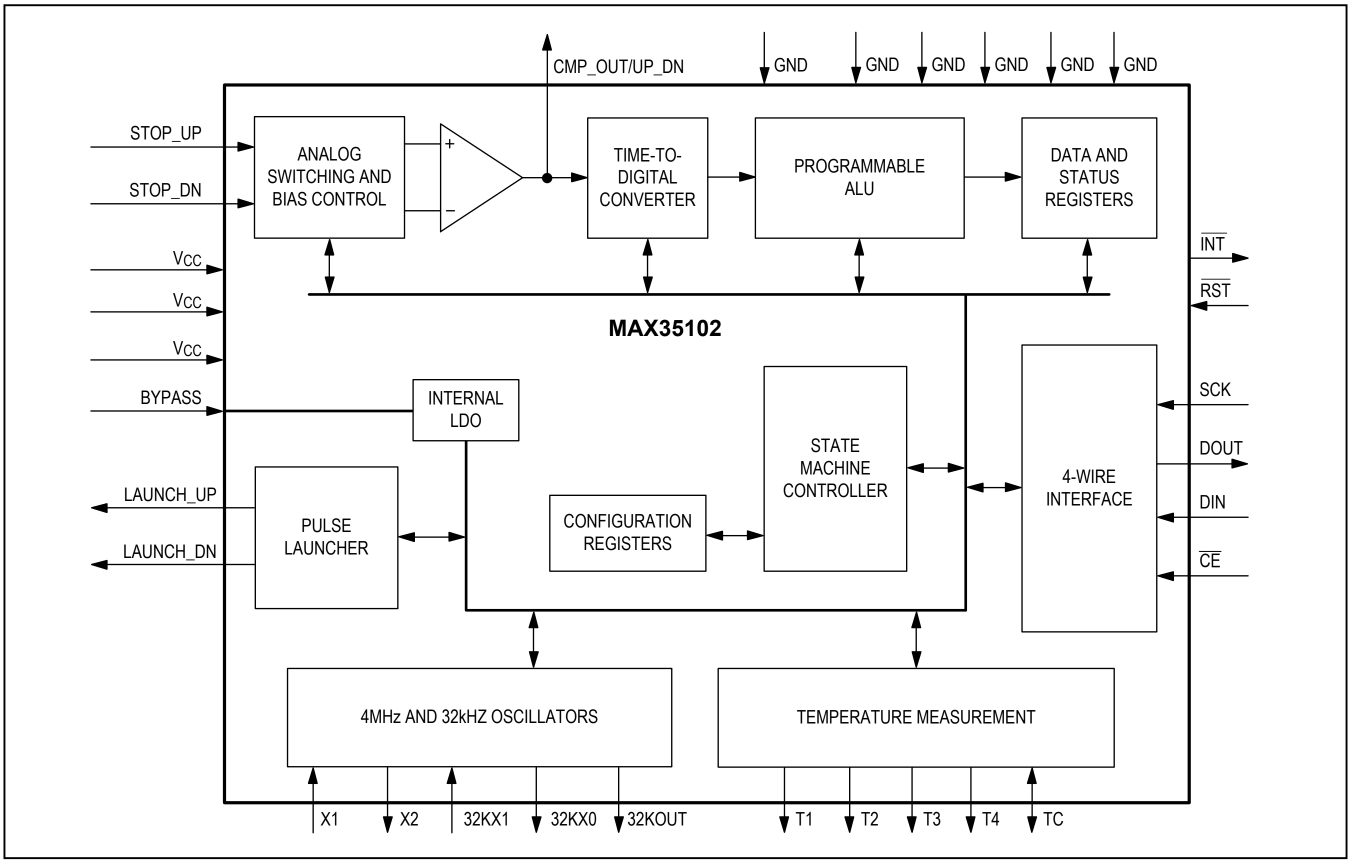
Pin Description

PIN	NAME	FUNCTION
1, 16, 22, 25, 28, 30	GND	Device Ground
2	BYPASS	Connect this pin to ground with a capacitor (100nF) to provide stability for the on-board low-dropout regulator. The effective series resistance of this capacitor needs to be in the 1Ω to 2Ω range.
3, 6, 29	V_{CC}	Main Supply. Typically sourced from a single lithium cell.
4	32KOUT	CMOS Output. Repeats the 32kHz crystal oscillator frequency.
5	LAUNCH_DN	CMOS Pulse Output Transmission in Downstream Direction of Water Flow
7	LAUNCH _UP	CMOS Pulse Output Transmission in Upstream Direction of Water Flow
8	CMP_OUT/UP_DN	CMOS Output. Indicates the direction (upstream or downstream) of which the pulse launcher is currently launching pulses OR the comparator output.
9	$\overline{\text{INT}}$	Active-Low Open-Drain Interrupt Output. The pin is driven low when the device requires service from the host microprocessor.
10	$\overline{\text{CE}}$	Active-Low CMOS Digital Input. Serial peripheral interface chip enable input.

Pin Description (continued)

PIN	NAME	FUNCTION
11	SCK	CMOS Digital Input. Serial peripheral interface clock input.
12	DIN	CMOS Digital Input. Serial peripheral interface data input.
13	DOUT	CMOS Output. Serial peripheral interface data output.
14	$\overline{RST}$	Active-Low CMOS Digital Reset Input
15	DNC	Do Not Connect. This pin must be left unconnected.
17	T1	Open-Drain Probe 1 Temperature Measurement
18	T2	Open-Drain Probe 2 Temperature Measurement
19	T3	Open-Drain Probe 3 Temperature Measurement
20	T4	Open-Drain Probe 4 Temperature Measurement
21	TC	Input/Output Temperature Measurement Capacitor Connection
23	32KX0	Connections for 32.768kHz Quartz Crystal. An external CMOS 32.768kHz oscillator can also drive the MAX35102. In this configuration, the 32KX1 pin is connected to the external oscillator signal and the 32KX0 pin is left unconnected.
24	32KX1	
26	STOP_DN	Downstream STOP Analog Input. Used for the signal that is received from the downstream transmission of a time-of-flight measurement.
27	STOP_UP	Upstream STOP Analog Input. Used for the signal that is received from the upstream transmission of a time-of-flight measurement.
31	X2	Connections for 4MHz Quartz Crystal. A ceramic resonator can also be used.
32	X1	
—	EP	Exposed Pad. Connect to GND.

Block Diagram



Detailed Description

The MAX35102 is a time-to-digital converter with built-in amplifier and comparator targeted as a complete analog front-end solution for the ultrasonic heat meter and flow meter markets.

With automatic differential time-of-flight (TOF) measurement, this device makes for simplified computation of liquid flow. Early edge detection ensures measurements are made with consistent wave patterns to greatly improve accuracy and eliminate erroneous measurements. Built-in arithmetic logic unit provides TOF difference measurements. A programmable receiver hit accumulator can be utilized to minimize the host microprocessor access.

Multihit capability with stop-enable windowing allows the device to be fine-tuned for the application. Internal analog switches, an autozero amplifier/comparator, and programmable receiver sensisitivity provide the analog interface and control for a minimal electrical bill of material solutions.

For temperature measurement, the MAX35102 supports up to four 2-wire PT1000/500 platinum resistive temperature detectors (RTD).

A simple opcode based 4-Wire SPI interface allows any microcontroller to effectively configure the device for its intended measurement.

Time-of-Flight (ToF) Measurement Operations

TOF is measured by launching pulses from one piezoelectric transducer and receiving the pulses at a second transducer. The time between when the pulses are launched and received is defined as the time of flight. The MAX35102 contains the functionality required to create a string of pulses, sense the receiving pulse string, and measure the time of flight. The MAX35102 can measure two separate TOFs, which are defined as TOF up and TOF down.

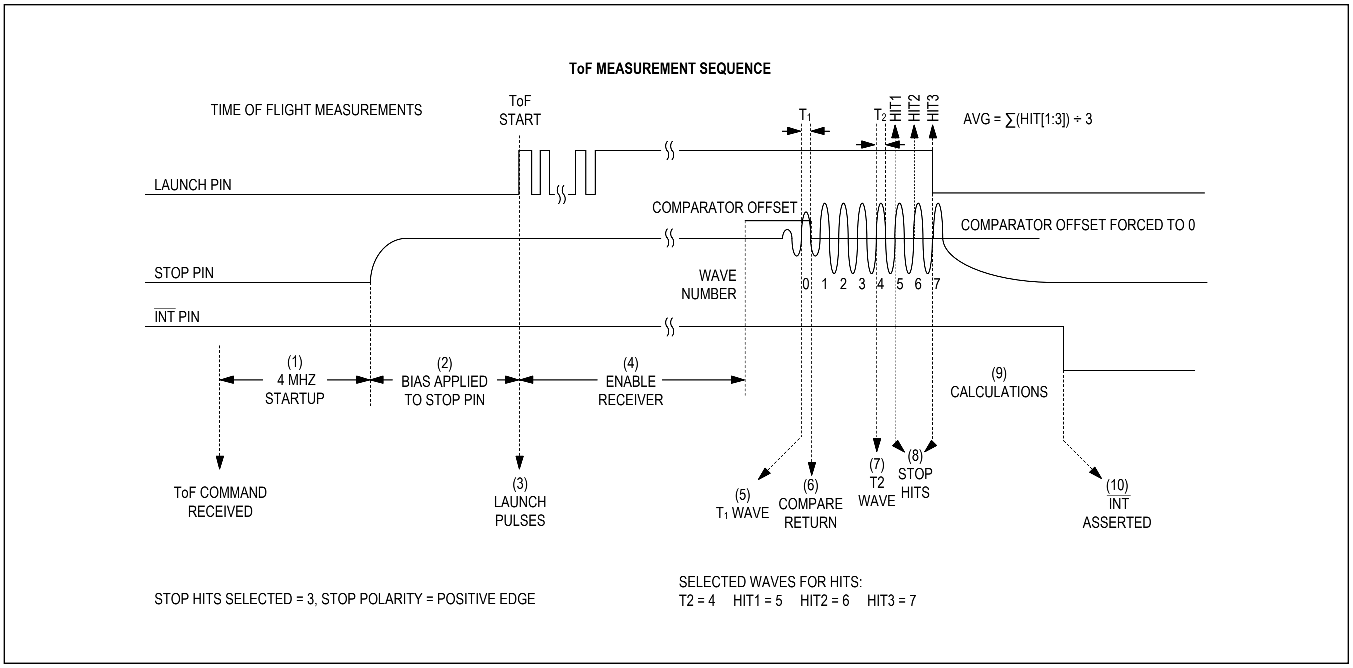


Figure 3. Time-of-Flight Sequence

A TOF up measurement has pulses launched from the LAUNCH_UP pin, which is connected to the downstream transducer. The ultrasonic pulse is received at the upstream transducer, which is connected to the STOP_UP pin. A TOF down measurement has pulses launched from the LAUNCH_DN pin, which is connected to the upstream transducer. The ultrasonic pulse is received at the downstream transducer, which is connected to the STOP_DN pin.

TOF measurements can be initiated by sending either the TOF_UP, TOF_DN, or TOF_DIFF commands.

The steps involved in a single TOF measurement are described here and shown in Figure 3.

1) The 4MHz oscillator and LDO is enabled with a programmable settling delay time set by the CLK_S[2:0] bits in Calibration and Control register.
2) A common-mode bias is enabled on the STOP pin. This bias charge time is set by the CT[1:0] bits in the TOF1 register.
3) Once the bias charge time has expired, the pulse launcher drives the appropriate LAUNCH pin with a programmable sequence of pulses. The number of pulses launched is set by the PL[7:0] bits in the TOF1 register. The frequency of these 50% duty-cycle pulses is set by the DPL[3:0] bits, also in the TOF1 register. The start of these launch pulses generates a start signal for the time-to-digital converter (TDC) and is considered to be time zero for the TOF measurement. This is denoted by the start signal in the start/stop TDC timing (Figure 3).
4) After a programmable delay time set in TOF Measurement Delay register, the comparator and hit detector at the appropriate STOP pin are enabled. This delay allows the receiver to start recording hits when the received wave is expected, eliminating possible false hits from noise in the system.
5) Stop hits are detected according to the programmed preferred edge of the acoustic signal sequence received at the STOP pin according to the setting of the STOP_POL bit in the TOF1 register. The first stop hit is detected when a wave received at the STOP pin exceeds the comparator offset voltage, which is set in the TOF6 and TOF7 registers. This first detected wave is wave number 0. The width of the wave's pulse that exceeds the comparator offset voltage is measured and stored as the t1 time.
6) The offset of the comparator then automatically and immediately switches to 0.
7) The t_2 wave is detected and the width of the t_2 pulse is measured and stored as the t_2 time. The wave number for the measurement of the t_2 wave width is set by the T2WV[5:0] bits in the TOF2 register.

8) Following the t_2 wave, 1 to 3 consecutive stop hits are then detected. For each hit, the measured TOF is stored in the appropriate HITxUPINT and HITxUPFrac or HITxDNINT and HITxDNFRAC registers. The number of hits to detect is set by the STOP[1:0] bits in the TOF2 register.

9) After receiving all of the programmed hits, the MAX35102 calculates the average of the recorded hits and stores this to AVGUPINT and AVGUPFrac or AVGDNInt and AVGDNFrac. The ratio of t_1/t_2 and t_2/t_{ideal} are calculated and stored in the WVRUP or WVRDN register.

10) Once all of the hit data, wave ratios, and averages become available in the Results registers, the TOF bit in the Interrupt Status register is set and the $\overline{\text{INT}}$ pin is asserted (if enabled) and remains asserted until the Interrupt Status register is accessed by the microprocessor with a Read Register command.

The computation of the total time of flight is performed by counting the number of full and fractional 4MHz clock cycles that elapsed between the launch start and a hit stop as shown in Figure 4.

Each TOF measurement result is comprised of an integer portion and a fractional portion. The integer portion is a binary representation of the number of t_{4MHz} periods that contribute to the time results. The fractional portion is a binary representation of one t_{4MHz} period quantized to a 16-bit resolution. The maximum size of the integer is 7FFFh or $(2^{15}-1) \times t_{4MHz}$ or ~ 8.19 ms. The maximum size of the fraction is:

$$\text{FFFFh or } \frac{2^{16}-1}{2^{16}} \times t_{4MHz}. \text{ or } \sim 249.9961 \text{ ns.}$$

Table 1. Two's Complement TOF_DIFF Conversion Example

REGISTER VALUE		CONVERTER VALUE
TOF_DIFFInt (hex)	**TOF_DIFFFrac (hex)**	**TOF DIFF VALUE (ns)**
7FFF	FFFF	8,191,999.9962
001C	0403	7,003.9177
0001	00A1	250.6142
0000	0089	0.5226
0000	0001	0.0038
0000	0000	0.0000
FFFF	FFFF	-0.0038
FFFF	FFC0	-0.2441
FFFE	1432	-480.2780
FF1C	8001	-56,874.9962
8000	0000	-8,192,000.0000

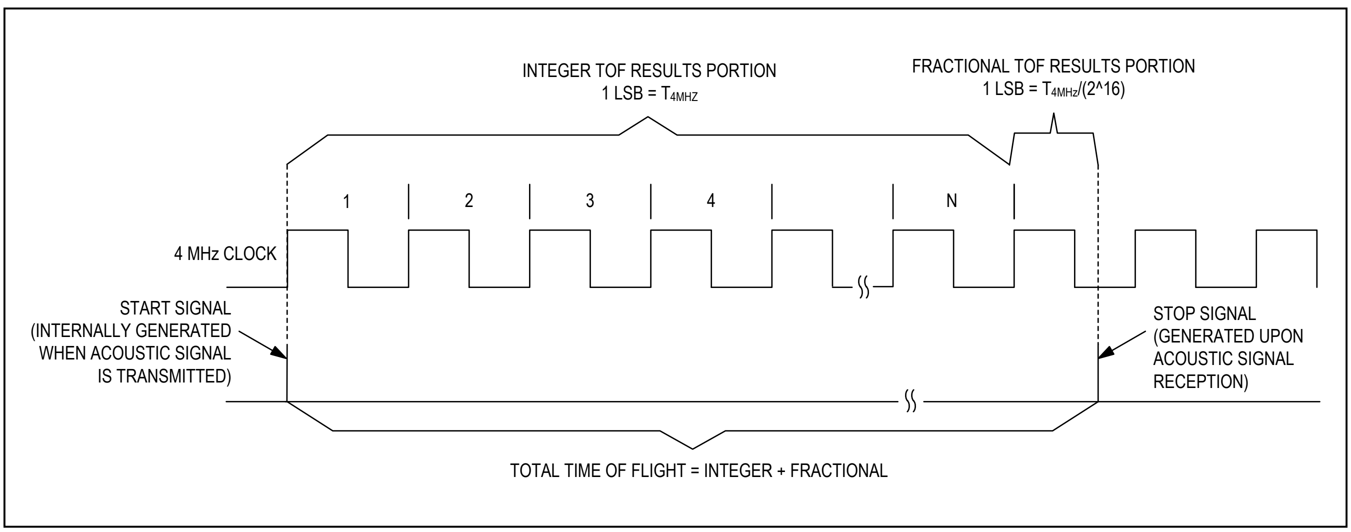


Figure 4.Start/Stop for Time-to-Digital Timing

Early Edge Detect

This early edge detect method of measuring the TOF of acoustic waves is used for all of the TOF commands including TOF_UP, TOF_DN, and TOF_DIFF. This method allows the MAX35102 to automatically control the input offset voltage of the receiver comparator so that it can provide advanced measurement accuracy. The input offset of the receiver comparator can be programmed with a range +31 LSBs if triggering on a positive edge and -32 LSBs if triggering on a negative edge, with 1 LSB = V_{CC}/3072. Separate input offset settings are available for the upstream received signal and the downstream received signal. The input offset for the upstream received signal is programmed using the C_OFFSETUP[4:0] bits in the TOF6 register. The input offset for the downstream received signal is programmed using the C_OFFSETDN[4:0] bits in the TOF7 register. Once the first hit is detected, the time t1 equal to the width of the earliest detectable edge is measured. The input offset voltage is then automatically and immediately returned to 0.

The MAX35102 is now ready to measure the successive hits. The next selected wave that is measured is the t_2 wave. In the example in Figure 5, this is the 7th wave after the early edge detect wave. The selection of the t_2 wave is made with the T2WV[5:0] bits in the TOF2 register.

With reference to Figure 5, the ratio t_1/t_2 is calculated and registered for the user. This ratio allows determination of abrupt changes in flow rate, received signal strength, partially filled tube detection, and empty tube. It also provides noise suppression to prevent erroneous edge detection. Also, the ratio t_2/t_{ideal} is calculated and registered for the user. For this calculation, t_{ideal} is1/2 the period of launched pulse. This ratio adds confirmation that the t_2 wave is a strong signal, which provides insight into the common mode offset of the received acoustic wave.

TOF Error Handling

Any of the TOF measurements can result in an error. If an error occurs during the measurement, all of the associated registers report FFFFh. If a TOF_DIFF is being performed, the TOF_DIFFInt and TOF_DIF_Frac registers report 7FFFh and FFFFh, respectively. If the measurement error is caused by the time measurement exceeding the timeout set by the TIMOUT[2:0] bits in the TOF2 register, then the TO bit in the Interrupt Status register is set and the $\overline{INT}$ pin asserts (if enabled).

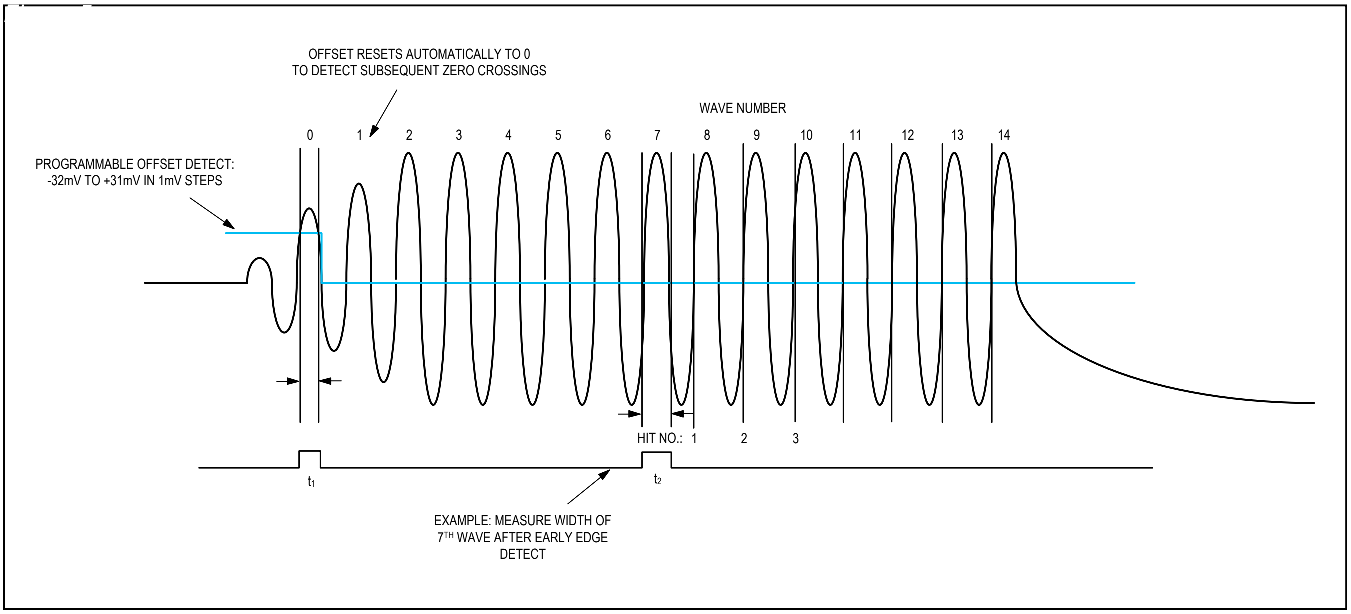


Figure 5. Early Edge Detect Received Wave Example

Temperature Measurement Operations

A temperature measurement is a time measurement of the RC circuit connected to the temperature port device pins T1 through T4 and TC. The TC device pin has a driver to charge the timing capacitor. The ports that are measured and the order in which the measurement is performed is selected with the TP[1:0] bits in the Temperature register.

Figure 6 depicts a 1000Ω platinum RTD with a 100nF NPO COG 30ppm/°C capacitor. It shows two dummy cycles with 4 temperature port evaluation measurements and 4 real temperature port measurements. This occurs when setting the TP[1:0] bits in the Temperature register to 11b.

The dummy 1 and dummy 2 cycles represent preamble measurements that are intended to eliminate the dielectric absorption of the temperature measurement capacitor. These dummy cycles are executed using a RTD Emulation resistor of 1000Ω internal to the MAX35102. This dummy path allows the dielectric absorption effects of the capacitor to be eliminated without causing any of the RTDs to be unduly self-heated. The number of dummy measurements to be taken ranges from 0 to 7. This parameter is configured by setting the PRECYC[2:0] bits in the Temperature register.

Following the dummy cycles, an evaluation, TXevaluate, is performed. This measurement allows the MAX35102 to maximize power efficiency by evaluating the temperature of the RTDs with a coarse measurement prior to a real measurement. The coarse measurement provides an approximation to the TDC converter. During the real measurement, the TDC can then optimize its measurement parameters to use power efficiently. These evaluate cycles are automatically inserted according to the order of ports selected with the of the Temperature Port bits. The time from the start of one port's temperature measurement to the next port's temperature measurement is set using with the PORTCYC[1:0] bits in the Temperature register.

Once all the temperature measurements are completed, the times measured for each port are reported in the corresponding TxInt and TxFrac Results registers. The TE bit in the Interrupt Status register is also set and the $\overline{\text{INT}}$ pin asserts (if enabled).

Actual temperature is determined by a ratiometric calculation. If T1 and T2 are connected to platinum RTDs and T3 and T4 are connected to the same reference resistor (as shown in the System Diagram), then the ratio of T1/T3 = R_{RTD1}/R_{REF} and T2/T4 = R_{RTD2}/R_{REF}. The ratios R_{RTD1}/R_{REF} and R_{RTD2}/R_{REF} can be determined by the host microprocessor and the temperature can be derived from a look-up table of Temperature vs. Resistance for each of the RTDs utilizing interpolation of table entries if required.

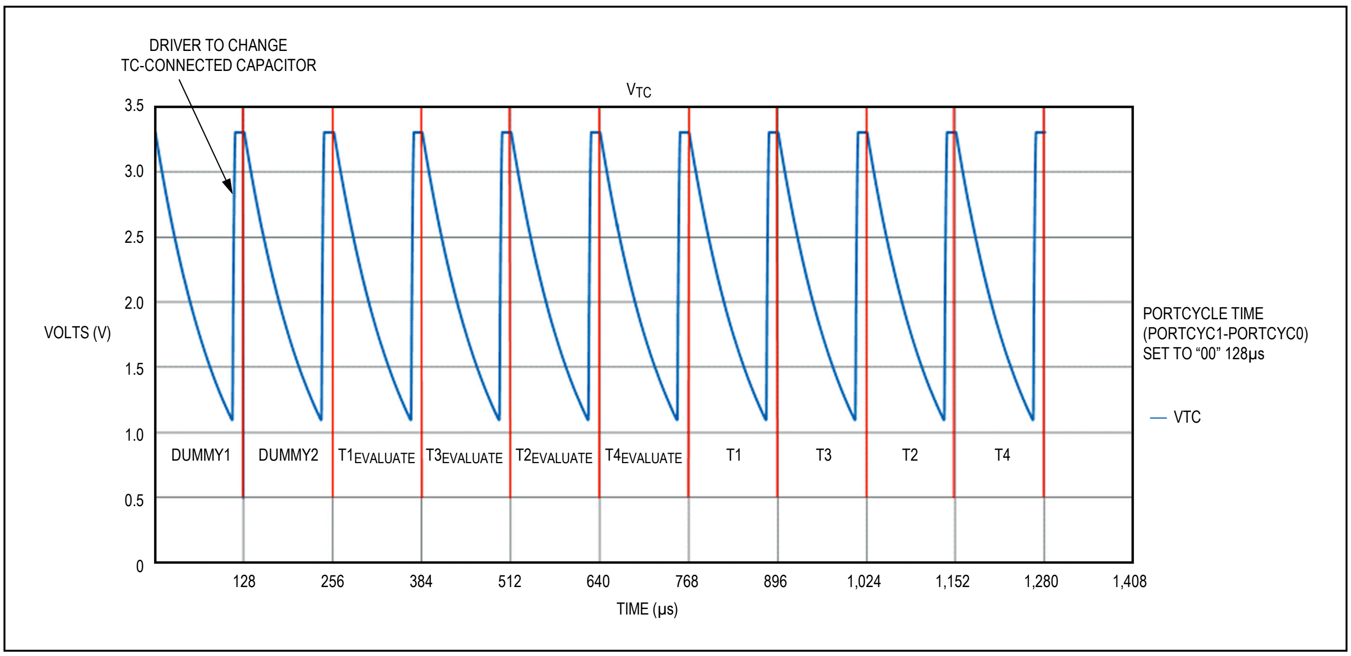


Figure 6. Temperature Command Execution Cycle Example

Temperature Error Handling

The temperature measurement unit can detect open and/or short-circuit temperature probes. If the resultant temperature reading in less than 8µs, then the MAX35102 writes a value of 0000h to the corresponding Results registers to indicate a short-circuit temperature probe. If the measurement process does not discharge the TC pin below the threshold of the internal temperature comparator within 2µs of the time set by the PORTCYC[1:0] bits in the Temperature register, then an open circuit temperature probe error is declared. The MAX35102 writes a value of FFFFh to the corresponding results registers to indicate an open circuit temperature probe, the TO bit in the Interrupt Status register is set, and the $\overline{\text{INT}}$ pin asserts (if enabled). If the temperature measurement error is caused by any other problems, then the MAX35102 writes a value of FFFFh to each of the temperature port results registers indicating that all of the temperature port measurements are invalid.

Calibration Operation

For more accurate results, calibration of the TDC can be performed. Calibration allows the MAX35102 to perform a calibration measurement that is based upon the 32.768kHz crystal, which is the most accurate clock in the system. This calibration is used when a ceramic oscillator is used in place of an AT-cut crystal for the 4MHz reference. The MAX35102 automatically generates START and STOP signals based upon edges of the 32.768kHz clock. The number of 32.768kHz clock periods that are used and then averaged are selected with the CAL_PERIOD[3:0] bits in the Calibration and Control register. The TDC measures the number of 4MHz clock pulses that occur during the 32.768kHz pulses. The measured time of a 32.768kHz clock pulse is reported in the CalibrationInt and CalibrationFrac Results registers.

Following is a description of an example calibration. Each TDC measurement is a 15-bit fixed-point integer value concatenated with a 16-bit fractional value binary representation of the number of t_{4MHz} periods that contribute to the time result, the actual period of t_{4MHz} needs to be known. If the CAL_PERIOD[3:0] bits in the Calibration and Control register are set to 6, then 6 measurements of 32.768kHz periods are measured by the TDC and then averaged. The expected measured value would be 30.5176µs/250ns = 122.0703125 t_{4MHz} periods. Assume that the 4MHz ceramic resonator is actually running at 4.02MHz. The TDC measurement unit would then measure 30.5176µs/248.7562ns = 122.6806641 t_{4MHz} periods and this result would be returned in the Calibration Results register. For all TDC measurements, a gain value of 122.0703125/122.6806641 = 0.995024876 would then be applied.

Calibration is performed when the Calibration command is sent to the MAX35102. At the completion of this calibration, the CAL bit in the Interrupt Status register and the $\overline{\text{INT}}$ pin asserts (if enabled).

Error Handling During Calibration

Any errors that occur during the Calibrate command stop the CalibrationInt and the CalibrationFrac Results registers from being updated with new calibration coefficients. The results for the previous Calibration data remain in these two registers and are used for scaling measured results. If the calibration error is caused by the internal calibration time measurement exceeding the time set by the TIMOUT[2:0] bits in the TOF2 register, then the TO bit in the Interrupt Status register is set and the $\overline{\text{INT}}$ pin asserts (if enabled).

Device Interrupt Operations

The MAX35102 is designed to optimize the power efficiency of a flow metering application by allowing the host microprocessor to remain in a low-power sleep mode, instead of requiring the microprocessor to keep track of complex real-time events being performed by the MAX35102. Upon completion of any command, the MAX35102 alerts the host microprocessor using the $\overline{\text{INT}}$ pin. The assertion of the $\overline{\text{INT}}$ pin can be used to awaken the host microprocessor from its low power mode. Upon receiving an interrupt on the $\overline{\text{INT}}$ pin, the host microprocessor should read the Interrupt Status Register to determine which tasks were completed.

Interrupt Status Register

The interrupt status register contains flags for all for all commands and events that occur within the MAX35102. These flags are set when the event occurs or at the completion of the executing command. When the Interrupt Status Register is read, all asserted bits are cleared. If another interrupt source has generated an interrupt during the read, these new flags assert following the read.

$\overline{\text{INT}}$ Pin

The $\overline{\text{INT}}$ pin asserts when any of the bits in the Interrupt Status register are set. The $\overline{\text{INT}}$ pin remains asserted until the Interrupt Status register is read by the user and all bits in this register are clear. In order for the $\overline{\text{INT}}$ pin to operate, it must first be enabled by setting the INT_EN bit in the Calibration and Control register.

Serial Peripheral Interface Operation

Four pins are used for SPI-compatible communications: DOUT (serial-data out), DIN (serial-data in), $\overline{CE}$ (chip enable), and SCK (serial clock). DIN and DOUT are the serial data input and output pins for the devices, respectively. The $\overline{CE}$ input initiates and terminates a data transfer. SCK synchronizes data movement between the master (microcontroller) and the slave (MAX35102). The SCK, which is generated by the microcontroller, is active only when $\overline{CE}$ is low and during opcode and data transfer to any device on the SPI bus. The inactive clock polarity is logic-low. DIN is latched on the falling edge of SCK. There is one clock for each bit transferred. Opcode bits are transferred in groups of eight, MSB first. Data bits are transferred in groups of sixteen, MSB first.

The serial peripheral interface is used to access the features and memory of the MAX35102 using an opcode/command structure.

Opcode Commands

Table 2 shows the opcode/commands that are supported by the device.

Execution Opcode Commands

The device supports several single byte opcode commands that cause the MAX35102 to execute various routines. All commands have the same SPI protocol sequence as shown in Figure 7. Once all 8 bits of the opcode are received by the MAX35102 and the $\overline{CE}$ device pin is deasserted, the MAX35102 begins execution of the specified command as described in that Command's description.

TOF_UP Command (00h)

The TOF_UP command generates a single TOF measurement in the upstream direction. Pulses launch from the LAUNCH_UP pin and are received by the STOP_UP pin. The measured hit results are reported in the HITxUPInt and HITxUPFrac registers, with the calculated average of all the measured hits being reported in the AVGUPInt and AVGUPFrac register. The t_1/t_2 and t_2/tideal wave ratios are reported in the WVRUP register. Once all these results are stored, then the TOF bit in the Interrupt Status register is set and the $\overline{INT}$ pin asserts (if enabled).

Note: The TOF_UP command yields a result that is only of use when used in conjunction with the TOF_DN command. Absolute TOF measurements include circuit delays and cannot be considered accurate.

Table 2. Opcode Commands

GROUP	COMMAND	OPCODE FIELD (HEX)
Execution Opcode Commands	TOF_Up	00h
	TOF_Down	01h
	TOF_Diff	02h
	Temperature	03h
	Reset	04h
	Initialize	05h
	Calibrate	0Eh
Register Opcode Commands	Read Register	B0h thru FFh. Each hex value represents the location of a single 16-bit register
	Write Register	30h thru 43h. Each hex value represents the location of a single 16-bit register

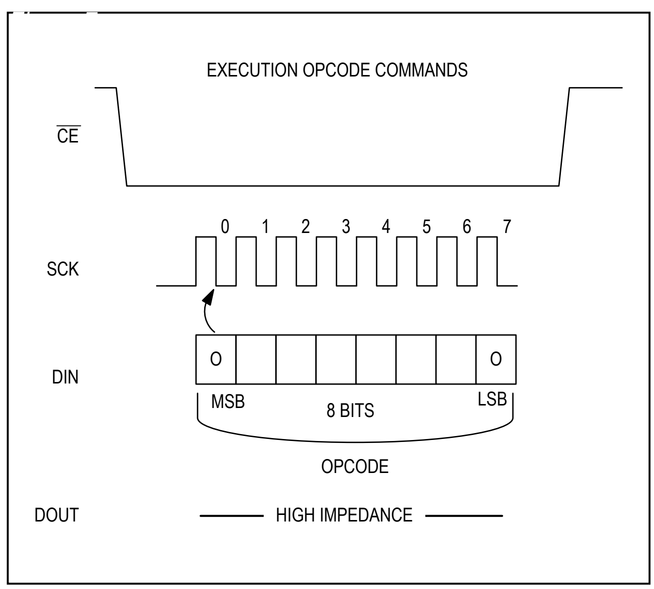


Figure 7. Execution Opcode Command Protocol

TOF_Down Command (01h)

The TOF_DOWN command generates a single TOF measurement in the downstream direction. Pulses launch from the LAUNCH_DN pin and are received by the STOP_DN pin. The measured hit results are reported in the HITxDnInt and HITxDnFrac registers, with the calculated average of all the measured hits being reported in the AVGDNInt and AVGDNFrac register. The t_1/t_2 and t_2/t_{ideal} wave ratios are reported in the WVRDN register. Once all these results are stored, then the TOF bit in the Interrupt Status register is set and the $\overline{\text{INT}}$ pin asserts (if enabled).

Note: The TOF_Down command yields a result that is only of use when used in conjunction with the TOF_UP command. Absolute TOF measurements include circuit delays and cannot be considered accurate.

TOF_DIFF Command (02h)

The TOF_DIFF command performs back-to-back TOF_UP and TOF_DN measurements as required for a metering application. The TOF_UP sequence is followed by the TOF_DN sequence. The time between the start of the TOF_UP measurement and the start of the TOF_DN measurement is set by the TOF_CYC[2:0] bits in the TOF2 register. Upon completion of the TOF_DN measurement, the results of AVGUP minus AVGDN is computed and stored at the TOF_DIFFInt and TOF_DIFFFrac Results register locations. Once these results are stored, then the TOF bit in the Interrupt Status register is set and the $\overline{\text{INT}}$ pin asserts (if enabled).

Temperature Command (03h)

The temperature command initiates a temperature measurement sequence as described in the *Temperature Measurement Operations* section. The characteristics the temperature measurement sequence depends upon the settings in the Temperature register. Once all the measurements are completed, the times measured for each port are reported in the corresponding TxInt and TxFrac Results registers. The TE bit in the Interrupt Status register also is set and the $\overline{\text{INT}}$ pin asserts (if enabled).

Reset Command (04h)

The reset command essentially performs the same function as a power-on reset (POR), and causes all of the Configuration registers to be set to their power-on reset values and all of the Results registers and the Interrupt Status register to be cleared and set to zero.

Initialize Command (05h)

The initialize command must be executed before any configuration of the device is done. This initializes the time-to-digital converter so that TOF and temperature commands can be executed. The MAX35102 sets the INIT bit in the Interrupt Status register and asserts the $\overline{\text{INT}}$ device pin (if enabled) to tell the host microprocessor that the initialize command has completed and the next desired command can be sent to the MAX35102.

Calibrate Command (0Eh)

The calibrate command performs the calibration routine as described in the calibration operation section. When the calibrate command has completed the measurement, the Calibration Results register contains the measured 32kHz period measurement value, the MAX35102 sets the calibration bit in the Interrupt Status register and then asserts the $\overline{\text{INT}}$ device pin (if enabled). The host microprocessor reads the Interrupt Status register to determine the interrupt source and then read the Calibration Results register to be able to calculate the 4MHz ceramic oscillator gain factor.

Register Opcode Commands

To manipulate the register memory, there are two commands supported by the device: Read Register and Write register. Each register accessed with these commands is 16 bits in length. These commands are used to access all sections of the memory map including the Configuration registers, Conversion Results registers, and Status registers. The Conversion Results registers and the Interrupt Status register of the Status registers are all read only.

Read Register Command

The opcode must be clocked into the DIN device pin before the DOUT device pin produces the register data. The SPI protocol sequence is shown in Figure 8.

The read register command can also be used to read consecutive addresses. In this case, the data bits are continuously delivered in sequence starting with the MSB of the data register that is addressed in the opcode, and continues with each SCK rising edge until the $\overline{\text{CE}}$ device pin is deasserted as shown in Figure 9. The address counter automatically increments.

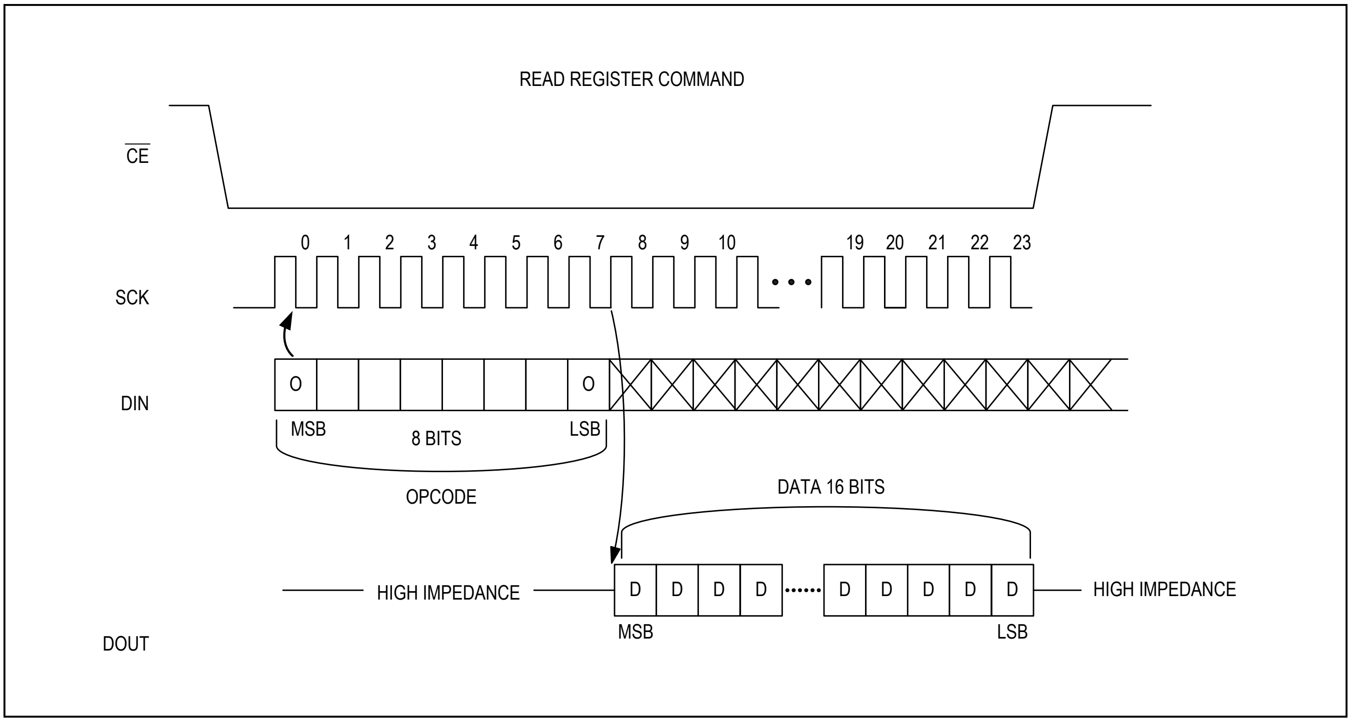


Figure 8. Read Register Opcode Command Protocol

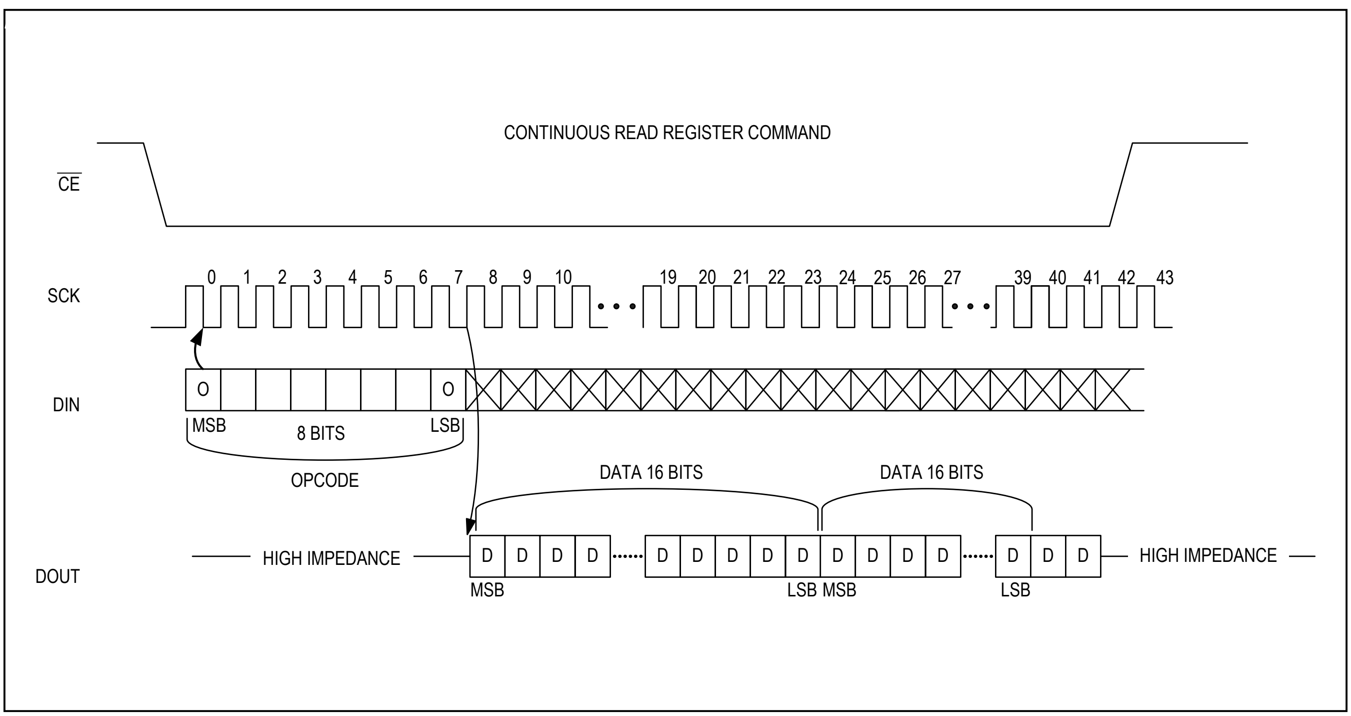


Figure 9. Continuous Read Register Opcode Command Protocol

Write Register Command

This command applies to all writable registers. See the *Register Memory Map* for more detail. The SPI protocol sequence is shown in Figure 10.

The write register command can also be used to write consecutive addresses. In this case, the data bits are continuously received on the DIN device pin and bound for the initial starting address register that is addressed in the opcode. The address counter automatically increments after each 16 bits of data if the SCK device pin is continually clocked and the $\overline{CE}$ device pin remain asserted as shown in Figure 11.

Register Memory Map

These registers are accessed by the read register command and the Write Register command: X represents a reserved bit. All addresses omitted are reserved

The Results, Interrupt Status, and Control registers are all 0000h following a reset.

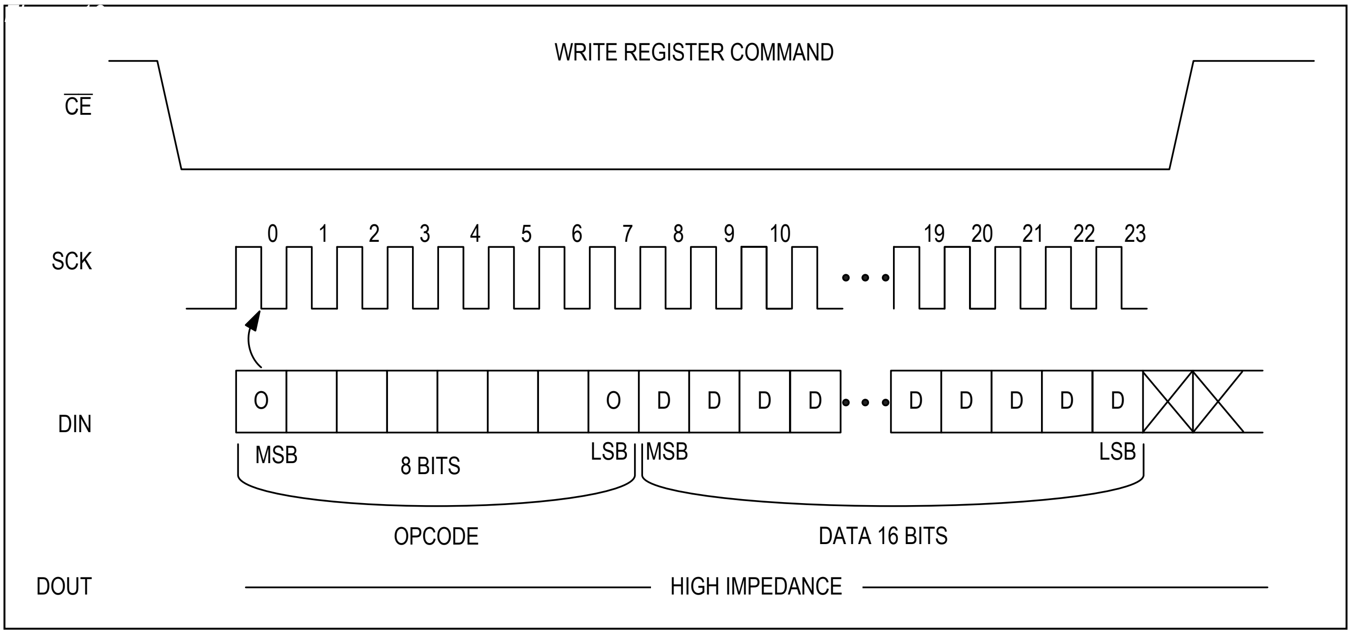


Figure 10. Write Register Opcode Command Protocol

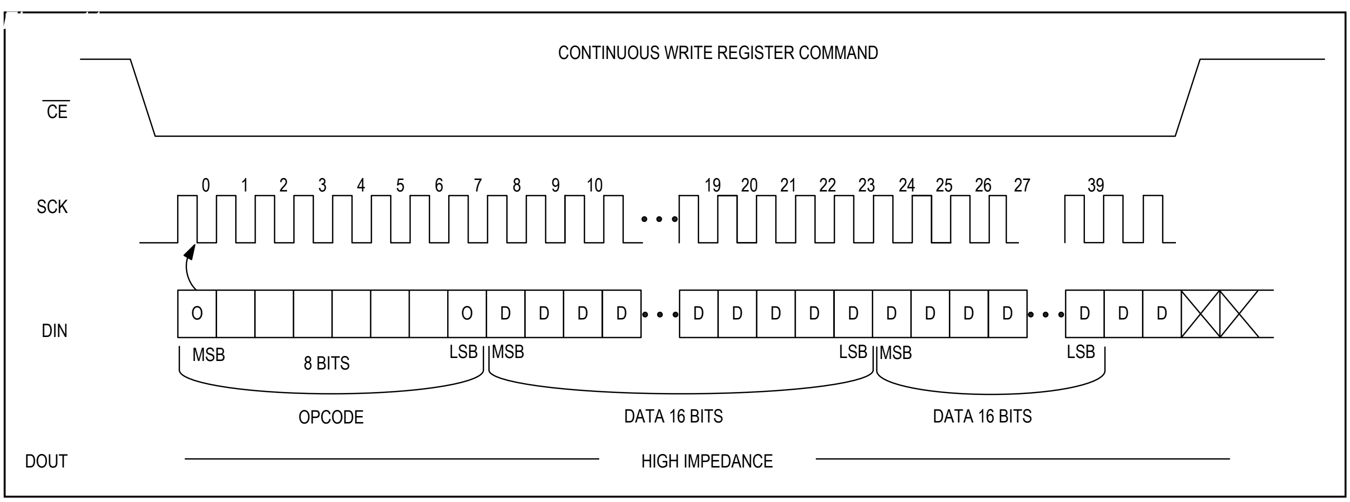


Figure 11. Continuous Write Register Opcode Command Protocol

Table 3. Register Memory Map

READ OPCODE	WRITE OPCODE	NAME	BITS[15:8]								BITS[7:0]							
CONFIGURATION REGISTERS																		
B6h	36h		Reserved															
B7h	37h		Reserved															
B8h	38h	TOF1	PL7	PL6	PL5	PL4	PL3	PL2	PL1	PL0	DPL3	DPL2	DPL1	DPL0	STOP_POL	X	CT1	CT0
B9h	39h	TOF2	STOP2	STOP1	STOP0	T2WV5	T2WV4	T2WV3	T2WV2	T2WV1	T2WV0	TOF_CYC2	TOF_CYC1	TOF_CYC0	EN_UP_DN	TIMOUT2	TIMOUT1	TIMOUT0
BDh	3Dh	TOF6	C_OFFSETRUP7	C_OFFSETRUP6	C_OFFSETRUP5	C_OFFSETRUP4	C_OFFSETRUP3	C_OFFSETRUP2	C_OFFSETRUP1	C_OFFSETRUP0	C_OFFSETUP7	C_OFFSETUP6	C_OFFSETUP5	C_OFFSETUP4	C_OFFSETUP3	C_OFFSETUP2	C_OFFSETUP1	C_OFFSETUP0
BEh	3Eh	TOF7	C_OFFSETRDN7	C_OFFSETRDN6	C_OFFSETRDN5	C_OFFSETRDN4	C_OFFSETRDN3	C_OFFSETRDN2	C_OFFSETRDN1	C_OFFSETRDN0	C_OFFSETDN7	C_OFFSETDN6	C_OFFSETDN5	C_OFFSETDN4	C_OFFSETDN3	C_OFFSETDN2	C_OFFSETDN1	C_OFFSETDN0
C0h	40h	Temperature	X	X	X	X	X	X	X	X	X	TP1	TP0	PRECYC2	PRECYC1	PRECYC0	PORTCYC1	PORTCYC0
C1h	41h	TOF Measurement Delay	DLY15	DLY14	LY13	DLY12	DLY11	DLY10	DLY9	DLY8	DLY7	DLY6	DLY5	DLY4	DLY3	DLY2	DLY1	DLY0
C2h	42h	Calibration and Control	X	X	X	X	CMP_EN	CMP_SEL	INT_EN	ET_CONT	CONT_INT	CLK_S2	CLK_S1	CLK_S0	Cal_Period3	Cal_Period2	Cal_Period1	Cal_Period0
C3h	43h	Oscillator	X	X	X	X	X	X	X	X	X	32K_BP	32K_EN	X	X	X	X	X
CONVERSION RESULTS REGISTERS																		
C4h	Read Only		WVRUP															
C5h	Read Only		Hit1UpInt															
C6h	Read Only		Hit1UpFrac															
C7h	Read Only		Hit2UpInt															
C8h	Read Only		Hit2UpFrac															
C9h	Read Only		Hit3UpInt															

Table 3. Register Memory Map (continued)

READ OPCODE	WRITE OPCODE	NAME	BITS[15:8]	BITS[7:0]
CAh	Read Only		Hit3UpFrac	
D1h	Read Only		AVGUPInt	
D2h	Read Only		AVGUPFrac	
D3h	Read Only		WVRDN	
D4h	Read Only		Hit1DnInt	
D5h	Read Only		Hit1DnFrac	
D6h	Read Only		Hit2DnInt	
D7h	Read Only		Hit2DnFrac	
D8h	Read Only		Hit3DnInt	
D9h	Read Only		Hit3DnFrac	
E0h	Read Only		AVGDNInt	
E1h	Read Only		AVGDNFrac	
E2h	Read Only		TOF_DIFFInt	
E3h	Read Only		TOF_DIFFFrac	
E7h	Read Only		T1Int	
E8h	Read Only		T1Frac	
E9h	Read Only		T2Int	

Table 3. Register Memory Map (continued)

EAh	Read Only		T2Frac															
READ OPCODE	**WRITE OPCODE**	**NAME**	**BITS[15:8]**								**BITS[7:0]**							
EBh	Read Only		T3Int															
ECh	Read Only		T3Frac															
EDh	Read Only		T4Int															
EEh	Read Only		T4Frac															
F8h	Read Only		CalibrationInt															
F9h	Read Only		CalibrationFrac															
FAh	Read Only		Reserved															
FBh	Read Only		Reserved															
FCh	Read Only		Reserved															
FDh	Read Only		Reserved															
STATUS REGISTERS																		
FEh	Read Only	Interrupt Status	TO	X	X	TOF	TE	LDO	X	X	X	CAL	X	X	INIT	POR	X	X

Configuration Register Descriptions

Table 4. TOF1 Register

WRITE OPCODE 38h	READ OPCODE B8h	POWER-ON RESET VALUE 0010h

Bit	15	14	13	12	11	10	9	8
Name	PL7	PL6	PL5	PL4	PL3	PL2	PL1	PL0

Bit	7	6	5	4	3	2	1	0
Name	DPL3	DPL2	DPL1	DPL0	STOP_POL	X	CT1	CT0

BIT	NAME	DESCRIPTION
15:8	PL[7:0]	**Pulse Launcher Size**: This is a hex value that defines the number of pulses that will be launched from the pulse launcher during transmission. The range of this hex value is 00h to FFh. When PL[7:0] is set to 00h, the Pulse Launcher is disabled. Up to 127 pulses can be launched. When PL7 is set, the pulse count is clamped at 127.
7:4	DPL[3:0]	**Pulse Launch Divider:** This is a hex value that defines the divider ratio of the internal clock signal used to drive the Pulse Launch signal. The 4MHz external reference oscillator is used as the source for the internal clock reference. The internal reference clock is first divided by 2 to produce a 2MHz clock. The range of this hex value is 1h to Fh, resulting in a range of division from ÷2 to ÷16 of the 2MHz clock. A value of 0h is not supported and should not be programmed Pulse Launch Frequency = 2MHz/(1+DPL[3:0])
		DPL[3:0] | **PULSE LAUNCH FREQUENCY** 0000b | RESERVED 0001b | 1MHz 0002b | 666kHz …. | …. 1110b | 133.33kHz 1111b | 125kHz
3	STOP_POL	**Stop Polarity:** This bit defines the edge sensitivity of the STOP_UP and STOP_DN channel. The signal received on the STOP_UP and STOP_DN device pins will generate a stop condition for the internal TDC time count on the rising slope of this signal if this bit is set to 0. The signal received on the STOP_UP and STOP_DN device pins will generate a stop condition for the internal TDC time count on the falling slope of this signal if this bit is set to 1.
2	X	Reserved

Table 4. TOF1 Register (continued)

BIT	NAME	DESCRIPTION			
1:0	CT[1:0]	**Bias Charge Time:** This is the time allotted for charging the external bias network on the STOP pins to produce common mode biasing for the analog receiver/comparator. It is based upon the 32.768 KHz crystal:			
		CT1	CT2	DESCRIPTION	
				32kHz CLOCK CYCLES (decimal)	TYPICAL TIME (µs)
		0	0	2	61
		0	1	4	122
		1	0	8	244
		1	1	16	488

Table 5. TOF2 Register

WRITE OPCODE 39h	READ OPCODE B9h	POWER-ON RESET VALUE 0000h

Bit	15	14	13	12	11	10	9	8
Name	X	STOP1	STOP0	T2WV5	T2WV4	T2WV3	T2WV2	T2WV1
Bit	7	6	5	4	3	2	1	0
Name	T2WV0	TOF_CYC2	TOF_CYC1	TOF_CYC0	X	TIMOUT2	TIMOUT1	TIMOUT0

BIT	NAME	DESCRIPTION		
15	X	Reserved		
14:13	STOP[1:0]	**Stop Hits:** These bits set the number of stop hits to be expected and measured.		
		STOP1	STOP0	DESCRIPTION
		0	0	1 Hit
		0	1	2 Hits
		1	0	3 Hits
		1	1	3 Hits
12:7	T2WV[5:0]	**Wave Selector for t_2:** These bits determine the wave number for which t_2 is measured. To ensure measurement accuracy, the first wave measurable after the early edge detect is wave 2. Waves are numbered as depicted in Figure 5.		
		T2WV[5:0] (decimal)	DESCRIPTION	
		0 through 2	Wave 2	
		3	Wave 3	
		4	Wave 4	

Table 5. TOF2 Register (continued)

<table>
<tr><th>BIT</th><th>NAME</th><th colspan="4">DESCRIPTION</th></tr>
<tr><td rowspan="11">6:4</td><td rowspan="11">TOF_CYC[2:0]</td><td colspan="4">TOF Duty Cycle: These bits determine the time delay between successive executions of TOF measurements. It is the start-to-start time of automatic execution of the TOF_UP and the TOF_DN and is applicable only for the TOF_DIFF command. It is based upon the 32.768kHz crystal. If the actual TOF of the acoustic path exceeds the programmed start-to-start time in this setting, then the TOF duty cycle performs as if the bit setting is 000b.</td></tr>
<tr><th rowspan="2">TOF_CYC[2:0]</th><th colspan="3">DESCRIPTION</th></tr>
<tr><th>32kHz CLOCK CYCLES (decimal)</th><th>TYPICAL TIME</th><th>4MHz ON BETWEEN TOF_ UP and TOF_DOWN</th></tr>
<tr><td>000b</td><td>0</td><td>0µs</td><td>Yes</td></tr>
<tr><td>001b</td><td>4</td><td>122µs</td><td>Yes</td></tr>
<tr><td>010b</td><td>8</td><td>244µs</td><td>Yes</td></tr>
<tr><td>011b</td><td>16</td><td>488µs</td><td>Yes</td></tr>
<tr><td>100b</td><td>24</td><td>732µs</td><td>Yes</td></tr>
<tr><td>101b</td><td>32</td><td>976µs</td><td>Yes</td></tr>
<tr><td>110b</td><td>546</td><td>16.65ms</td><td>No</td></tr>
<tr><td>111b</td><td>655</td><td>19.97ms</td><td>No</td></tr>
<tr><td>3</td><td>X</td><td colspan="4">Reserved</td></tr>
<tr><td rowspan="10">2:0</td><td rowspan="10">TIMOUT[2:0]</td><td colspan="4">Timeout: These bits force a timeout in the time-to-digital measurement block. If the hit required to measure t_1, t_2, or Hit1 through Hit3 of the received signal does not occur in this time, the TO bit in the Interrupt Status register is set and the $\overline{INT}$ pin is asserted (if enabled). Additionally, any of the Conversion Results registers read FFFFh if the data for that register is invalid.</td></tr>
<tr><th>TIMOUT2</th><th>TIMOUT1</th><th>TIMOUT0</th><th>DESCRIPTION (µs)</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>128</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>256</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>512</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>1024</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>2048</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>4096</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>8192</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>16384</td></tr>
</table>

Table 6. TOF6 Register

WRITE OPCODE 3Dh	READ OPCODE BDh	POWER-ON RESET VALUE 0000h

Bit	15	14	13	12	11	10	9	8
Name	X	X	X	X	X	X	X	X
Bit	7	6	5	4	3	2	1	0
Name	X	X	X	C_OFFSET UP4	C_OFFSET UP3	C_OFFSET UP2	C_OFFSET UP1	C_OFFSET UP0

BIT	NAME	DESCRIPTION
15:5	X	Reserved
4:0	C_OFFSETUP [4:0]	**Comparator Offset Upstream:** These bits define an initial selected receive comparator offset voltage for the analog receiver comparator front-end. This comparator offset is used to detect the early edge wave, t_1. The actual common-mode voltage is dependent upon and scales with the voltage present at the V_{CC} pins. When the STOP_POL bit in the TOF1 register is set to zero indicating a rising edge detection of the zero crossing of the received acoustic wave, then the comparator offset is a positive value. When the STOP_POL bit in the TOF1 register is set to one indicating a falling edge detection of the zero crossing of the received acoustic wave, then the comparator offset is a negative value. The following formulas define the comparator offset voltage setting $\text{STOP\_POL} = 0 \quad \text{Comparator Offset Voltage} = V_{CC} \times \frac{(1152 + C_{OFFSETUP})}{3072}$ $\text{STOP\_POL} = 1 \quad \text{Comparator Offset Voltage} = V_{CC} \times \frac{(1151 - C_{OFFSETUP})}{3072}$ $\text{where 1 LSB} = \frac{V_{CC}}{3072}$

C_OFFSETUP[4:0]	OFFSET (LSBs)
00h through 1Fh	0 through 31

Table 7. TOF7 Register

WRITE OPCODE 3Eh	READ OPCODE BEh	POWER-ON RESET VALUE 0000h

Bit	15	14	13	12	11	10	9	8
Name	X	X	X	X	X	X	X	X

Bit	7	6	5	4	3	2	1	0
Name	X	X	X	C_OFFSET DN4	C_OFFSET DN3	C_OFFSET DN2	C_OFFSET DN1	C_OFFSET DN0

BIT	NAME	DESCRIPTION
15:5	X	Reserved
4:0	C_OFFSETDN [4:0]	**Comparator Offset Downstream:** These bits define an initial selected receive comparator offset voltage for the analog receiver comparator front-end. This comparator offset is used to detect the early edge wave, t_1. The actual common-mode voltage is dependent upon and scales with the voltage present at the V_{CC} pins. When the STOP_POL bit in the TOF1 register is set to zero indicating a rising edge detection of the zero crossing of the received acoustic wave, then the comparator offset is a positive value. When the STOP_POL bit in the TOF1 register is set to one indicating a falling edge detection of the zero crossing of the received acoustic wave, then the comparator offset is a negative value. The following formulas define the comparator offset voltage setting: $\text{STOP\_POL} = 0 \quad \text{Comparator Offset Voltage} = V_{CC} \times \frac{(1152 + C_{OFFSETDN})}{3072}$ $\text{STOP\_POL} = 1 \quad \text{Comparator Offset Voltage} = V_{CC} \times \frac{(1151 - C_{OFFSETDN})}{3072}$ $\text{where 1 LSB} = \frac{V_{CC}}{3072}$

C_OFFSETDN[4:0]	OFFSET (LSBs)
00h through 1Fh	0 through 31

Table 8. Temperature Register

WRITE OPCODE 40h		READ OPCODE C0h		POWER-ON RESET VALUE 0000h				
Bit	15	14	13	12	11	10	9	8
Name	X	X	X	X	X	X	X	X
Bit	7	6	5	4	3	2	1	0
Name	X	TP1	TP0	PRECYC2	PRECYC1	PRECYC0	PORTCYC1	PORTCYC0

BIT	NAME	DESCRIPTION
15:7	X	Reserved
6:5	TP[1:0]	**Temperature Port:** These bits set the number of temperature ports to stimulate during a temperature measurement sequence and the sequence in which the temperature ports are stimulated.
4:2	PRECYC[2:0]	**Preamble Temperature Cycle:** These 3 bits are used to set the number of cycles to use as preamble for reducing dielectric absorption of the temperature measurement capacitor. Each cycle comprises one temperature measurement sequence as defined by the TP[1:0] bits.
1:0	PORTCYC[1:0]	**Port Cycle Time:** These two bits define the time interval between successive individual temperature port measurements. It is a start-to-start time. These bits also define the timeout function of the temperature measurement ports. See the *Temperature Operation* section for timeout details.

TP[1:0]:

TP1	TP0	DESCRIPTION
0	0	Measure ports T1 and T3
0	1	Measure ports T2 and T4
1	0	Measure ports T1, T3, and T2
1	1	Measure ports T1, T3, T2, and T4

PRECYC[2:0]:

PRECYC2	PRECYC1	PRECYC0	DESCRIPTION
0	0	0	0 dummy cycle
0	0	1	1 dummy cycles
0	1	0	2 dummy cycles
0	1	1	3 dummy cycles
1	0	0	4 dummy cycles
1	0	1	5 dummy cycles
1	1	0	6 dummy cycles
1	1	1	7 dummy cycles

PORTCYC[1:0]:

PORTCYC1	PORTCYC0	DESCRIPTION (µs)
0	0	128
0	1	256
1	0	384
1	1	512

Table 9. ToF Measurement Delay Register

WRITE OPCODE 41h	READ OPCODE C1h	POWER-ON RESET VALUE 0000h

Bit	15	14	13	12	11	10	9	8
Name	DLY15	DLY14	DLY13	DLY12	DLY11	DLY10	DLY9	DLY8

Bit	7	6	5	4	3	2	1	0
Name	DLY7	DLY6	DLY5	DLY4	DLY3	DLY2	DLY1	DLY0

BIT	NAME	DESCRIPTION
15:0	DLY[15:0]	This is hexadecimal value ranging from 0000h to FFFFh (decimal 0 to 65535). It is a multiple of the 4MHz crystal period (250ns). Settings less than 0012h are reserved and should not be used. The analog comparator driven by the STOP_UP and STOP_DN device pins does not generate a stop condition until this delay, counted from the internally generated start pulse for the acoustic wave, has expired. This delay applies to early edge detect wave. Care must be taken to set the TIMOUT bits in the TOF2 register so that a timeout interrupt does not occur before this delay expires.

Table 10. Calibration and Control Register

WRITE OPCODE 42h	READ OPCODE C2h	POWER-ON RESET VALUE 0000h

Bit	15	14	13	12	11	10	9	8
Name	X	X	X	X	CMP_EN	CMP_SEL	INT_EN	X

Bit	7	6	5	4	3	2	1	0
Name	X	CLK_S2	CLK_S1	CLK_S0	CAL_ PERIOD3	CAL_ PERIOD2	CAL_ PERIOD1	CAL_ PERIOD0

BIT	NAME	DESCRIPTION
15:12	X	Reserved
11	CMP_EN	**Comparator/UP_DN Output Enable:** 1 = CMP_OUT/UP_DN output device pin is enabled. 0 = CMP_OUT/UP_DN output device pin is driven low.

Table 10. Calibration and Control Register (continued)

<table>
<tr><th>BIT</th><th>NAME</th><th>DESCRIPTION</th></tr>
<tr><td>10</td><td>CMP_SEL</td><td>Comparator/UP_DN Output Select: This bit selects the output function of the CMP_OUT/UP_DN pin and is only used when CMP_EN = 1.
1 = CMP_EN: The output monitors the receiver front end comparator output.
0 = UP_DN: The output monitors the launch direction of the pulse launcher.
High Output: Upstream measurement (Launch_UP to STOP_UP)
Low Output: Downstream measurement (Launch_DN to STOP_DN)</td></tr>
<tr><td>9</td><td>INT_EN</td><td>Interrupt Enable: This bit, when set, enables the $\overline{INT}$ pin. All interrupt sources are wire-ORed to the $\overline{INT}$ pin.</td></tr>
<tr><td>8</td><td>X</td><td>Reserved</td></tr>
<tr><td>7</td><td>X</td><td>Reserved</td></tr>
<tr><td>6:4</td><td>CLK_S[2:0]</td><td>Clock Settling Time: These bits define the time interval that the MAX35102 waits after enabling the 4MHz clock for it to stabilize before making any measurements of time or temperature.
<table>
<tr><th rowspan="2">CLK_S2</th><th rowspan="2">CLK_S1</th><th rowspan="2">CLK_S0</th><th colspan="2">DESCRIPTION</th></tr>
<tr><th>32kHz CLOCK CYCLES</th><th>TYPICAL TIME</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>16</td><td>488μs</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>48</td><td>1.46ms</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>96</td><td>2.93ms</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>128</td><td>3.9ms</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>168</td><td>5.13ms</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td colspan="2">4MHz oscillator on continuously</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td colspan="2">4MHz oscillator on continuously</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td colspan="2">4MHz oscillator on continuously</td></tr>
</table></td></tr>
<tr><td>3:0</td><td>CAL_PERIOD[3:0]</td><td>4MHz Ceramic Oscillator Calibration Period: These bits define the number of 32.768kHz oscillator periods to measure for determination of the 4MHz ceramic oscillator period.
32kHz clock cycles = 1+ CAL_PERIOD[3:0]
<table>
<tr><th rowspan="2">CAL_PERIOD[3:0] (decimal)</th><th colspan="2">DESCRIPTION</th></tr>
<tr><th>32kHz CLOCK CYCLES (decimal)</th><th>32kHz CLOCK CYCLES (μs)</th></tr>
<tr><td>0</td><td>1</td><td>30.5</td></tr>
<tr><td>1</td><td>2</td><td>61</td></tr>
<tr><td>….</td><td>….</td><td>….</td></tr>
<tr><td>14</td><td>15</td><td>457.7</td></tr>
<tr><td>15</td><td>16</td><td>488.0</td></tr>
</table></td></tr>
</table>

Table 11. Oscillator Register

WRITE OPCODE 43h	READ OPCODE C3h	POWER-ON RESET VALUE 0000h

Bit	15	14	13	12	11	10	9	8
Name	X	X	X	X	X	X	X	X
Bit	7	6	5	4	3	2	1	0
Name	X	32K_BP	32K_EN	EOSC	X	X	X	X

BIT	NAME	DESCRIPTION
15:7	X	Reserved
6	32K_BP	**32kHz Bypass:** This bit, when set, allows an external CMOS-level 32.768kHz signal to be applied to the 32KX1 device pin. The internal 32.768kHz oscillator is bypassed and the external signal is driven into the MAX35102 core.
5	32K_EN	**32kHz Clock Output Enable:** This bit enables the 32KOUT device pin to drive a CMOS-level square wave representation of the 32kHz crystal.
4	EOSC	**Enable Oscillator:** This active-low bit when set to logic 0 starts the 32kHz oscillator. When this bit is set to logic 1, the oscillator is stopped.
3:0	X	Reserved

Status Register Descriptions

Table 12. Interrupt Status Register

WRITE OPCODE Read Only	READ OPCODE FEh	POWER-ON RESET VALUE 0000h

Bit	15	14	13	12	11	10	9	8
Name	TO	X	X	TOF	TE	X	X	X
Bit	7	6	5	4	3	2	1	0
Name	X	CAL	X	X	INIT	POR	X	X

Note: This register is read only and bits are self-clearing upon a read to this register. See the *Device Interrupt Operations* section for more information.

BIT	NAME	DESCRIPTION
15	TO	**Timeout:** The TO bit is set if any one of the t_1, t_2, Hit1 through Hit3, or temperature measurements do not occur within the associated timeout window.
14:13	X	Reserved

Table 12. Interrupt Status Register (continued)

BIT	NAME	DESCRIPTION
12	TOF	**Time of Flight:** Set when the TOF_UP, TOF_DN, or TOF_DIFF command has completed.
11	TE	**Temperature:** Set when the temperature command has completed.
10:7	X	Reserved
6	CAL	**Calibrate:** Set after completion of the Calibrate command when the command is manually sent by the host microprocessor.
5	X	Reserved
4	X	Reserved
3	INIT	**Initialize:** Set when the Initialize command has completed.
2	POR	**Power-On-Reset:** Set when the MAX35102 has been successfully powered by application of V_{CC}. Upon application of power, the SPI port becomes inactive until this bit has been set.
1:0	X	Reserved

Conversion Results Register Descriptions

The devices conversion results registers are all read-only volatile SRAM. The POR value for all registers is 0000h.

Table 13. Conversion Results Registers Description

<table>
<tr><th>READ ONLY ADDRESS</th><th>NAME</th><th colspan="8">DESCRIPTION</th></tr>
<tr><td rowspan="7">C4h</td><td rowspan="7">WVRUP</td><td colspan="8">Bit 15 through Bit 8 holds the 8-bit value of the pulse width ratio ($t_1 \div t_2$).for the upstream measurement. Each bit is weighted as follows:</td></tr>
<tr><td>BIT 15</td><td>BIT 14</td><td>BIT 13</td><td>BIT 12</td><td>BIT 11</td><td>BIT 10</td><td>BIT 9</td><td>BIT 8</td></tr>
<tr><td>1</td><td>0.5</td><td>0.25</td><td>0.125</td><td>0.0625</td><td>0.03125</td><td>0.015625</td><td>0.0078125</td></tr>
<tr><td colspan="8">Bit 7 thru bit 0 holds the 8-bit value of the pulse width ratio ($t_2 \div t_{ideal}$) where t_{ide}al is equal to half the period of the Pulse Launch Frequency for the upstream measurement. Each bit is weighted as follows:</td></tr>
<tr><td>BIT 7</td><td>BIT 6</td><td>BIT 5</td><td>BIT 4</td><td>BIT 3</td><td>BIT 2</td><td>BIT 1</td><td>BIT 0</td></tr>
<tr><td>1</td><td>0.5</td><td>0.25</td><td>0.125</td><td>0.0625</td><td>0.03125</td><td>0.015625</td><td>0.0078125</td></tr>
<tr><td colspan="8">The maximum value of each of these ratios is 1.9921875.</td></tr>
<tr><td>C5h</td><td>Hit1UPInt</td><td colspan="8">15-bit fixed-point integer value of the first hit in the upstream direction. This integer portion is a binary representation of the number of t_{4MHz} periods that contribute to the time results. The maximum size of the integer is 7FFFh or $(2^{15} - 1) \times t_{4MHz}$.</td></tr>
<tr><td>C6h</td><td>Hit1UPFrac</td><td colspan="8">16-bit fractional value of the first hit in the upstream direction. This fractional portion is a binary representation of one t_{4MHz} period quantized to a 16-bit resolution. The maximum size of the fraction is FFFFh or $(2^{16} - 1)/2^{16} \times t_{4MHz}$.</td></tr>
</table>

Table 13. Conversion Results Registers Description (continued)

<table>
<tr><th>READ ONLY ADDRESS</th><th>NAME</th><th colspan="8">DESCRIPTION</th></tr>
<tr><td>C7h</td><td>Hit2UPInt</td><td colspan="8">15-bit fixed-point integer value of the second hit in the upstream direction. This integer portion is a binary representation of the number of t_{4MHz} periods that contribute to the time results. The maximum size of the integer is 7FFFh or $(2^{15} - 1) \times t_{4MHz}$.</td></tr>
<tr><td>C8h</td><td>Hit2UPFrac</td><td colspan="8">16-bit fractional value of the second hit in the upstream direction. This fractional portion is a binary representation of one t_{4MHz} period quantized to a 16-bit resolution. The maximum size of the fraction is FFFFh or $(2^{16} - 1)/2^{16} \times t_{4MHz}$.</td></tr>
<tr><td>C9h</td><td>Hit3UPInt</td><td colspan="8">15-bit fixed-point integer value of the third hit in the upstream direction. This integer portion is a binary representation of the number of t_{4MHz} periods that contribute to the time results. The maximum size of the integer is 7FFFh or $(2^{15} - 1) \times t_{4MHz}$.</td></tr>
<tr><td>CAh</td><td>Hit3UPFrac</td><td colspan="8">16-bit fractional value of the third hit in the upstream direction. This fractional portion is a binary representation of one t_{4MHz} period quantized to a 16-bit resolution. The maximum size of the fraction is FFFFh or $(2^{16} - 1)/2^{16} \times t_{4MHz}$.</td></tr>
<tr><td>D1h</td><td>AVGUPInt</td><td colspan="8">15-bit fixed-point integer value of the average of the hits recorded in the upstream direction This integer portion is a binary representation of the number of t_{4MHz} periods that contribute to the time results. The maximum size of the integer is 7FFFh or $(2^{15} - 1) \times t_{4MHz}$.</td></tr>
<tr><td>D2h</td><td>AVGUPFrac</td><td colspan="8">16-bit fractional value of the average of the hits recorded in the upstream direction. This fractional portion is a binary representation of one t_{4MHz} period quantized to a 16-bit resolution. The maximum size of the fraction is FFFFh or $(2^{16} - 1)/2^{16} \times t_{4MHz}$.</td></tr>
<tr><td rowspan="7">D3h</td><td rowspan="7">WVRDN</td><td colspan="8">Bit 15 through Bit 8 holds the 8 bit value of the pulse width ratio (t_1/t_2).for the downstream measurement. Each bit is weighted as follows:</td></tr>
<tr><th>BIT 15</th><th>BIT 14</th><th>BIT 13</th><th>BIT 12</th><th>BIT 11</th><th>BIT 10</th><th>BIT 9</th><th>BIT 8</th></tr>
<tr><td>1</td><td>0.5</td><td>0.25</td><td>0.125</td><td>0.0625</td><td>0.03125</td><td>0.015625</td><td>0.0078125</td></tr>
<tr><td colspan="8">Bit 7 thru bit 0 holds the 8 bit value of the pulse width ratio (t_2/t_{ideal}) where t_{ideal} is equal to half the period of the pulse launch frequency for the downstream measurement. Each bit is weighted as follows:</td></tr>
<tr><th>BIT 7</th><th>BIT 6</th><th>BIT 5</th><th>BIT 4</th><th>BIT 3</th><th>BIT 2</th><th>BIT 1</th><th>BIT 0</th></tr>
<tr><td>1</td><td>0.5</td><td>0.25</td><td>0.125</td><td>0.0625</td><td>0.03125</td><td>0.015625</td><td>0.0078125</td></tr>
<tr><td colspan="8">The maximum value of each of these ratios is 1.9921875.</td></tr>
<tr><td>D4h</td><td>Hit1DNInt</td><td colspan="8">15-bit fixed-point integer value of the first hit in the downstream direction. This integer portion is a binary representation of the number of t_{4MHz} periods that contribute to the time results. The maximum size of the integer is 7FFFh or $(2^{15} - 1) \times t_{4MHz}$.</td></tr>
<tr><td>D5h</td><td>Hit1DNFrac</td><td colspan="8">16-bit fractional value of the first hit in the downstream direction. This fractional portion is a binary representation of one t_{4MHz} period quantized to a 16-bit resolution. The maximum size of the fraction is FFFFh or $(2^{16} - 1)/2^{16} \times t_{4MHz}$.</td></tr>
<tr><td>D6h</td><td>Hit2DNInt</td><td colspan="8">15-bit fixed-point integer value of the second hit in the downstream direction. This integer portion is a binary representation of the number of t_{4MHz} periods that contribute to the time results. The maximum size of the integer is 7FFFh or $(2^{15} - 1) \times t_{4MHz}$.</td></tr>
</table>

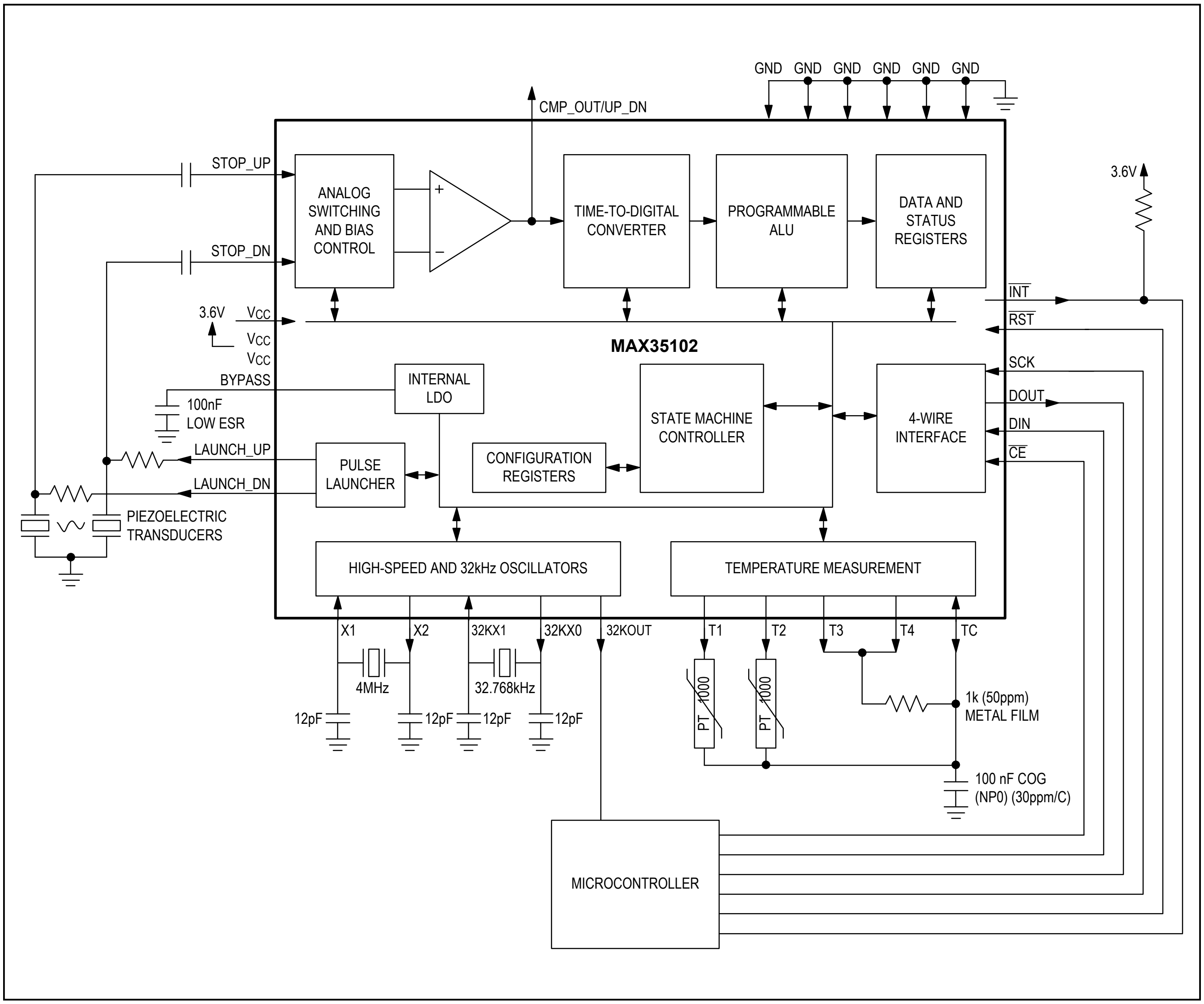
Table 13. Conversion Results Registers Description (continued)

READ ONLY ADDRESS	NAME	DESCRIPTION
D7h	Hit2DNFrac	16-bit fractional value of the second hit in the downstream direction. This fractional portion is a binary representation of one t_{4MHz} period quantized to a 16-bit resolution. The maximum size of the fraction is FFFFh or $(2^{16} - 1)/2^{16} \times t_{4MHz}$.
D8h	Hit3DNInt	15-bit fixed-point integer value of the third hit in the downstream direction. This integer portion is a binary representation of the number of t_{4MHz} periods that contribute to the time results. The maximum size of the integer is 7FFFh or $(2^{15} - 1) \times t_{4MHz}$.
D9h	Hit3DNFrac	16-bit fractional value of the third hit in the downstream direction. This fractional portion is a binary representation of one t_{4MHz} period quantized to a 16-bit resolution. The maximum size of the fraction is FFFFh or $(2^{16} - 1)/2^{16} \times t_{4MHz}$.
E0h	AVGDNInt	15-bit fixed-point integer value of the average of the hit times recorded in the downstream direction. This integer portion is a binary representation of the number of t_{4MHz} periods that contribute to the time results. The maximum size of the integer is 7FFFh or $(2^{15} – 1) \times t_{4MHz}$.
E1h	AVGDNFrac	16-bit fractional value of the average of the hit times recorded in the downstream direction. This fractional portion is a binary representation of one period quantized to a 16-bit resolution. The maximum size of the fraction is FFFFh or $(2^{16} – 1)/2^{16} \times t_{4MHz}$.
E2h	TOF_DIFFInt	16-bit fixed-point two's-complement integer portion of the difference of the averages for the hits recorded in both the upstream and downstream directions. It is computed as: AVGUP – AVGDN This integer represents the number of t_{4MHz} periods that contribute to computation. The maximum size of the integer is 7FFFh or $(2^{15} – 1) \times t_{4MHz}$. The minimum size of this integer is 8000h or $-2^{15} \times t_{4MHz}$.
E3h	TOF_ DIFFFrac	16-bit fractional portion of the two's complement difference of the averages for the hits recorded in both the upstream and downstream directions. This fractional portion is a binary representation of one t_{4MHz} period quantized to a 16-bit resolution. The maximum size of the fraction is FFFFh or $(2^{16} - 1)/2^{16} \times t_{4MHz}$.
E7h	T1Int	15-bit fixed-point integer value of the time taken to discharge the timing capacitor through the RTD connected to the T1 device pin. This integer portion is a binary representation of the number of t_{4MHz} periods that contribute to the time results. The maximum size of the integer is 7FFFh or $(2^{15} - 1) \times t_{4MHz}$.
E8h	T1Frac	16-bit fractional value of the time taken to charge the timing capacitor through the RTD connected to the T1 device pin. This fractional portion is a binary representation of one t_{4MHz} period quantized to a 16-bit resolution. The maximum size of the fraction is FFFFh or $(2^{16} - 1)/2^{16} \times t_{4MHz}$.
E9h	T2Int	15-bit fixed-point integer value of the time taken to charge the timing capacitor through the RTD connected to the T2 device pin. This integer portion is a binary representation of the number of periods that contribute to the time results. The maximum size of the integer is 7FFFh or $(2^{15} - 1) \times t_{4MHz}$.
EAh	T2Frac	16-bit fractional value of the time taken to charge the timing capacitor through the RTD connected to the T2 device pin. This fractional portion is a binary representation of one t_{4MHz} period quantized to a 16-bit resolution. The maximum size of the fraction is FFFFh or $(2^{16} - 1)/2^{16} \times t_{4MHz}$.

Table 19. Conversion Results Registers Description (continued)

READ ONLY ADDRESS	NAME	DESCRIPTION
EBh	T3Int	15-bit fixed-point integer value of the time taken to charge the timing capacitor through the RTD connected to the T3 device pin. This integer portion is a binary representation of the number of t_{4MHz} periods that contribute to the time results. The maximum size of the integer is 7FFFh or $(2^{15} - 1) \times t_{4MHz}$.
ECh	T3Frac	16-bit fractional value of the time taken to charge the timing capacitor through the RTD connected to the T3 device pin. This fractional portion is a binary representation of one t_{4MHz} period quantized to a 16-bit resolution. The maximum size of the fraction is FFFFh or $(2^{16} - 1)/2^{16} \times t_{4MHz}$.
EDh	T4Int	15-bit fixed-point integer value of the time taken to charge the timing capacitor through the RTD connected to the T4 device pin. This integer portion is a binary representation of the number of t_{4MHz} periods that contribute to the time results. The maximum size of the integer is 7FFFh or $(2^{15} - 1) \times t_{4MHz}$.
EEh	T4Frac	16-bit fractional value of the time taken to charge the timing capacitor through the RTD connected to the T4 device pin. This fractional portion is a binary representation of one t_{4MHz} period quantized to a 16-bit resolution. The maximum size of the fraction is FFFFh or $(2^{16} - 1)/2^{16} \times t_{4MHz}$.
F8h	Calibration Int	15-bit fixed-point integer value of the time taken to measure the period of the 32.768kHz crystal oscillator during execution of the calibrate command. This integer portion is a binary representation of the number of t_{4MHz} periods that contribute to the time results. The maximum size of the integer is 7FFFh or $(2^{15} - 1) \times t_{4MHz}$.
F9h	Calibration Frac	16-bit fractional value of the time taken to measure the period of the 32.768kHz crystal oscillator during execution of the calibrate command. This fractional portion is a binary representation of one t_{4MHz} period quantized to a 16-bit resolution. The maximum size of the fraction is FFFFh or $(2^{16} - 1)/2^{16} \times t_{4MHz}$.
FAh		Reserved
FBh		Reserved
FCh		Reserved
FDh		Reserved

Typical Application Circuit



Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX35102ETJ+	-40°C to +85°C	32 TQFN
MAX35102ETJ+T	-40°C to +85°C	32 TQFN

+Denotes a lead(Pb)-free/RoHS-compliant package.

T = Tape and reel.

Chip Information

PROCESS: CMOS

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
32 TQFN	T3244+1C	21-0681	90-0428

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	11/14	Initial release	—

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