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October 2014

# FDMS86201

# N-Channel Shielded Gate PowerTrench<sup>®</sup> MOSFET 120 V, 49 A, 11.5 m $\Omega$

#### **Features**

- Shielded Gate MOSFET Technology
- Max  $r_{DS(on)}$  = 11.5 m $\Omega$  at  $V_{GS}$  = 10 V,  $I_D$  = 11.6 A
- Max  $r_{DS(on)} = 14.5 \text{ m}\Omega$  at  $V_{GS} = 6 \text{ V}$ ,  $I_D = 10.7 \text{ A}$
- Advanced Package and Silicon combination for low r<sub>DS(on)</sub> and high efficiency
- MSL1 robust package design
- 100% UIL tested
- RoHS Compliant



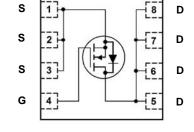
#### **General Description**

This N-Channel MOSFET is produced using Fairchild Semiconductor's advanced PowerTrench® process that incorporates Shielded Gate technology. This process has been optimized for the on-state resistance and yet maintain superior switching performance.

## **Application**

■ DC-DC Conversion





MOSFET Maximum Ratings T<sub>A</sub> = 25 °C unless otherwise noted

Symbol	Parameter			Ratings	Units
V <sub>DS</sub>	Drain to Source Voltage			120	V
V <sub>GS</sub>	Gate to Source Voltage			±20	V
I <sub>D</sub>	Drain Current -Continuous	T <sub>C</sub> = 25 °C		49	
	-Continuous	T <sub>A</sub> = 25 °C	(Note 1a)	11.6	Α
	-Pulsed			160	
E <sub>AS</sub>	Single Pulse Avalanche Energy		(Note 3)	264	mJ
$P_{D}$	Power Dissipation	T <sub>C</sub> = 25 °C		104	W
	Power Dissipation	T <sub>A</sub> = 25 °C	(Note 1a)	2.5	VV
T <sub>J</sub> , T <sub>STG</sub>	Operating and Storage Junction Temperation	ture Range		-55 to +150	°C

#### **Thermal Characteristics**

$R_{\theta JC}$	Thermal Resistance, Junction to Case		1.2	°C/M
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1a)	50	°C/W

#### **Package Marking and Ordering Information**

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDMS86201	FDMS86201	Power 56	13 "	12 mm	3000 units

# **Electrical Characteristics** $T_J = 25$ °C unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Тур	Max	Units
Off Chara	cteristics					
BV <sub>DSS</sub>	Drain to Source Breakdown Voltage	$I_D = 250 \mu A, V_{GS} = 0 V$	120			V
$\frac{\Delta BV_{DS}}{\Delta T_{J}}$	Breakdown Voltage Temperature Coefficient	I <sub>D</sub> = 250 μA, referenced to 25 °C		95		mV/°C
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> = 96 V, V <sub>GS</sub> = 0 V			1	μΑ
$I_{GSS}$	Gate to Source Leakage Current, Forward	$V_{GS} = \pm 20 \text{ V}, V_{DS} = 0 \text{ V}$			100	nA

#### On Characteristics

V <sub>GS(th)</sub>	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}, I_D = 250 \mu A$	2.0	2.6	4.0	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	I <sub>D</sub> = 250 μA, referenced to 25 °C		-10		mV/°C
		V <sub>GS</sub> = 10 V, I <sub>D</sub> = 11.6 A		9.6	11.5	
r <sub>DS(on)</sub>	Static Drain to Source On Resistance	$V_{GS} = 6 \text{ V}, I_D = 10.7 \text{ A}$		11.8	14.5	mΩ
	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 11.6 A, T <sub>J</sub> = 125 °C		15.7	21.5		
9 <sub>FS</sub>	Forward Transconductance	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 11.6 A		39		S

#### **Dynamic Characteristics**

C <sub>iss</sub>	Input Capacitance	V <sub>DS</sub> = 60 V, V <sub>GS</sub> = 0 V, f = 1 MHz	2056	2735	pF
C <sub>oss</sub>	Output Capacitance		322	430	pF
C <sub>rss</sub>	Reverse Transfer Capacitance		15	25	pF
$R_g$	Gate Resistance		1.2		Ω

### **Switching Characteristics**

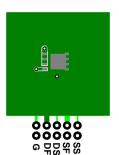
t <sub>d(on)</sub>	Turn-On Delay Time		$V_{DD}$ = 60 V, $I_{D}$ = 11.6 A, $V_{GS}$ = 10 V, $R_{GEN}$ = 6 $\Omega$		13	24	ns
t <sub>r</sub>	Rise Time	V <sub>DD</sub> = 60 V, I <sub>D</sub> = 11.			7.7	16	ns
t <sub>d(off)</sub>	Turn-Off Delay Time	V <sub>GS</sub> = 10 V, R <sub>GEN</sub> =			27	44	ns
t <sub>f</sub>	Fall Time				7.1	15	ns
$Q_g$	Total Gate Charge	V <sub>GS</sub> = 0 V to 10 V			32	46	nC
Qg	Total Gate Charge	$V_{GS} = 0 V to 5 V$			18	26	nC
Q <sub>gs</sub>	Gate to Source Charge		I <sub>D</sub> = 11.6 A		8.1		nC
Q <sub>gd</sub>	Gate to Drain "Miller" Charge				7.1		nC

#### **Drain-Source Diode Characteristics**

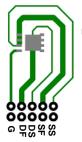
V <sub>SD</sub> Source to Drain Diode Forward Volta	Source to Drain Diade Forward Voltage	$V_{GS} = 0 \text{ V}, I_{S} = 2 \text{ A}$	(Note 2)	0.69	1.2	\/
	Source to Drain blode Forward voltage	$V_{GS} = 0 \text{ V}, I_S = 11.6 \text{ A}$	(Note 2)	0.78	1.3	V
t <sub>rr</sub>	Reverse Recovery Time	1 11 C A di/dt 100 A/	/0	66	106	ns
Q <sub>rr</sub>	Reverse Recovery Charge	I <sub>F</sub> = 11.6 A, di/dt = 100 A/μs		88	140	nC

#### Notes:

<sup>1.</sup> R<sub>6JA</sub> is determined with the device mounted on a 1in<sup>2</sup> pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material. R<sub>6JC</sub> is guaranteed by design while R<sub>6CA</sub> is determined by the user's board design.



a) 50 °C/W when mounted on a 1 in<sup>2</sup> pad of 2 oz copper



b) 125 °C/W when mounted on a minimum pad of 2 oz copper.

<sup>2.</sup> Pulse Test: Pulse Width < 300  $\mu\text{s},$  Duty cycle < 2.0%.

<sup>3.</sup> Starting  $T_J = 25$  °C; N-ch: L = 1 mH,  $I_{AS} = 23$  A,  $V_{DD} = 120$  V,  $V_{GS} = 10$  V. 100% test at L = 0.1 mH,  $I_{AS} = 50$  A.

### Typical Characteristics T<sub>J</sub> = 25 °C unless otherwise noted

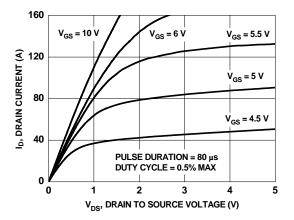


Figure 1. On Region Characteristics

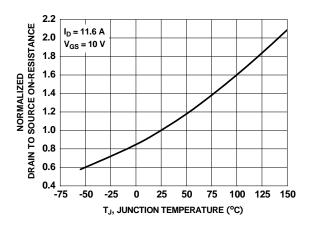


Figure 3. Normalized On Resistance vs Junction Temperature

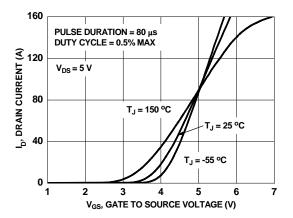


Figure 5. Transfer Characteristics

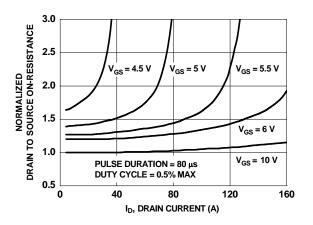


Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

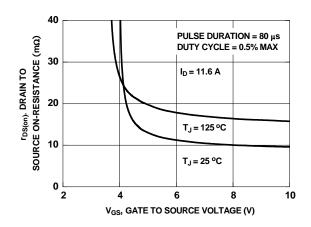


Figure 4. On-Resistance vs Gate to Source Voltage

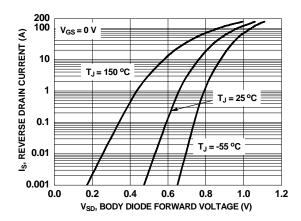


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

## **Typical Characteristics** $T_J = 25$ °C unless otherwise noted

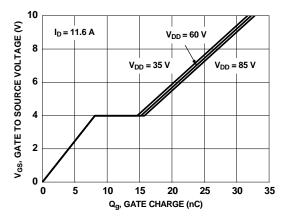


Figure 7. Gate Charge Characteristics

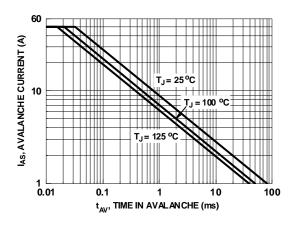


Figure 9. Unclamped Inductive Switching Capability

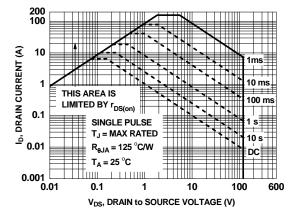


Figure 11. Forward Bias Safe Operating Area

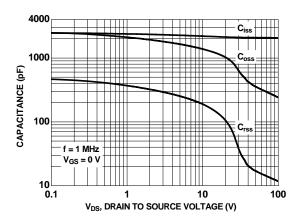


Figure 8. Capacitance vs Drain to Source Voltage

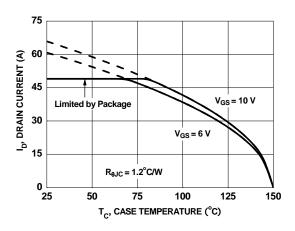


Figure 10. Maximum Continuous Drain Current vs Case Temperature

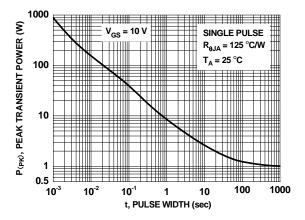


Figure 12. Single Pulse Maximum Power Dissipation

# **Typical Characteristics** $T_J = 25$ °C unless otherwise noted

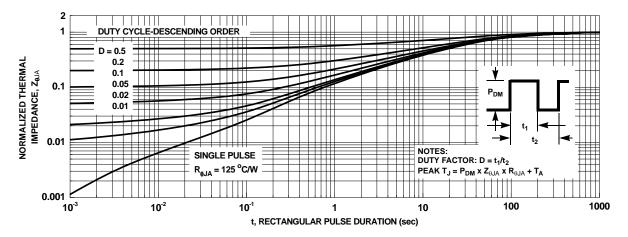


Figure 13. Junction-to-Ambient Transient Thermal Response Curve



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