SL2S1412_SL2S1512_SL2S1612

ICODE ILT-M

Rev. 3.3 — 15 October 2019 Product data sheet
167733 COMPANY PUBLIC

1 General description

The ISO 18000-3 mode 3/EPC Class-1 HF standard allows the commercialized provision of mass adoption of HF RFID technology for passive smart tags and labels. Main fields of applications are supply chain management and logistics for worldwide use.

The ICODE ILT-M is a dedicated chip for passive, intelligent tags and labels supporting the ISO 18000-3 mode 3 RFID standard. It is especially suited for applications where reliable identification and high anti-collision rates are required.

The ICODE ILT-M is a product out of the NXP Semiconductors ICODE product family. The entire ICODE product family offers anti-collision functionality. This allows a reader to simultaneously operate multiple labels/tags within its antenna field. An ICODE ILT-M based label/tag requires no external power supply.

Its contactless interface generates the power supply via the antenna circuit by inductive energy transmission from the interrogator (reader), while the system clock is extracted from the magnetic field. Data transmitted from interrogator to label/tag is demodulated by the interface, and it also modulates the interrogator's magnetic field for data transmission from label/tag to interrogator. A label/tag can be operated without the need for line of sight or battery, as long as it is connected to a dedicated antenna for the targeted frequency range. When the label/tag is within the interrogator's operating range, the high-speed wireless interface allows data transmission in both directions.

2 Features and benefits

2.1 Key features

- 512-bit user memory
- Up to 240-bit of EPC memory
- 96-bit tag identifier (TID) including 48-bit unique serial number
- EAS (Electronic Article Surveillance) functionality
- Recommissioning feature (privacy) with 32-bit kill password
- 32-bit access password to allow a transition into the secured state
- Long read/write ranges due to extremely low-power design
- Reliable operation of multiple tags due to advanced anti-collision (up to 800 tags/s)
- Fast initialization (write EPC)
- Forward link: 25 kbit/s to 100 kbit/s
- Return link: 53 kbit/s to 848 kbit/s

2.2 Key benefits

- High sensitivity provides long read range
- Highly advanced anti-collision resulting in highest identification speed
- Reliable and robust RFID technology suitable noisy environments and dense label populations

2.3 Custom features

- EAS
  Enables the HF RFID tag to be used as EAS tag without the need for a backend data base.

3 Applications

- Healthcare and pharmaceutical supply chain
- Medical lab automation
- Document tracking
- Casino chips
- Laundry automation

4 Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
SL2S1412FUD	Wafer	sawn, bumped wafer, 120 µm, on film frame carrier, C_i between LA and LB = 0 pF (typical)	-
SL2S1412FUF	Wafer	sawn, bumped wafer, 75 µm, on film frame carrier, C_i between LA and LB = 0 pF (typical)	-
SL2S1512FUD	Wafer	sawn, bumped wafer, 120 µm, on film frame carrier, C_i between LA and LB = 23.5 pF (typical)	-
SL2S1512FUF	Wafer	sawn, bumped wafer, 75 µm, on film frame carrier, C_i between LA and LB = 23.5 pF (typical)	-
SL2S1612FUD	Wafer	sawn, bumped wafer, 120 µm, on film frame carrier, C_i between LA and LB = 97 pF (typical)	-
SL2S1512FTB	XSON3	plastic extremely thin small outline package; no leads; 3 terminals; body 1 x 1.45 x 0.5 mm; C_i between LA and LB = 23.5 pF (typical)	SOT1122

5 Block diagram

The SL2S1412; SL2S1512; SL2S1612 IC consists of three major blocks:

- Analog RF Interface
- Digital Controller
- EEPROM

The analog part provides stable supply voltage and demodulates data received from the reader for being processed by the digital part. Further, the modulation transistor of the analog part transmits data back to the reader.

The digital section includes the state machines, processes the protocol and handles communication with the EEPROM, which contains the EPC and the user data.

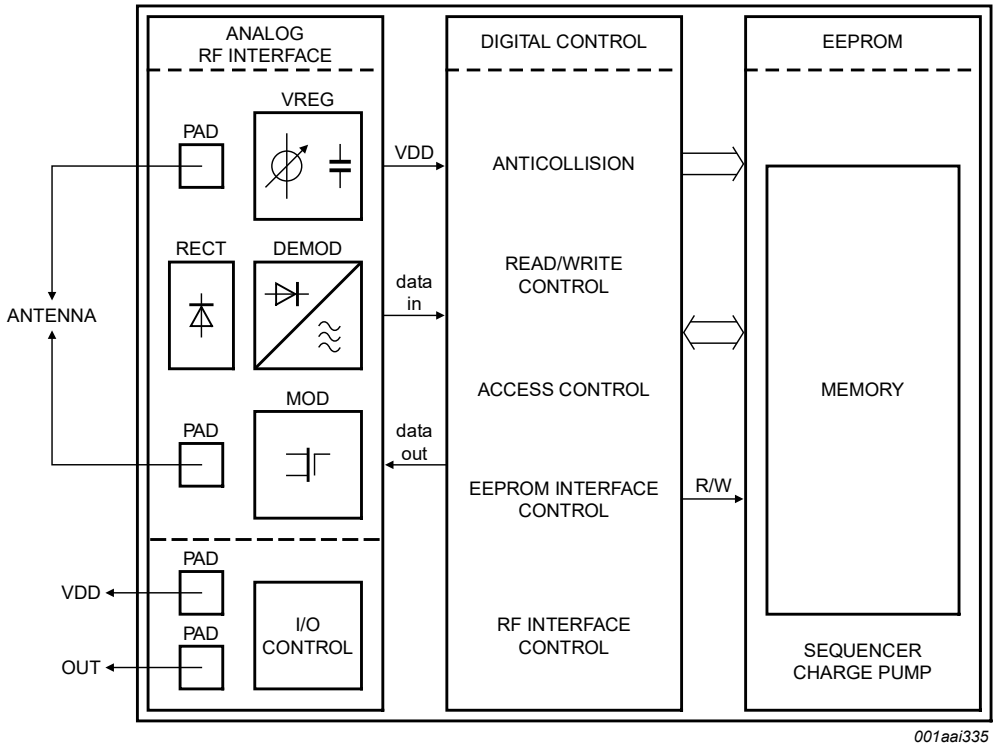
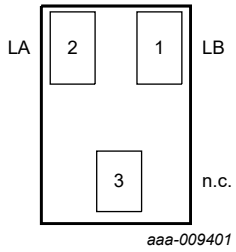


Figure 1. Block diagram

6 Pinning information



Transparent top view

Figure 2. Pin configuration for SOT1122

Table 2. Pin description SOT1122

Pin	Symbol	Description
1	LB	antenna RF input
2	LA	antenna RF input
3	n.c.	not connected

7 Wafer layout

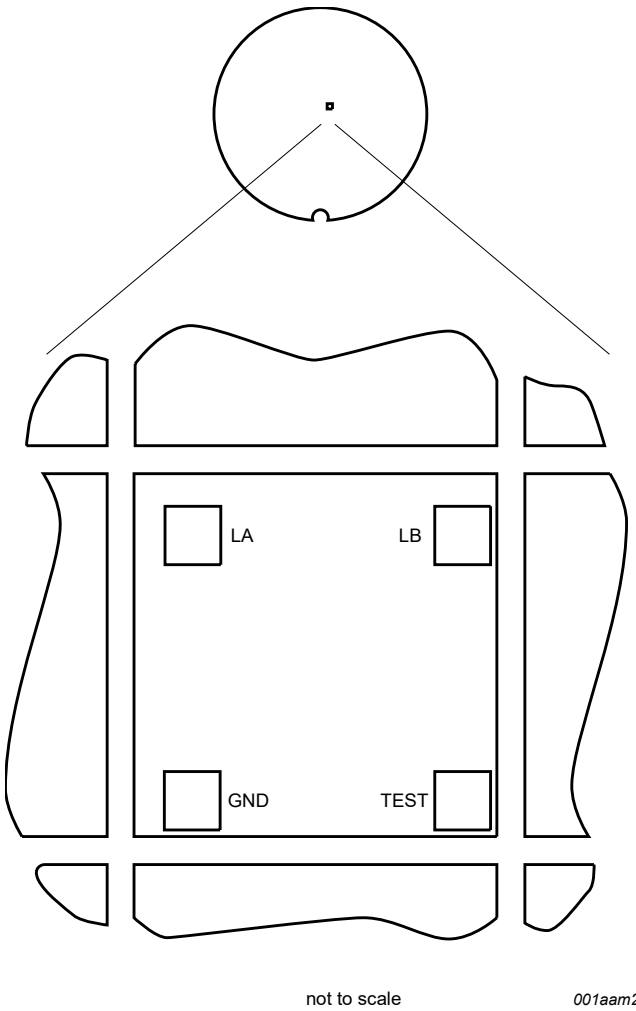


Figure 3. Wafer SL2S1412FUx and SL2S1512FUx layout and pin configuration for the bare die

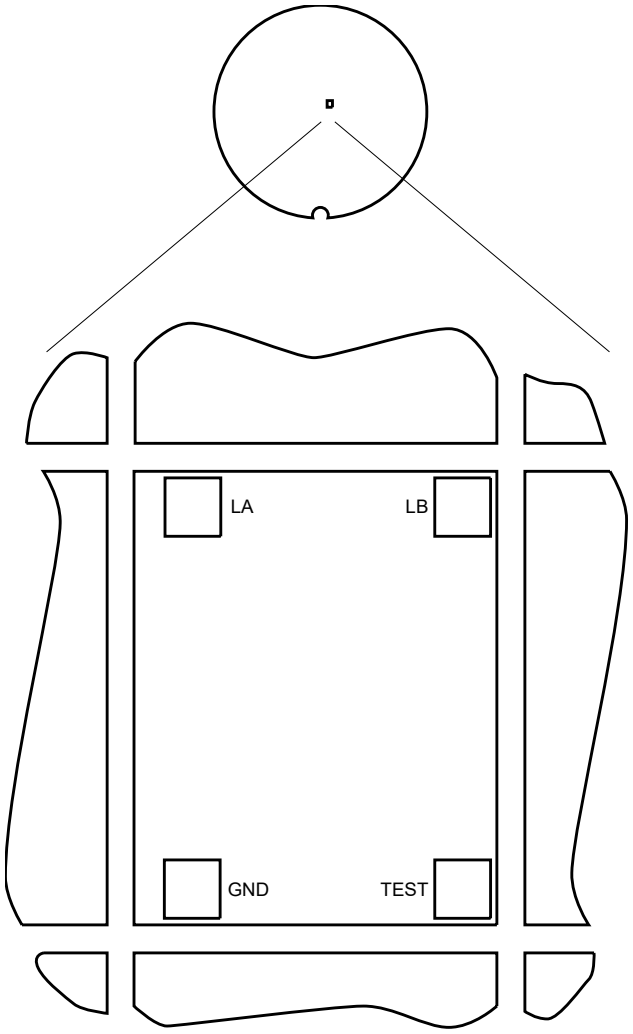


Figure 4. Wafer SL2S1612FUD layout and pin configuration for the bare die

Table 3. Bonding pad description

Symbol	Description
LA	antenna RF input
LB	antenna RF input
GND	ground
TEST	test input

8 Mechanical specification

8.1 Wafer specification

See Ref. 13 "General specification for 8" wafer on UV-tape with electronic fail die marking".

Table 4. Wafer specification

Wafer	
Designation	each wafer is inscribed with batch number and wafer number
Diameter	200 mm (8 inches)
Thickness	
SL2S1412FUD/ SL2S1512FUD/ SL2S1612FUD	120 µm ± 15 µm
SL2S1412FUF/SL2S1512FUF	75 µm ± 15 µm
Process	CMOS 0.14 µm
Batch size	25 wafers
Dies per wafer	
SL2S1412FUx/SL2S1512FUx	110050
SL2S1612FUD	88225
Wafer backside	
Material	Si
Treatment	ground and stress release
Roughness	R_a minimum = 0.5 µm
	R_t maximum = 5 µm
Chip dimensions	
Die size without scribe	
SL2S1412FUx/SL2S1512FUx	520 µm × 484 µm = 251680 $µm^2$
SL2S1612FUD	520 µm × 607 µm = 315640 $µm^2$
Scribe line width	
X-dimension	15 µm (scribe line width measured between nitride edges)
Y-dimension	15 µm (scribe line width measured between nitride edges)
Number of pads	4
Pad location	non-diagonal/placed in chip corners
Distance pad to pad LA to LB	400 µm
Distance pad to pad LB to TEST	
SL2S1412FUx/SL2S1512FUx	360 µm
SL2S1612FUD	517 µm
Passivation on front	

Type	sandwich structure
Material	PE-nitride (on top)
Thickness	1.75 µm total thickness of passivation
Au bump	
Material	>99.9 % pure Au
Hardness	35 HV to 80 HV 0.005
Shear strength	>70 MPa
Height	18 µm
Height uniformity	
within a die	±2 µm
within a wafer	±3 µm
wafer to wafer	±4 µm
Bump flatness	±1.5 µm
Bump size	
LA, LB	60 µm × 60 µm
TEST, GND	60 µm × 60 µm
variation	±5 µm
Under bump metallization	sputtered TiW

8.1.1 Fail die identification

No inkdots are applied to the wafer.

Electronic wafer mapping (SECS II format) covers the electrical test results and additionally the results of mechanical/visual inspection.

See Ref. 13 "General specification for 8" wafer on UV-tape with electronic fail die marking"

8.1.2 Map file distribution

See Ref. 13 "General specification for 8" wafer on UV-tape with electronic fail die marking".

9 Functional description

9.1 Power transfer

Whenever connected to a very simple and cheap type of antenna (as a result of the 13.56 MHz carrier frequency) made out of a few windings printed, winded, etched or punched coil the ICODE ILT-M IC can be operated without line of sight up to a distance of 1.5 m (gate width). No battery is needed.

9.2 Data transfer

9.2.1 Reader to tag Link

An interrogator transmits information to the ICODE ILT-M by modulating an RF signal in the 13.56 MHz frequency. The ICODE ILT-M receives both information and operating energy from this RF signal. Tags are passive, meaning that they receive all of their operating energy from the interrogator's RF waveform.

An interrogator is using a fixed modulation and data rate for the duration of at least an inventory round. It communicates to the ICODE ILT-M by modulating an RF carrier using DSB-ASK with PIE encoding.

For further details refer to Section 18, Ref. 2. Interrogator-to-tag (R=>T) communications.

9.2.2 Tag to reader Link

An interrogator receives information from the ICODE ILT-M by transmitting a continuous-wave RF signal to the tag; the ICODE ILT-M responds by load modulation of the 13.56 MHz carrier frequency, thereby generating modulated sidebands used to transmit an information signal to the interrogator. The system is a reader talks first (RTF) system, meaning that a ICODE ILT-M only responds with an information signal after being directed by the interrogator.

ICODE ILT-M transmits information using ASK modulation. The returned data are either coded with FM0 baseband, Miller with sub carrier or Manchester with sub carrier. The interrogator can select if the ICODE ILT-M shall respond with a sub carrier frequency of 424 kHz or 848 kHz.

For further details refer to Section 18, Ref. 2. tag-to-interrogator (T=>R) communications.

9.3 Air interface standards

The ICODE ILT-M fully supports all parts of the ISO 18000-3 Mode 3 (refer to Section 18, Ref. 1) and the "EPC™ Radio-Frequency Identity Protocols EPC Class-1 HF RFID Air Interface Protocol for Communications at 13.56 MHz, Version 2.0.3" (refer to Section 18, Ref. 2).

10 Memory configuration

This section contains all information including commands by which a reader selects, inventories, and accesses a ICODE ILT-M population

An interrogator manages ICODE ILT-M equipped tag populations using three basic operations. Each of these operations comprises one or more commands. The operations are defined as follows

Select: The process by which an interrogator selects a tag population for inventory and access. Interrogators may use one or more Select commands to select a particular tag population prior to inventory.

Inventory: The process by which an interrogator identifies ICODE ILT-M equipped tags. An interrogator begins an inventory round by transmitting a BeginRound command in one of two sessions. One or more tags may reply. The interrogator detects a single tag reply and requests the PC, EPC, and CRC-16 from the chip. An inventory round operates in one and only one session at a time. For an example of an interrogator inventorying and accessing a single tag refer to Section 18, Ref. 2.

Access: The process by which an interrogator transacts with (reads from or writes to) individual tags. An individual tag must be uniquely identified prior to access. Access comprises multiple commands, some of which employ one-time-pad based cover-coding of the R=>T link.

10.1 Memory

For the general memory layout according to the standard Section 18, Ref. 2. The tag memory is logically subdivided into four distinct banks.

In accordance to the standard Section 18, Ref. 2. The tag memory of the ICODE ILT-M is organized in following 4 memory sections:

Table 5. Memory sections

Name	Size	Bank
Reserved memory (32-bit ACCESS and 32-bit KILL password)	64 bit	00b
EPC (excluding 16 bit CRC-16 and 16-bit PC)	240 bit	01b
TID (including unique 48 bit serial number)	96 bit	10b
User memory	512 bit	11b

The logical address of all memory banks begin at zero (00h).

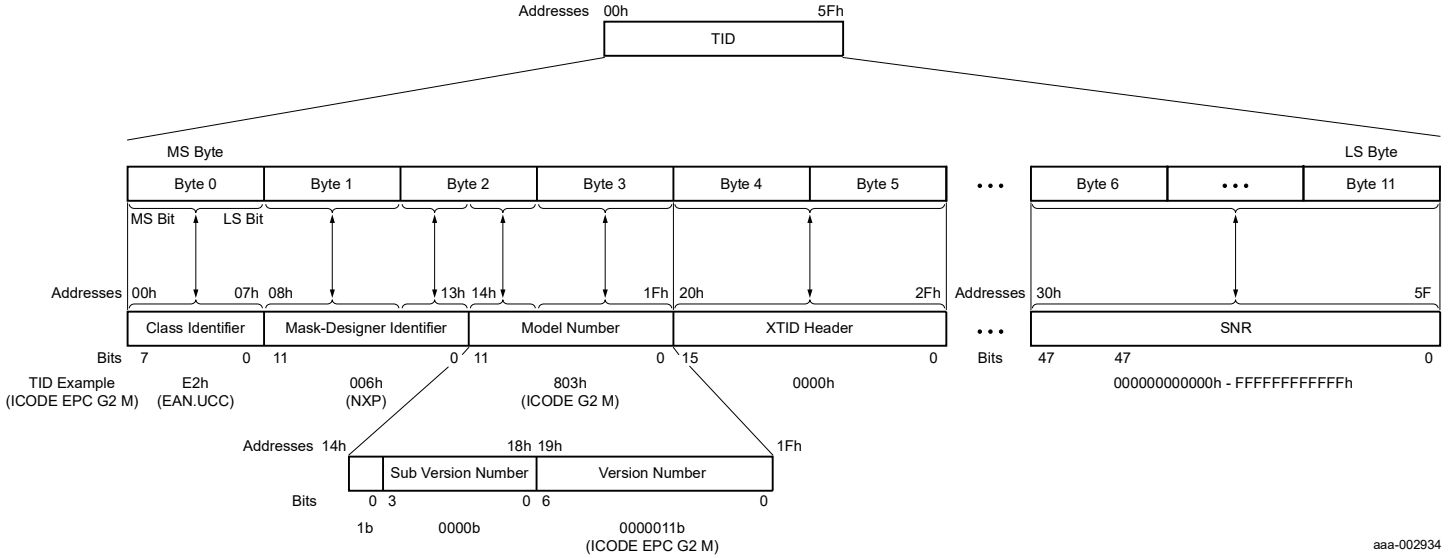


Figure 5. TID for ICODE ILT-M

Table 6. Model number

	SI (Status Indicator Bit)	Sub Version No.	Version (Silicon) No.
ICODE ILT-M	1	0000b	0000011b

10.1.1 Memory map

Table 7. Memory map

Bank address	Memory address	Type	Content	Initial [1]	Remark
Bank 00	00h – 1Fh	Reserved	kill password: refer to Section 18, Ref. 2	all 00h	unlocked memory
	20h – 3Fh	Reserved	access password: refer to Section 18, Ref. 2	all 00h	unlocked memory
Bank 01	00h – 0Fh	EPC	CRC-16: refer to Section 18, Ref. 2		memory mapped calculated CRC
	10h – 14h	EPC	Backscatter length: refer to Section 18, Ref. 2	00110b	unlocked memory
	15h	EPC	UMI refer to Section 18, Ref. 2	0b	unlocked memory
	16h	EPC	XI: refer to Section 18, Ref. 2	0b	calculated
	17h –1Fh	EPC	Numbering system indicator: refer to Section 18, Ref. 2	00h	unlocked memory
	20h - 10Fh	EPC	EPC: refer to Section 18, Ref. 2		unlocked memory
	110h - 1FFh	EPC	RFU	0000h	factory locked memory
	200h - 20Fh	EPC	ConfigWord	0000h	unlocked memory
	210h - 21Fh	EPC	XPC_W1	0000h	factory locked memory
Bank 10	00h – 07h	TID	allocation class identifier: refer to Section 18, Ref. 2	1110 0010b	factory locked memory
	08h – 13h	TID	tag mask designer identifier: refer to Section 18, Ref. 2	0000 0000 0110b	factory locked memory
	14h – 1Fh	TID	tag model number: refer to Section 18, Ref. 2	TMNR	factory locked memory
	20h – 2Fh	TID	Extended TID header refer to [Section 18, Ref. 3	XTID Header	locked memory
	30h – 5Fh	TID	serial number: refer to [Section 18, Ref. 2	SNR	locked memory
Bank 11	00h – 1FFh	User	user memory: refer to [Section 18, Ref. 2	undefined	unlocked memory

[1] This is the initial memory content when delivered by NXP Semiconductors

10.1.1.1 User memory

The User Memory bank contains a sequential block of 512 bits (32 words of 16 bit) ranging from address 00h to 1Fh. The user memory can be accessed via Select, Read

or Write command and it may be write locked, permanently write locked, unlocked, permanently unlocked or block permalocked.

10.1.1.2 Supported EPC types

The EPC types are defined in the EPC Tag Standards document from EPCglobal.

These standards define completely that portion of EPC tag data that is standardized, including how that data is encoded on the EPC tag itself (i.e. the EPC Tag Encodings), as well as how it is encoded for use in the information systems layers of the EPC Systems Network (i.e. the EPC URI or Uniform Resource Identifier Encodings).

The EPC Tag Encodings include a Header field followed by one or more Value Fields. The Header field indicates the length of the Values Fields and contains a numbering system identifier (NSI). The Value Fields contain a unique EPC Identifier and optional Filter Value when the latter is judged to be important to encode on the tag itself.

11 Interrogator commands and tag replies

For a detailed description refer to Section 18, Ref. 2.

11.1 Commands

An overview of interrogator to tag commands is located in Section 18, Ref. 2.

Note that all mandatory commands are implemented on the ICODE ILT-M according to the standard. Additionally the optional command Access is supported by the ICODE ILT-M (for details refer to Section 11.5 "Optional Access Command"). Besides also custom commands are implemented on the ICODE ILT-M (for details refer to Section 11.7 "Custom Commands".

11.2 Mandatory Select Commands

Select commands select a particular ICODE ILT-M tag population based on user-defined criteria.

11.2.1 Select

For a detailed description of the mandatory Select command refer to Section 18, Ref. 2.

11.3 Mandatory Inventory Commands

Inventory commands are used to run the collision arbitration protocol.

11.3.1 BeginRound

For a detailed description of the mandatory BeginRound command refer to Section 18, Ref. 2.

11.3.2 AdjustRound

For a detailed description of the mandatory AdjustRound command refer to Section 18, Ref. 2.

11.3.3 NextSlot

For a detailed description of the mandatory NextSlot command refer to Section 18, Ref. 2.

11.3.4 ACK

For a detailed description of the mandatory ACK command refer to Section 18, Ref. 2.

11.3.5 NAK

For a detailed description of the mandatory NAK command refer to Section 18, Ref. 2.

11.4 Mandatory Access Commands

Access commands are used to read or write data from or to the ICODE ILT-M memory. For a detailed description of the mandatory Access command refer to Section 18, Ref. 2.

11.4.1 REQ_RN

Access commands are used to read or write data from or to the ICODE ILT-M memory. For a detailed description of the mandatory Access command refer to Section 18, Ref. 2.

11.4.2 READ

For a detailed description of the mandatory Req_RN command refer to Section 18, Ref. 2.

11.4.3 WRITE

For a detailed description of the mandatory Write command refer to Section 18, Ref. 2.

11.4.4 KILL (RECOMMISSIONING)

Only mandatory asserted Recom bit 3SB is supported.

For a detailed description of the mandatory Kill command refer to Section 18, Ref. 2.

11.4.5 LOCK

For a detailed description of the mandatory Lock command refer to Section 18, Ref. 2.

11.5 Optional Access Command

11.5.1 Access

For a detailed description of the optional Access command refer to Section 18, Ref. 2, section 6.3.2.10.

11.5.2 BlockPermalock

The User Memory bank is defined in 8 blocks of 4 words each block.

Table 8. BlockPermalock

Bank address	Memory address	Word	Type	Content	Initial	Remark
Bank 11	00h - 3Fh	0 to 3	User	UserMemory Block 0	undefined	
	40h - 7Fh	4 to 7	User	UserMemory Block 1	undefined	
	80h - BFh	8 to 11	User	UserMemory Block 2	undefined	
	C0h - FFh	12 to 15	User	UserMemory Block 3	undefined	
	100h - 13Fh	16 to 19	User	UserMemory Block 4	undefined	
	140h - 17Fh	20 to 23	User	UserMemory Block 5	undefined	
	180h - 1BFh	24 to 27	User	UserMemory Block 6	undefined	

Bank address	Memory address	Word	Type	Content	Initial	Remark
	1C0h - 1FFh	28 to 31	User	UserMemory Block 7	undefined	

For a detailed description of the optional BlockPermalock command refer to Section 18, Ref. 2.

11.5.3 BlockWrite

The BlockWrite command supports the writing of up to two data words at once (WordCount = 00h to 02h). For a detailed description of the optional BlockWrite command refer to Section 18, Ref. 2.

11.6 Optional Features

11.6.1 UMI

The UMI (User Memory Indicator bit 15h) of the Protocol-control (PC) word is supported using Method 2 (written by the reader). For a detailed description of the optional UMI bit refer to Section 18, Ref. 2.

11.7 Custom Commands

11.7.1 ChangeConfigWord

The ConfigWord is located in the EPC Memory Bank at the memory address 200h - 20Fh. Dedicated bits in this word control the custom-specific feature EAS. Memory is accessible with Select and Read sequence.

The ChangeConfigWord command allows to read the dedicated bits in open and secured state. Changing these dedicated bits is only possible if the access password is not equal zero and the IC is in the secured state.

Table 9. ConfigWord

Bank address	Memory address	Type	Initial	Remark
Bank 01 (EPC)	200h - 20Eh	RFU	0b	
	20Fh	EAS Alarm bit	0b	

Table 10. ConfigWord details

MSB															LSB
200 hex	201 hex	202 hex	203 hex	204 hex	205 hex	206 hex	207 hex	208 hex	209 hex	20A hex	20B hex	20C hex	20D hex	20E hex	20F hex
RFU	RFU	RFU	RFU	RFU	RFU	RFU	RFU	RFU	RFU	RFU	RFU	RFU	RFU	RFU	EAS alarm bit

Table 11. Command coding

	Command	RFU	Data	RN	CRC-16
No. of bits	16	8	16	16	16
Description	11100000 00000111	0000 0000	Toggle EAS Bit optionally XOR RN16	handle	

After completing a successful ChangeConfigWord command the ICODE ILT-M backscatters the reply within 20 ms shown below comprising a header (a 0-bit), the ConfigWord, the handle, and a CRC-16 calculated over the 0-bit, ConfigWord and handle.

Table 12. ChangeConfigWord command response

	Header	Status bits	RN	CRC-16
No. of bits	1	16	16	16
Description	0	ConfigWord	handle	

If the toggle bits are transmitted with a value of 00h the ICODE ILT-M responds with a successful Change ConfigWord reply (i.e. the ConfigWord) which allows to read the actual ConfigWord content.

If the ICODE ILT-M encounters an error during execution of ChangeConfigWord it backscatters an error code (see Section 18, Ref. 2 for error-code definitions and for the reply format).

Table 13. Command response table

Starting state	Condition	Response	Next state
ready	all	-	ready
arbitrate, reply, acknowledged	all	-	arbitrate
open	valid handle, ConfigWord needs to change	Backscatter unchanged ConfigWord immediately	open
	valid handle, ConfigWord does not need to change	Backscatter ConfigWord immediately	open
secured	valid handle, ConfigWord needs to change	Backscatter modified ConfigWord, when done	secured
	valid handle, ConfigWord does not need to change	Backscatter ConfigWord immediately	secured
	invalid handle	-	secured
killed	all	-	killed

11.8 Custom features

11.8.1 EAS

The ICODE ILT-M offers an EAS feature which can be enabled or disabled with the ChangeConfigWord command by toggling the EAS Alarm bit.

Only tags with the EAS Alarm bit set to 1 will respond to the following command sequence (inventory round) with their EPC:

1. Select command to the EAS Alarm bit with the parameters
   MemBank: 01h (EPC)
   Action: 010b (deassert SL if not matching)
   Pointer: 20Fh
   Mask length: 01h
   Mask: 1b
2. BeginRound
3. ACK

11.8.2 FastInitialWrite

If the memory content where data shall be written is completely 00h the write command will be executed within shorter time. The FastInitialWrite is internally executed for all commands where the memory content is changed (e.g. Write, Lock, BlockWrite, BlockPermalock,...).

12 Limiting values

Table 14. Limiting values (Wafer)[1][2]

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
T_{stg}	storage temperature			-55	+125	°C
P_{tot}	total power dissipation			-	125	mW
T_j	junction temperature			-40	+85	°C
$I_{i(max)}$	maximum input current	LA to LB; peak	[3]	-	±60	mA
I_I	input current	LA to LB; RMS		-	30	mA
V_{ESD}	electrostatic discharge voltage	Human body model	[4] [5]	-	±2	kV

[1] Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any conditions other than those described in the operating conditions and electrical characteristics sections of this specification is not implied.

[2] This product includes circuitry specifically designed for the protection of its internal devices from the damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying greater than the rated maxima.

[3] The voltage between LA and LB is limited by the on-chip voltage limitation circuitry (corresponding to parameter I_I).

[4] For ESD measurement, the IC was mounted in a CDIP8 package.

[5] HBM: ANSI/ESDA/JEDEC JS-001

CAUTION

This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices.

Such precautions are described in the *ANSI/ESD S20.20, IEC/ST 61340-5, JESD625-A* or equivalent standards.

13 Characteristics

13.1 Memory characteristics

Table 15. EEPROM characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{ret}	retention time	$T_{amb} \leq 55$ °C	50	-	-	year
$N_{endu(W)}$	write endurance		100000	-	-	cycle

13.2 Interface characteristics

Table 16. Interface characteristics

Typical ratings are not guaranteed. The values listed are at room temperature.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
f_i	input frequency		[1]	13.553	13.56	13.567	MHz
$V_{i(RMS)min}$	minimum RMS input voltage	operating read/write		1.5	-	1.7	V
$P_{i(min)}$	minimum input power	operating	[2]	-	40	-	µW
C_i	input capacitance	between LA and LB	[3]				
		SL2S1412FUx		-	-	-	pF
		SL2S1512FUx		22.3	23.5	24.7	pF
		SL2S1612FUD		92	97	102	pF

[1] Bandwidth limitation (± 7 kHz) according to ISM band regulations.
[2] Including losses in the resonant capacitor and rectifier.
[3] Measured with an HP4285A LCR meter at 13.56 MHz and 2 V RMS.

14 Marking

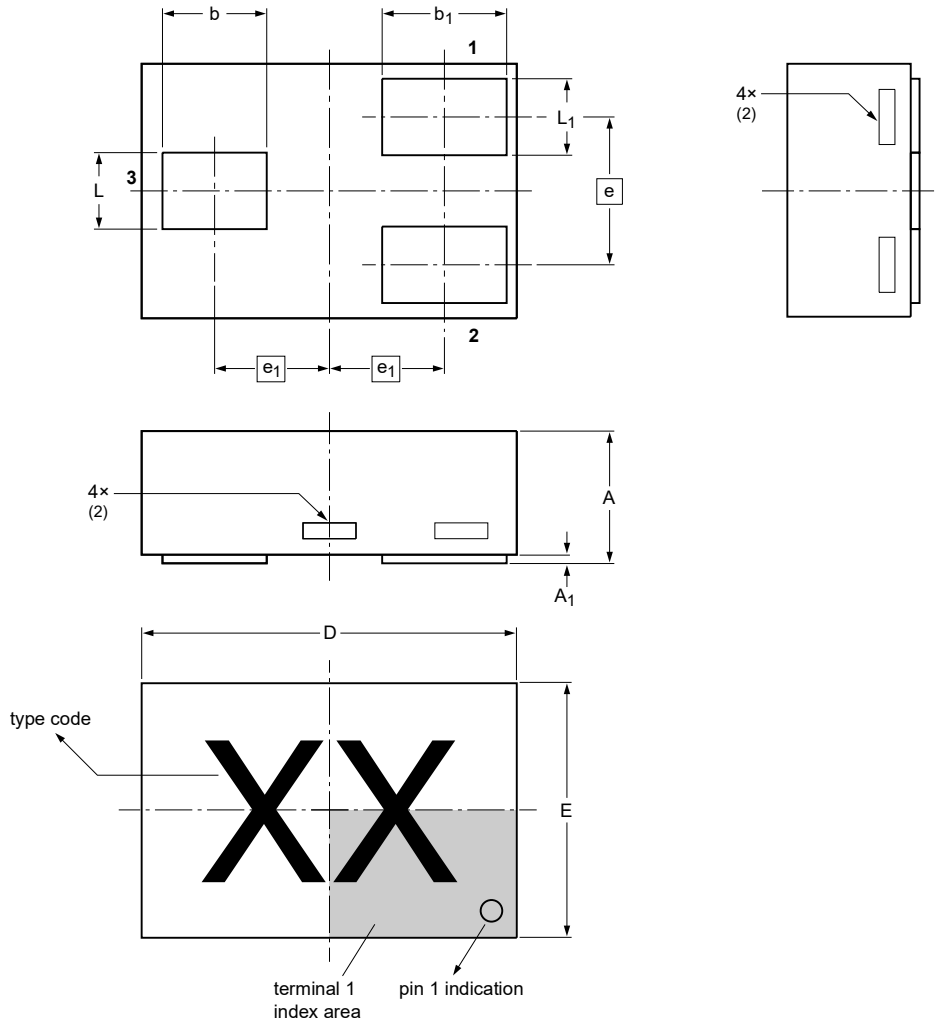
14.1 Marking SOT1122

Table 17. Marking SOT1122

Type number	Marking code
SL2S1512FTB	S1

15 Package outline

XSON3: plastic extremely thin small outline package; no leads; 3 terminals; body 1 x 1.45 x 0.5 mm **SOT1122**



Dimensions

Unit		A(1)	A1	b	b1	D	E	e	e1	L	L1
mm	max	0.50	0.04	0.45	0.55	1.50	1.05			0.35	0.30
	nom			0.40	0.50	1.45	1.00	0.55	0.425	0.30	0.25
	min			0.37	0.47	1.40	0.95			0.27	0.22

Notes

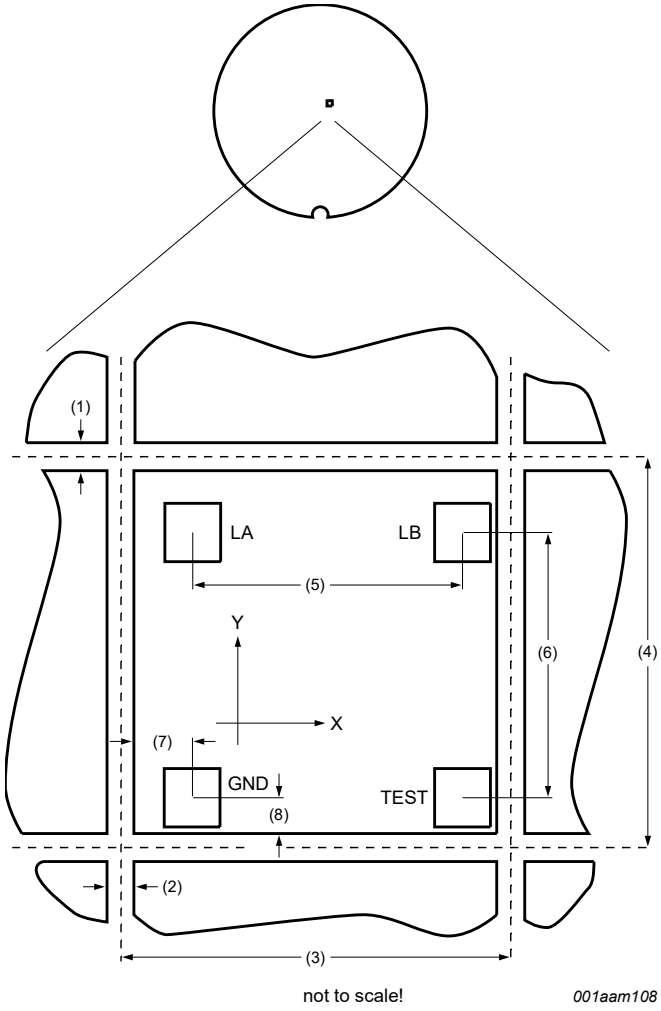
1. Dimension A is including plating thickness.
2. Can be visible in some manufacturing processes.

sot1122_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1122		MO-252				09-10-09

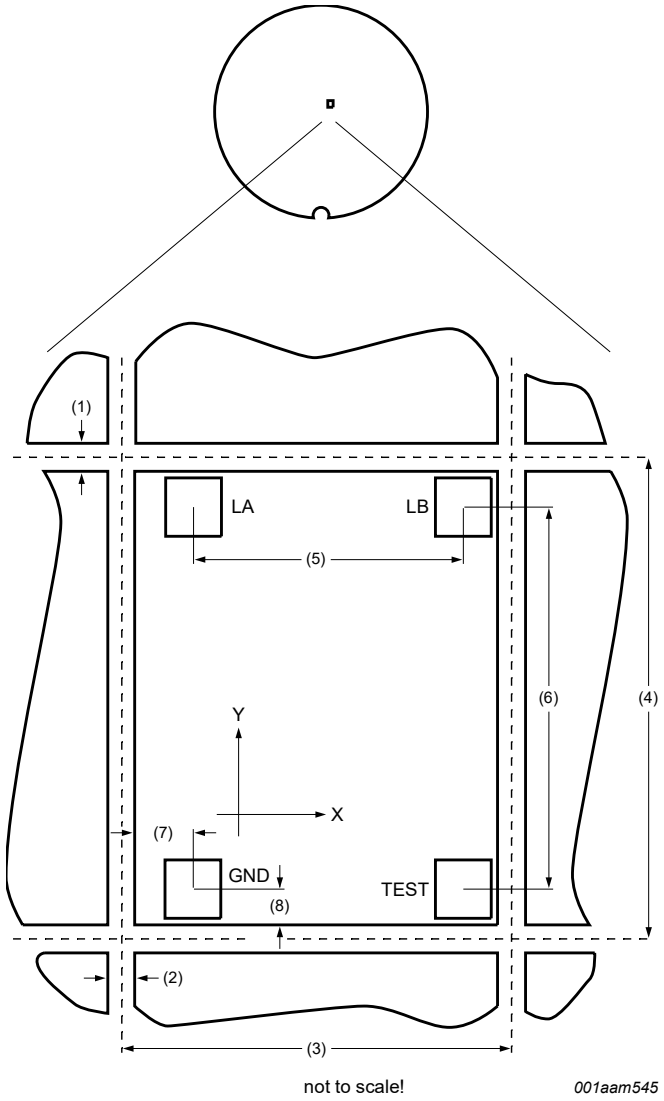
Figure 6. Package outline SOT1122

16 Bare die outline



(1) X-scribe line width: 15 µm
(2) Y-scribe line width: 15 µm
(3) Chip step, X-length: 535 µm
(4) Chip step, Y-length: 499 µm
(5) Bump to bump distance X (LA - LB): 400 µm
(6) Bump to bump distance Y (LB - TEST): 360 µm
(7) Distance bump to nitride edge X: 75 µm
(8) Distance bump to nitride edge Y: 45 µm
Bump size X × Y: 60 µm × 60 µm

Figure 7. Wafer SL2S1412FUx and SL2S1512FUx bare die layout



(1) X-scribe line width: 15 µm
(2) Y-scribe line width: 15 µm
(3) Chip step, X-length: 535 µm
(4) Chip step, Y-length: 622 µm
(5) Bump to bump distance X (LA - LB): 400 µm
(6) Bump to bump distance Y (LB - TEST): 517 µm
(7) Distance bump to nitride edge X: 75 µm
(8) Distance bump to nitride edge Y: 45 µm
Bump size X × Y: 60 µm × 60 µm

Figure 8. Wafer SL2S1612FUD bare die layout

17 Abbreviations

Table 18. Abbreviations

Acronym	Description
CRC	Cyclic redundancy check
CW	Continuous wave
EEPROM	Electrically Erasable Programmable Read Only Memory
EPC	Electronic Product Code (containing Header, Domain Manager, Object Class and Serial Number)
FM0	Bi phase space modulation
IC	Integrated Circuit
LSB	Least Significant Byte/Bit
MSB	Most Significant Byte/Bit
NRZ	Non-Return to Zero coding
RF	Radio Frequency
RTF	Reader Talks First
Tari	Type A Reference Interval (ISO 18000-3 mode 3/EPC Class-1 HF)
HF	High Frequency
XX_b	Value in binary notation
xx_{hex}	Value in hexadecimal notation

18 References

1. ISO 18000-3M3
2. EPC™ Radio-Frequency Identity Protocols EPC Class-1 HF RFID Air Interface Protocol for Communications at 13.56 MHz, Version 2.0.3
3. EPCglobal: EPC Tag Data Standards 1.5
4. ECC ERC Recommendation 70-03 Annex 9
5. ISO/IEC Directives, Part 2: Rules for the structure and drafting of International Standards
6. ISO/IEC 3309: Information technology – Telecommunications and information exchange between systems – High-level data link control (HDLC) procedures – Frame structure
7. ISO/IEC 15961: Information technology, Automatic identification and data capture – Radio frequency identification (RFID) for item management – Data protocol: application interface
8. ISO/IEC 15962: Information technology, Automatic identification and data capture techniques – Radio frequency identification (RFID) for item management – Data protocol: data encoding rules and logical memory functions
9. ISO/IEC 15963: Information technology — Radio frequency identification for item management — Unique identification for RF tags
10. ISO/IEC 18000-1: Information technology — Radio frequency identification for item management — Part 1: Reference architecture and definition of parameters to be standardized
11. ISO/IEC 19762: Information technology AIDC techniques – Harmonized vocabulary – Part 3: radio-frequency identification (RFID)
12. U.S. Code of Federal Regulations (CFR), Title 47, Chapter I, Part 15: Radio-frequency devices, U.S. Federal Communications Commission

[13]

General specification for 8" wafer on UV-tape with electronic fail die marking

Delivery type description – BU-ID document number: 1093**[1].

1 ** ... document version number

19 Revision history

Table 19. Revision history

Document ID	Release date	Data sheet status	Supersedes
SL2S1412_SL2S1512_SL2S1612 v. 3.3	20191015	Product data sheet	SL2S1412_SL2S1512_SL2S1612 v. 3.2
Modifications:	• 75 µ wafer thickness delivery types SL2S1412FUF and SL2S1512FUF in Section 4 "Ordering Information" and Section 8.1 "Wafer specification" added		
SL2S1412_SL2S1512_SL2S1612 v. 3.2	20131008	Product data sheet	SL2S1412_SL2S1512_SL2S1612 v. 3.1
Modifications:	• Type SL2S1512FTB added • Section 14 "Marking" and Section 15 "Package outline": added		
SL2S1412_SL2S1512_SL2S1612 v. 3.1	20130923	Product data sheet	SL2S1412_SL2S1512_SL2S1612 v. 3.0
Modifications:	• Security status into COMPANY PUBLIC		
SL2S1412_SL2S1512_SL2S1612 v. 3.0	20120502	Product data sheet	SL2S1412_SL2S1512_SL2S1612 v. 1.2
Modifications:	• Data sheet status changed into Product data sheet		
SL2S1412_SL2S1512_SL2S1612 v. 1.2	20120328	Objective data sheet	167711
Modifications:	• Type SL2S1612 added • Section 4 "Ordering information": updated		
167711	20110316	Objective data sheet	167710
Modifications:	• Update to final version of ISO 18000-3M3		
167710		Objective data sheet	-

20 Legal information

20.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
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105318, г.Москва, ул.Щербаковская д.3, офис 1107, 1118, ДЦ «Щербаковский»

Телефон: +7 495 668-12-70 (многоканальный)

Факс: +7 495 668-12-70 (доб.304)

E-mail: info@moschip.ru

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moschip.ru
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