

N-Channel Power MOSFET

600V, 4A, 0.9Ω

FEATURES

- Super-Junction technology
- High performance due to small figure-of-merit
- High ruggedness performance
- High commutation performance
- 100% UIL tested
- Pb-free plating
- Compliant to RoHS Directive 2011/65/EU and in accordance to WEEE 2002/96/EC
- Halogen-free according to IEC 61249-2-21

KEY PERFORMANCE PARAMETERS

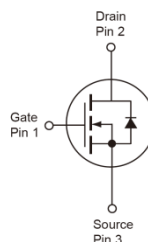
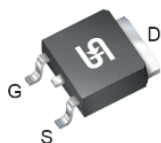
PARAMETER	VALUE	UNIT
V_{DS}	600	V
$R_{DS(on)}$ (max)	0.9	Ω
Q_g	9.6	nC

APPLICATIONS

- Power Supply
- Lighting



TO-252 (DPAK)



Note: MSL 3 (Moisture Sensitivity Level) per J-STD-020

ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ unless otherwise noted)

PARAMETER					SYMBOL	LIMIT	UNIT
Drain-Source Voltage					V_{DS}	600	V
Gate-Source Voltage					V_{GS}	± 30	V
Continuous Drain Current ^(Note 1)			T _C = 25°C		I _D	4	A
			T _C = 100°C			2.4	A
Pulsed Drain Current ^(Note 2)					I _{DM}	12	A
Total Power Dissipation @ T _C = 25°C					P _{DTOT}	36.8	W
Single Pulsed Avalanche Energy ^(Note 3)					E _{AS}	42.3	mJ
Single Pulsed Avalanche Current ^(Note 3)					I _{AS}	1.3	A
Operating Junction and Storage Temperature Range					T _J , T _{STG}	- 55 to +150	°C

THERMAL PERFORMANCE

PARAMETER	SYMBOL	LIMIT	UNIT
Junction to Case Thermal Resistance	$R_{\theta JC}$	3.4	°C/W
Junction to Ambient Thermal Resistance	$R_{\theta JA}$	62	°C/W

Thermal Performance Note: $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistances. The case-thermal reference is defined at the solder mounting surface of the drain pins. $R_{\theta JA}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design. $R_{\theta JA}$ shown below for single device operation on FR-4 PCB in still air.

ELECTRICAL SPECIFICATIONS (T _A = 25°C unless otherwise noted)						
PARAMETER	CONDITIONS	SYMBOL	MIN	TYP	MAX	UNIT
Static						
Drain-Source Breakdown Voltage	V _{GS} = 0V, I _D = 250μA	BV _{DSS}	600	--	--	V
Gate Threshold Voltage	V _{DS} = V _{GS} , I _D = 250μA	V _{GS(TH)}	2	3.3	4	V
Gate Body Leakage	V _{GS} = ±30V, V _{DS} = 0V	I _{GSS}	--	--	±100	nA
Zero Gate Voltage Drain Current	V _{DS} = 600V, V _{GS} = 0V	I _{DSS}	--	--	1	μA
Drain-Source On-State Resistance (Note 4)	V _{GS} = 10V, I _D = 1.2A	R _{DS(on)}	--	0.69	0.9	Ω
Dynamic (Note 5)						
Total Gate Charge	V _{DS} = 380V, I _D = 4A, V _{GS} = 10V	Q _g	--	9.6	--	nC
Gate-Source Charge		Q _{gs}	--	2.0	--	
Gate-Drain Charge		Q _{gd}	--	4.5	--	
Input Capacitance	V _{DS} = 100V, V _{GS} = 0V, f = 1.0MHz	C _{iss}	--	315	--	pF
Output Capacitance		C _{oss}	--	46.4	--	
Gate Resistance	F = 1MHz, open drain	R _g	--	3.2	--	Ω
Switching (Note 6)						
Turn-On Delay Time	V _{DD} = 380V, R _{GEN} = 25Ω, I _D = 4A, V _{GS} = 10V,	t _{d(on)}	--	18	--	ns
Turn-On Rise Time		t _r	--	10	--	
Turn-Off Delay Time		t _{d(off)}	--	36.4	--	
Turn-Off Fall Time		t _f	--	8	--	
Source-Drain Diode						
Forward Voltage (Note 4)	I _S = 4A, V _{GS} = 0V	V _{SD}	--	--	1.4	V
Reverse Recovery Time	V _R = 100V, I _S = 4A dI _F /dt = 100A/μs	t _{rr}	--	185.5	--	ns
Reverse Recovery Charge		Q _{rr}	--	1.38	--	μC

Notes:

1. Current limited by package.
2. Pulse width limited by the maximum junction temperature.
3. $L = 50mH, I_{AS} = 1.3A, V_{DD} = 50V, R_G = 25\Omega$, Starting $T_J = 25^\circ\text{C}$
4. Pulse test: $PW \leq 300\mu s$, duty cycle $\leq 2\%$.
5. For DESIGN AID ONLY, not subject to production testing.
6. Switching time is essentially independent of operating temperature.

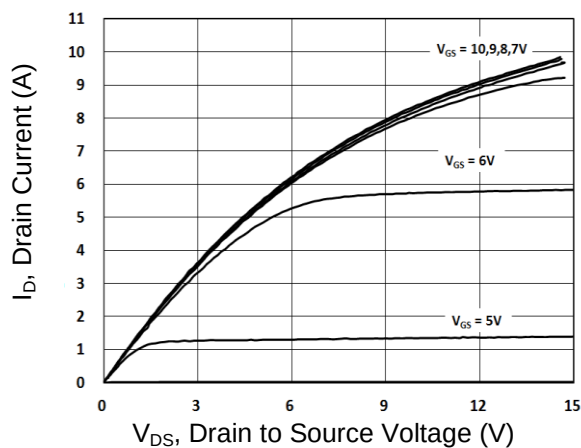
ORDERING INFORMATION

PART NO.	PACKAGE	PACKING
TSM60NB900CP ROG	TO-252 (DPAK)	2,500pcs / 13" Reel

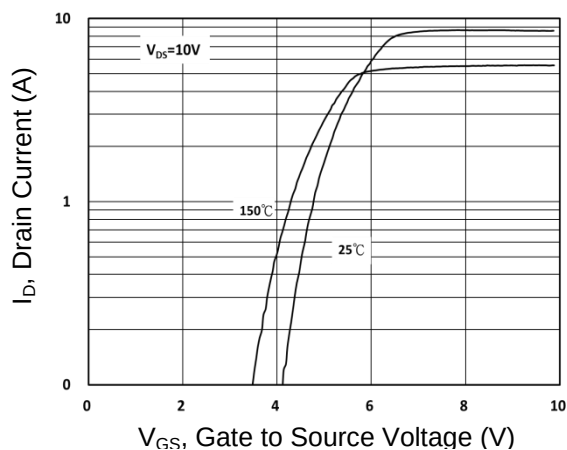
CHARACTERISTICS CURVES

($T_c = 25^\circ\text{C}$ unless otherwise noted)

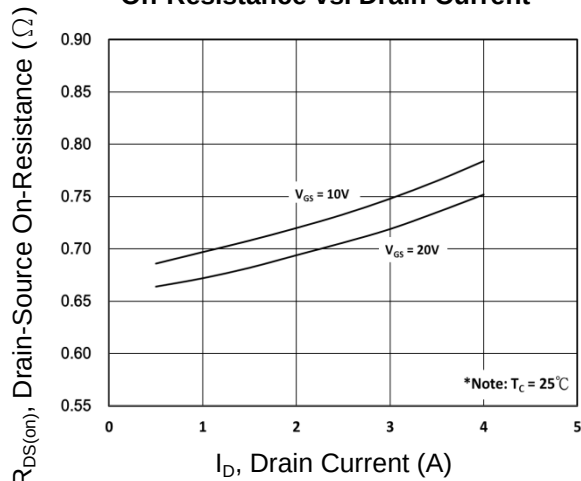
Output Characteristics



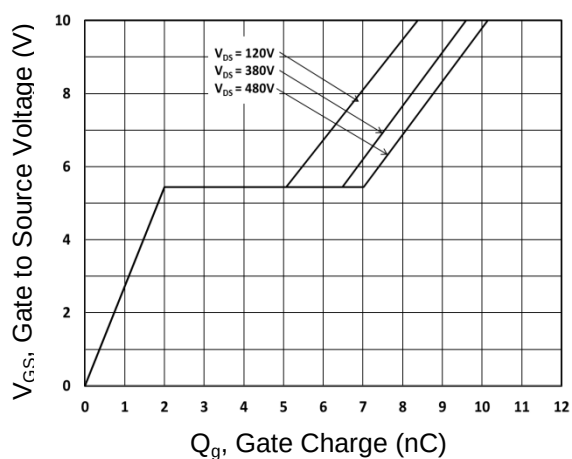
Transfer Characteristics



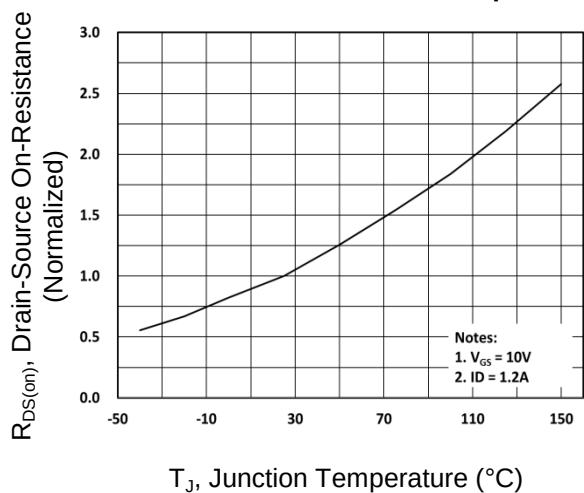
On-Resistance vs. Drain Current



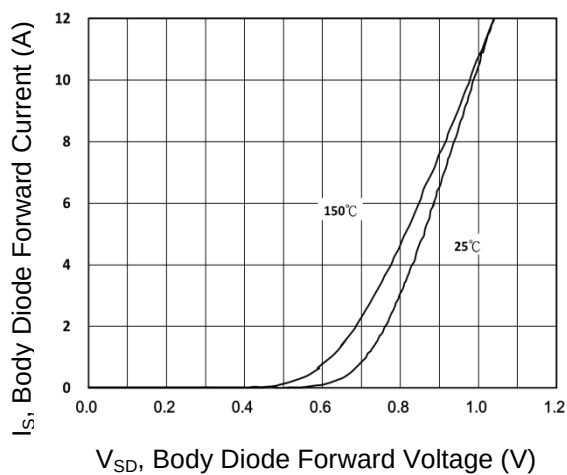
Gate-Source Voltage vs. Gate Charge



On-Resistance vs. Junction Temperature



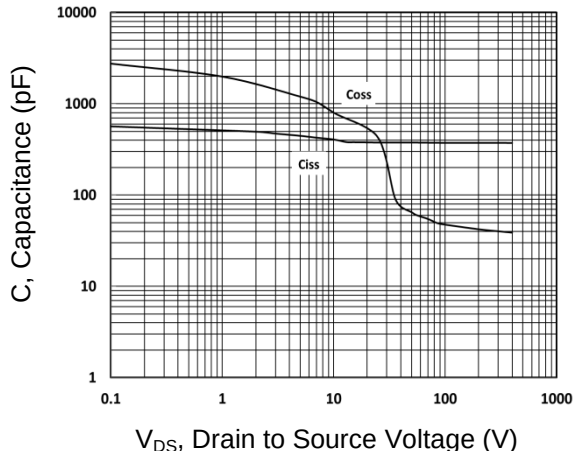
Source-Drain Diode Forward Current vs. Voltage



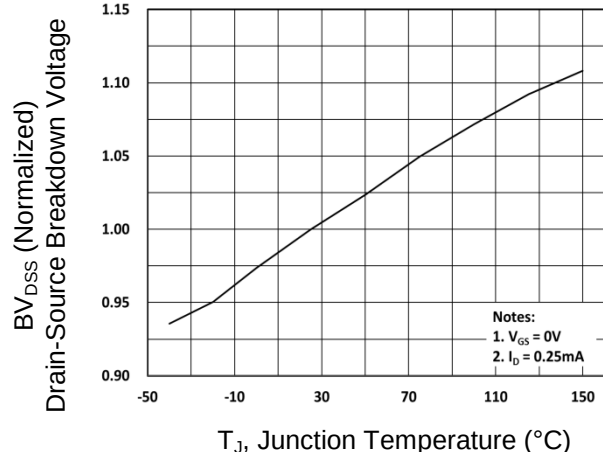
CHARACTERISTICS CURVES

($T_C = 25^\circ\text{C}$ unless otherwise noted)

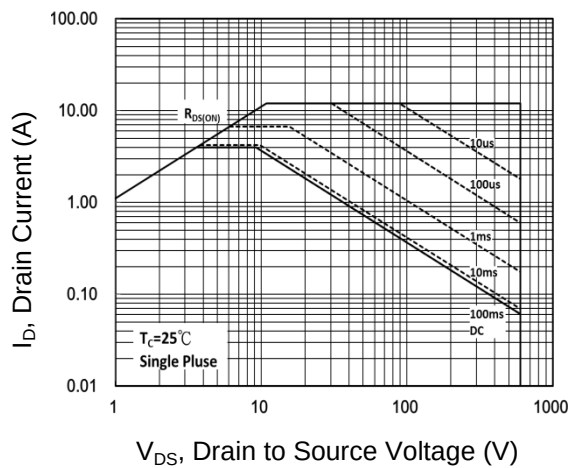
Capacitance vs. Drain-Source Voltage



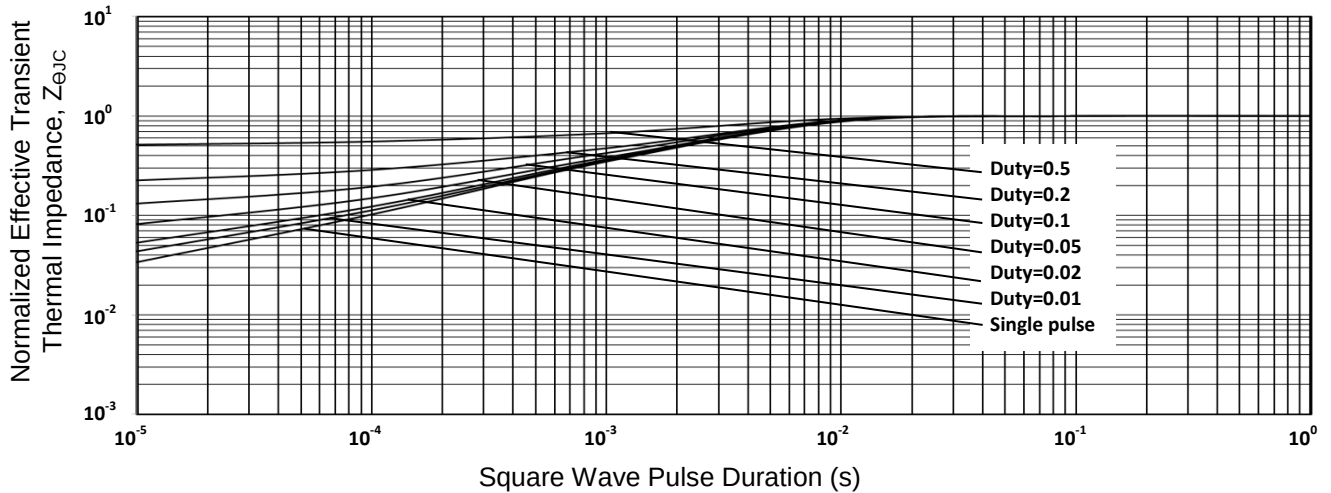
BV_{DSS} vs. Junction Temperature



Maximum Safe Operating Area

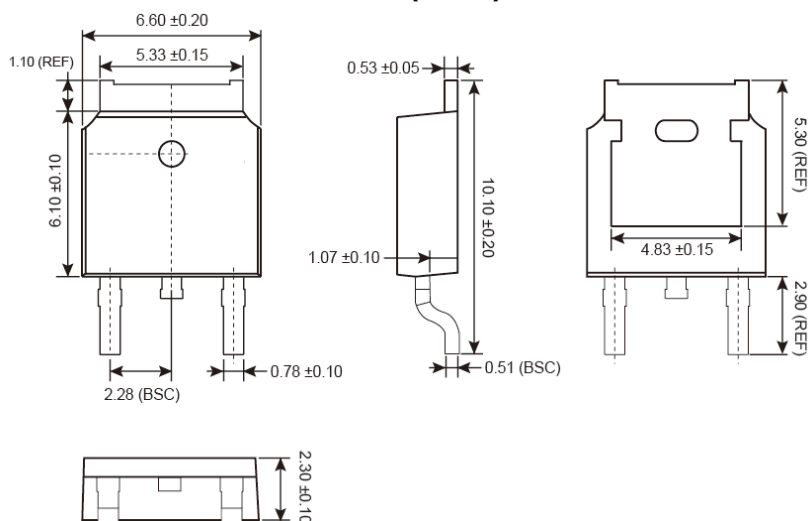


Normalized Thermal Transient Impedance, Junction-to-Case

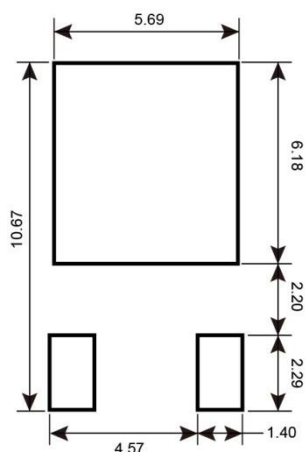


PACKAGE OUTLINE DIMENSIONS (Unit: Millimeters)

TO-252 (DPAK)



SUGGESTED PAD LAYOUT (Unit: Millimeters)



MARKING DIAGRAM



Y = Year Code

M = Month Code for Halogen Free Product

O =Jan **P** =Feb **Q** =Mar **R** =Apr

S =May **T** =Jun **U** =Jul **V** =Aug

W =Sep **X** =Oct **Y** =Nov **Z** =Dec

L = Lot Code (1~9, A~Z)

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