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July 2015

FDMT800100DC

N-Channel Dual CoolTM 88 PowerTrench[®] MOSFET 100 V, 162 A, 2.95 m Ω

Features

- Max $r_{DS(on)}$ = 2.95 m Ω at V_{GS} = 10 V, I_D = 24 A
- Max $r_{DS(on)} = 4.46 \text{ m}\Omega$ at $V_{GS} = 6 \text{ V}$, $I_D = 19 \text{ A}$
- Advanced Package and Silicon combination for low r_{DS(on)} and high efficiency
- Next generation enhanced body diode technology, engineered for soft recovery
- Low profile 8x8mm MLP package
- MSL1 robust package design
- 100% UIL tested
- RoHS Compliant

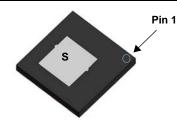


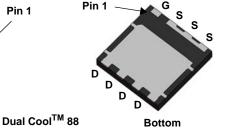
General Description

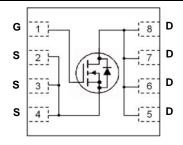
This N-Channel MOSFET is produced using Fairchild Semiconductor's advanced PowerTrench® process. Advancements in both silicon and Dual Cool TM package technologies have been combined to offer the lowest $r_{DS(on)}$ while maintaining excellent switching performance by extremely low Junction-to-Ambient thermal resistance.

Applications

- OringFET / Load Switching
- Synchronous Rectification
- DC-DC Conversion







MOSFET Maximum Ratings T_A = 25 °C unless otherwise noted

Symbol	Parame	eter		Ratings	Units
V_{DS}	Drain to Source Voltage			100	V
V_{GS}	Gate to Source Voltage			±20	V
	Drain Current -Continuous	T _C = 25 °C	(Note 5)	162	
	-Continuous	T _C = 100 °C	(Note 5)	102	^
ID	-Continuous	T _A = 25 °C	(Note 1a)	24	Α
	-Pulsed		(Note 4)	989	
E _{AS}	Single Pulse Avalanche Energy		(Note 3)	1536	mJ
D	Power Dissipation	T _C = 25 °C		156	W
P_{D}	Power Dissipation	T _A = 25 °C	(Note 1a)	3.2	VV
T _J , T _{STG}	Operating and Storage Junction Tempera	ture Range		-55 to +150	°C

Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction to Case	(Top Source)	1.6	
$R_{\theta JC}$	Thermal Resistance, Junction to Case	(Bottom Drain)	0.8	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1a)	38	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1b)	81	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1i)	15	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1j)	21	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1k)	9	

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
800100DC	FDMT800100DC	Dual Cool TM 88	=	13.3 mm	3000 units

Electrical Characteristics $T_J = 25$ °C unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Тур	Max	Units
Off Chara	acteristics					
BV _{DSS}	Drain to Source Breakdown Voltage	$I_D = 250 \mu A, V_{GS} = 0 V$	100			V
$\Delta BV_{DSS} \over \Delta T_J$	Breakdown Voltage Temperature Coefficient	I_D = 250 μ A, referenced to 25 °C		66		mV/°C
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} = 80 V, V _{GS} = 0 V			1	μΑ
I _{GSS}	Gate to Source Leakage Current	$V_{GS} = \pm 20 \text{ V}, V_{DS} = 0 \text{ V}$			100	nA

On Characteristics

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}, I_{D} = 250 \mu A$	2.0	2.8	4.0	V
$\Delta V_{GS(th)} \over \Delta T_J$	Gate to Source Threshold Voltage Temperature Coefficient	I_D = 250 μ A, referenced to 25 °C		-11		mV/°C
		V _{GS} = 10 V, I _D = 24 A		2.3	2.95	
r _{DS(on)}	Static Drain to Source On Resistance	V _{GS} = 6 V, I _D = 19 A		3.5	4.46	mΩ
, ,		$V_{GS} = 10 \text{ V}, I_D = 24 \text{ A}, T_J = 125 \text{ °C}$		4.2	5.39	
9 _{FS}	Forward Transconductance	V _{DS} = 5 V, I _D = 24 A		66		S

Dynamic Characteristics

C _{iss}	Input Capacitance	V 50 V V 0 V		5595	7835	pF
Coss	Output Capacitance	$V_{DS} = 50 \text{ V}, V_{GS} = 0 \text{ V},$ f = 1 MHz		1160	1625	pF
C _{rss}	Reverse Transfer Capacitance	1 - 1 101112		39	75	pF
R _a	Gate Resistance		0.1	1.4	3.5	Ω

Switching Characteristics

t _{d(on)}	Turn-On Delay Time				29	47	ns
t _r	Rise Time	$V_{DD} = 50 \text{ V}, I_{D} = 24$	$V_{DD} = 50 \text{ V}, I_D = 24 \text{ A},$		18	33	ns
t _{d(off)}	Turn-Off Delay Time	$V_{GS} = 10 \text{ V}, R_{GEN}$	= 6 Ω		40	64	ns
t _f	Fall Time				10	20	ns
$Q_{g(TOT)}$	Total Gate Charge	V _{GS} = 0 V to 10 V			79	111	nC
$Q_{g(TOT)}$	Total Gate Charge	$V_{GS} = 0 V to 6 V$	V _{DD} = 50 V,		50	70	nC
Q_{gs}	Gate to Source Charge		I _D = 24 A		23		nC
Q_{gd}	Gate to Drain "Miller" Charge				16		nC

Drain-Source Diode Characteristics

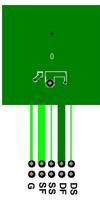
V	Vop I Source to Drain Diode Forward Voltage	$V_{GS} = 0 \text{ V}, I_{S} = 2.9 \text{ A}$	(Note 2)	0.7	1.1	V
V SD		$V_{GS} = 0 V, I_{S} = 24 A$	(Note 2)	0.8	1.2	
t _{rr}	Reverse Recovery Time	$I_{\rm F} = 24 \text{ A}, \text{di/dt} = 100 \text{A/}$	u.c	71	114	ns
Q_{rr}	Reverse Recovery Charge	1F = 24 A, αl/αι = 100 A/μs		94	151	nC

Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction to Case	(Top Source)	1.6	
$R_{\theta JC}$	Thermal Resistance, Junction to Case	(Bottom Drain)	0.8	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1a)	38	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1b)	81	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1c)	26	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1d)	34	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1e)	14	°C // /
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1f)	16	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1g)	26	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1h)	60	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1i)	15	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1j)	21	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1k)	9	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1I)	11	

NOTES:

1. R_{0JA} is determined with the device mounted on a FR-4 board using a specified pad of 2 oz copper as shown below. R_{0CA} is determined by the user's board design.



a. 38 °C/W when mounted on a 1 in² pad of 2 oz copper



b. 81 °C/W when mounted on a minimum pad of 2 oz copper

- c. Still air, 20.9x10.4x12.7mm Aluminum Heat Sink, 1 in² pad of 2 oz copper
- d. Still air, 20.9x10.4x12.7mm Aluminum Heat Sink, minimum pad of 2 oz copper
- e. Still air, 45.2x41.4x11.7mm Aavid Thermalloy Part # 10-L41B-11 Heat Sink, 1 in² pad of 2 oz copper
- f. Still air, 45.2x41.4x11.7mm Aavid Thermalloy Part # 10-L41B-11 Heat Sink, minimum pad of 2 oz copper
- g. 200FPM Airflow, No Heat Sink,1 in² pad of 2 oz copper
- h. 200FPM Airflow, No Heat Sink, minimum pad of 2 oz copper
- i. 200FPM Airflow, 20.9x10.4x12.7mm Aluminum Heat Sink, 1 in 2 pad of 2 oz copper
- j. 200FPM Airflow, 20.9x10.4x12.7mm Aluminum Heat Sink, minimum pad of 2 oz copper
- $k.\ 200 FPM\ Airflow,\ 45.2x41.4x11.7mm\ Aavid\ Thermalloy\ Part\ \#\ 10-L41B-11\ Heat\ Sink,\ 1\ in^2\ pad\ of\ 2\ oz\ copperator of\ 2\ oz\ copperator\ 2$
- $I.\ 200 FPM\ Airflow,\ 45.2 x 41.4 x 11.7 mm\ Aavid\ Thermalloy\ Part\ \#\ 10-L41 B-11\ Heat\ Sink,\ minimum\ pad\ of\ 2\ oz\ copper$
- 2. Pulse Test: Pulse Width < 300 $\mu\text{s},$ Duty cycle < 2.0%.
- 3. E_{AS} of 1536 mJ is based on starting $T_J = 25$ °C; N-ch: L = 3 mH, $I_{AS} = 32$ A, $V_{DD} = 100$ V, $V_{GS} = 10$ V. 100% test at L = 0.1 mH, $I_{AS} = 101$ A.
- 4. Pulsed Id please refer to Fig 11 SOA graph for more details.
- 5. Computed continuous current limited to Max Junction Temperature only, actual continuous current will be limited by thermal & electro-mechanical application board design.

Typical Characteristics T_J = 25 °C unless otherwise noted

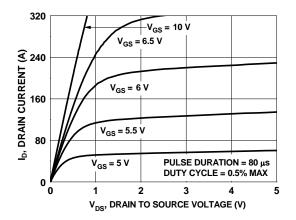


Figure 1. On-Region Characteristics

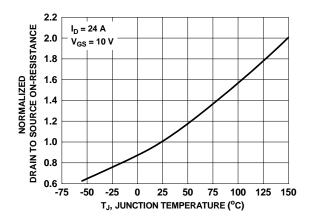


Figure 3. Normalized On-Resistance vs Junction Temperature

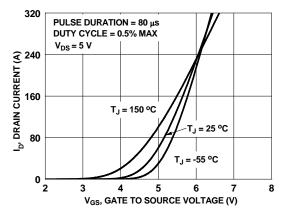


Figure 5. Transfer Characteristics

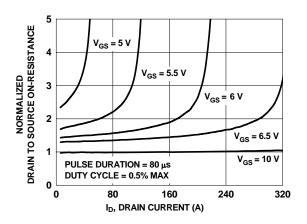


Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

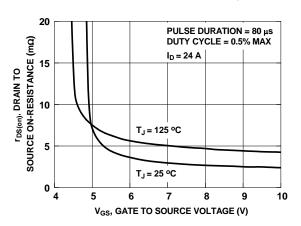


Figure 4. On-Resistance vs Gate to Source Voltage

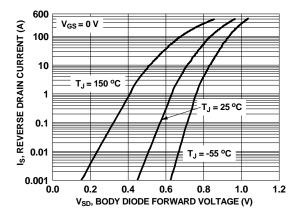


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

Typical Characteristics $T_J = 25$ °C unless otherwise noted

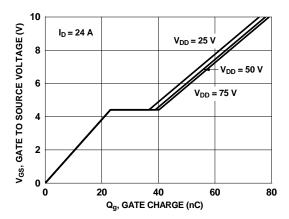


Figure 7. Gate Charge Characteristics

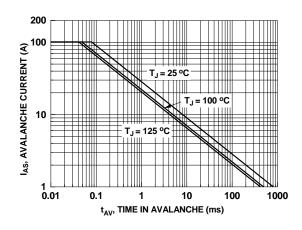


Figure 9. Unclamped Inductive Switching Capability

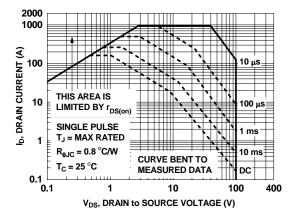


Figure 11. Forward Bias Safe Operating Area

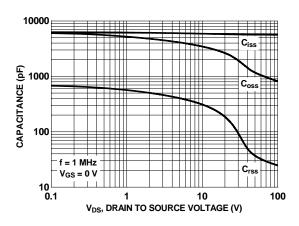


Figure 8. Capacitance vs Drain to Source Voltage

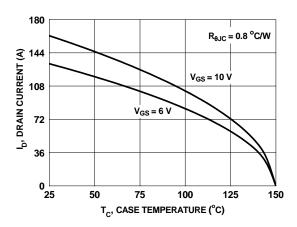


Figure 10. Maximum Continuous Drain Current vs Case Temperature

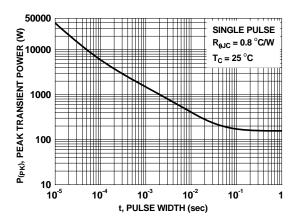


Figure 12. Single Pulse Maximum Power Dissipation



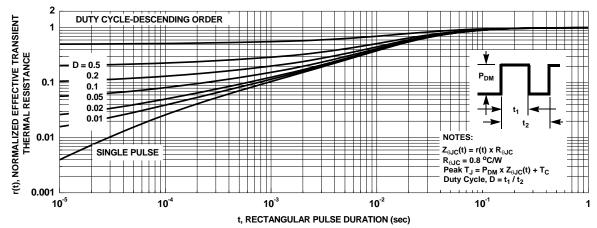
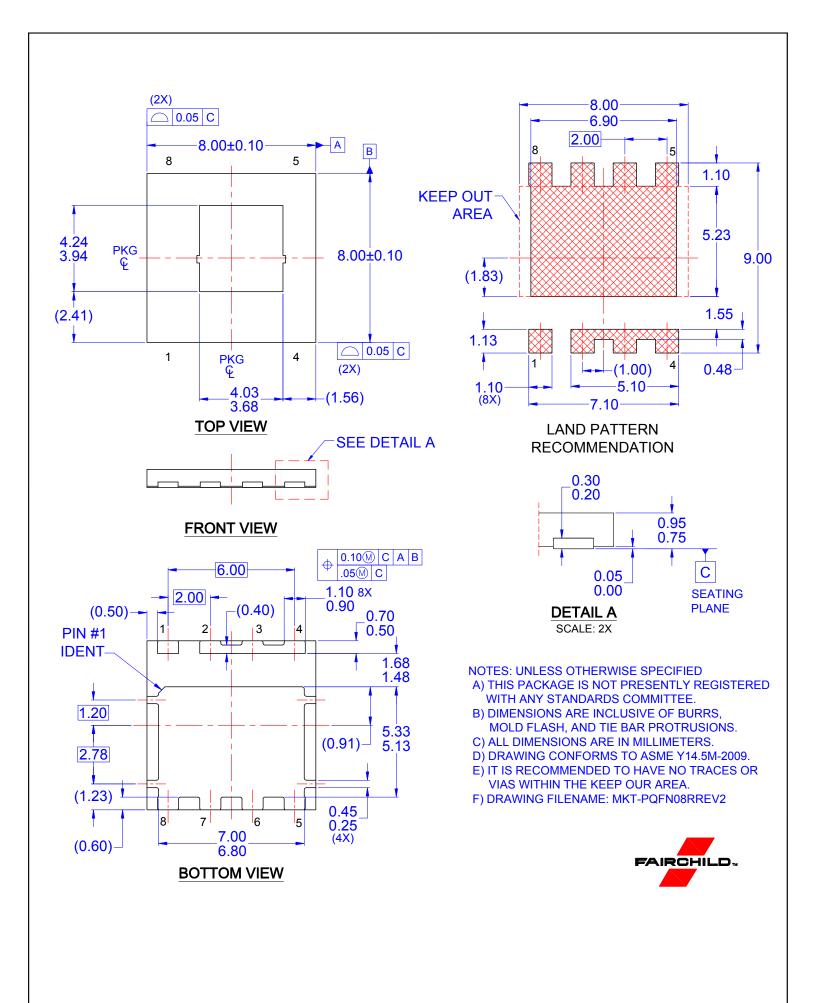


Figure 13. Junction-to-Case Transient Thermal Response Curve



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