32-Channel Serial To Parallel Converter With Open Drain Outputs

Features

- Processed with HVCMOS® technology
- Sink current minimum 100mA
- Shift register speed 16MHz
- Polarity and blanking inputs
- CMOS compatible inputs

Applications

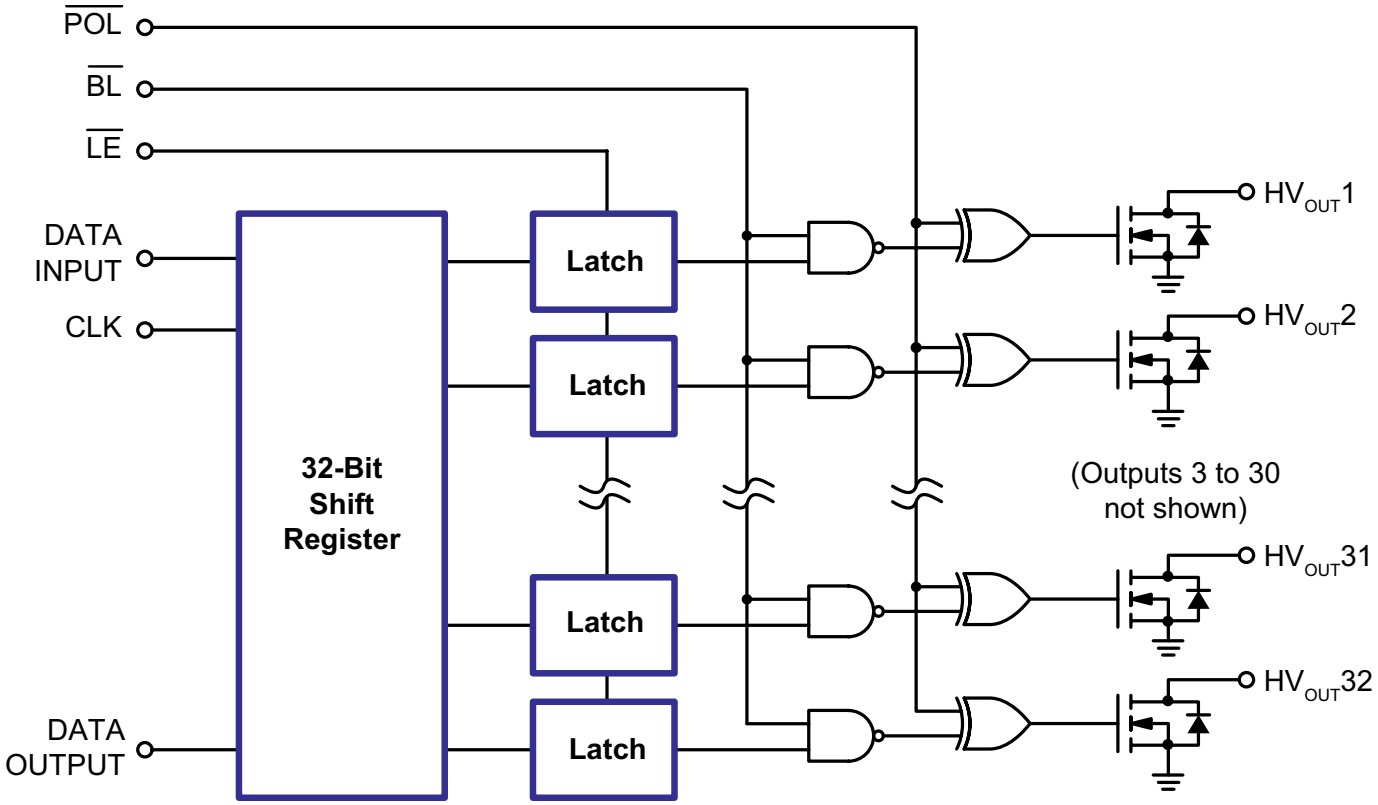
- Inkjet and Electrostatic Print Heads
- AC-Electroluminescent Displays
- MEMS Applications

General Description

The HV5623 is a low-voltage serial to high-voltage parallel converter with open drain outputs. This device has been designed for use as a driver for AC-electroluminescent displays. It can also be used in any application requiring multiple output high voltage current sinking capabilities, such as driving inkjet and electrostatic print heads, plasma panels, and vacuum fluorescent or large matrix LCD displays.

This device consists of a 32-bit shift register, 32 latches, and control logic to perform the polarity selection and blanking of the outputs. Data are shifted through the shift register on the high to low transition of the clock. The HV5623 shifts in a clockwise direction when viewed from the top of the package. A data output buffer is provided for cascading devices. This output reflects the current status of the last bit of the shift register. Operation of the shift register is not affected by the $\overline{LE}$ (latch enable), $\overline{BL}$ (blanking), or $\overline{POL}$ (polarity) inputs. Transfer of data from the shift register to the latch occurs when the $\overline{LE}$ (latch enable) input is high. The data in the latch is stored when $\overline{LE}$ is low.

Block Diagram

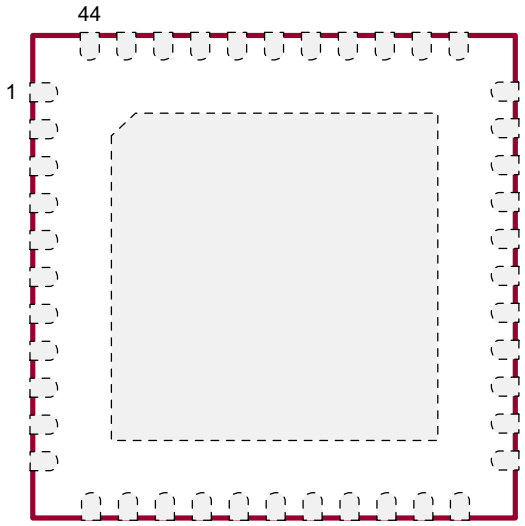


Ordering Information

Device	High Voltage Output HV_{OUT} *(max V)*	44-Lead QFN *7.00x7.00mm body, 0.80mm height (max), 0.50mm pitch*
HV5623	220	HV5623K7-G

-G indicates package is RoHS compliant ('Green')

Pin Configuration



44-Lead QFN (K7)
(top view)

Absolute Maximum Ratings

Parameter	Value
Supply voltage, V_{DD}[1]	-0.5V to +7.0V
Output voltage, HV_{OUT}[1]	-0.5V to +230V
Logic input levels[1]	-0.5V to V_{DD} +0.5V
Ground current[2]	1.5A
Continuous total power dissipation[3]	3.4W
Operating temperature range	-40°C to +85°C
Storage temperature range	-65°C to +150°C
Maximum junction temperature	+125°C
Thermal resistance (θ_{ja})[3]	29°C/W

Notes:

1. *Voltages are referenced to V_{SS}.*
2. *Duty cycle is limited by the total power dissipated in the package.*
3. *1.0oz 4-layer 3x4" PCB.*

Product Marking

L = Lot Number
YY = Year Sealed
WW = Week Sealed
A = Assembler ID
C = Country of Origin
____ = "Green" Packaging

Package may or may not include the following marks: Si or

44-Lead QFN (K7)

Operating Supply Voltages and Conditions

Sym	Parameter	Min	Typ	Max	Units	Conditions
V_{DD}	Logic supply voltage	4.5	-	5.5	V	---
HV_{OUT}	High voltage output	-0.3	-	+220	V	---
V_{IH}	High-level input voltage	$0.8V_{DD}$	-	V_{DD}	V	---
V_{IL}	Low-level input voltage	0	-	$0.2V_{DD}$	V	---
f_{CLK}	Clock frequency	-	-	16	MHz	---
T_A	Operating free-air temperature	-40	-	+85	°C	---

Notes:

Power-up sequence should be the following:

1. Connect ground.
2. Apply V_{DD}.
3. Set all inputs to a known state. Power-down sequence should be the reverse of the above.

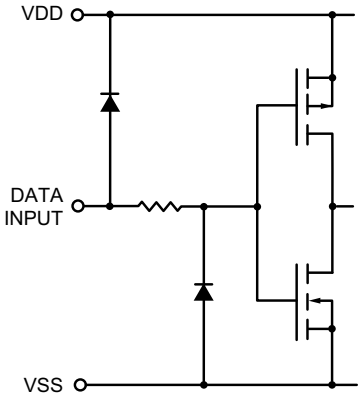
DC Electrical Characteristics *(Over operating supply voltages and temperature, unless otherwise noted)*

Sym	Parameter		Min	Typ	Max	Units	Conditions
I_{DD}	V_{DD} supply current		-	-	25	mA	f_{CLK} = 16MHz, f_{DATA} = 8.0MHz
I_{DDQ}	Quiescent V_{DD} supply current		-	-	100	µA	D_{IN} = 0V, all input logic pins = 0V, all outputs OFF
$I_{O(OFF)}$	OFF state output current		-	-	10	µA	All outputs high, all switches parallel
I_{IH}	High-level logic input current		-	-	1.0	µA	$V_{IH} = V_{DD}$
I_{IL}	Low-level logic input current		-	-	-1.0	µA	V_{IL} = 0V
V_{OH}	High level output		V_{DD} -1.0V	-	-	V	ID_{OUT} = -10mA
V_{OL}	Low level output	HV_{OUT}	-	-	15	V	IHV_{OUT} = +100mA
		DATA OUT	-	-	1.0	V	ID_{OUT} = +10mA
V_{OC}	HV_{OUT} clamp voltage		-	-	-1.5	V	I_{OL} = -100mA

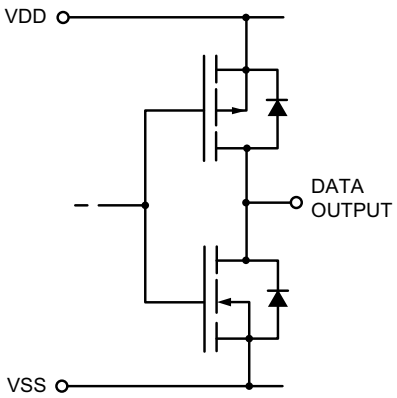
AC Electrical Characteristics *(V_{DD} = 5.0V, T_j = 25°C)*

Sym	Parameter	Min	Typ	Max	Units	Conditions
f_{CLK}	Clock frequency	-	-	16	MHz	---
t_W	Clock high / low pulse width	31	-	-	ns	---
t_{SU}	Data setup time before clock falls	25	-	-	ns	---
t_H	Data hold time after clock falls	10	-	-	ns	---
t_{ON}	Turn ON time, HV_{OUT} from Enable	-	-	400	ns	R_L = 2.0kΩ to V_{PP} max
t_{DHL}	Delay time clock to data high to low	-	-	35	ns	C_L = 15pF
t_{DLH}	Delay time clock to data low to high	-	-	35	ns	C_L = 15pF
t_{DLE}	Delay time clock to $\overline{LE}$ low to high	20	-	-	ns	---
t_{WLE}	Width of $\overline{LE}$ pulse	20	-	-	ns	---
t_{SLE}	$\overline{LE}$ set-up time before clock falls	20	-	-	ns	---
C_{IN}	Digital logic input capacitance	-	-	15	pF	---

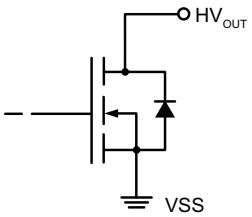
Input and Output Equivalent Circuits



Logic Inputs

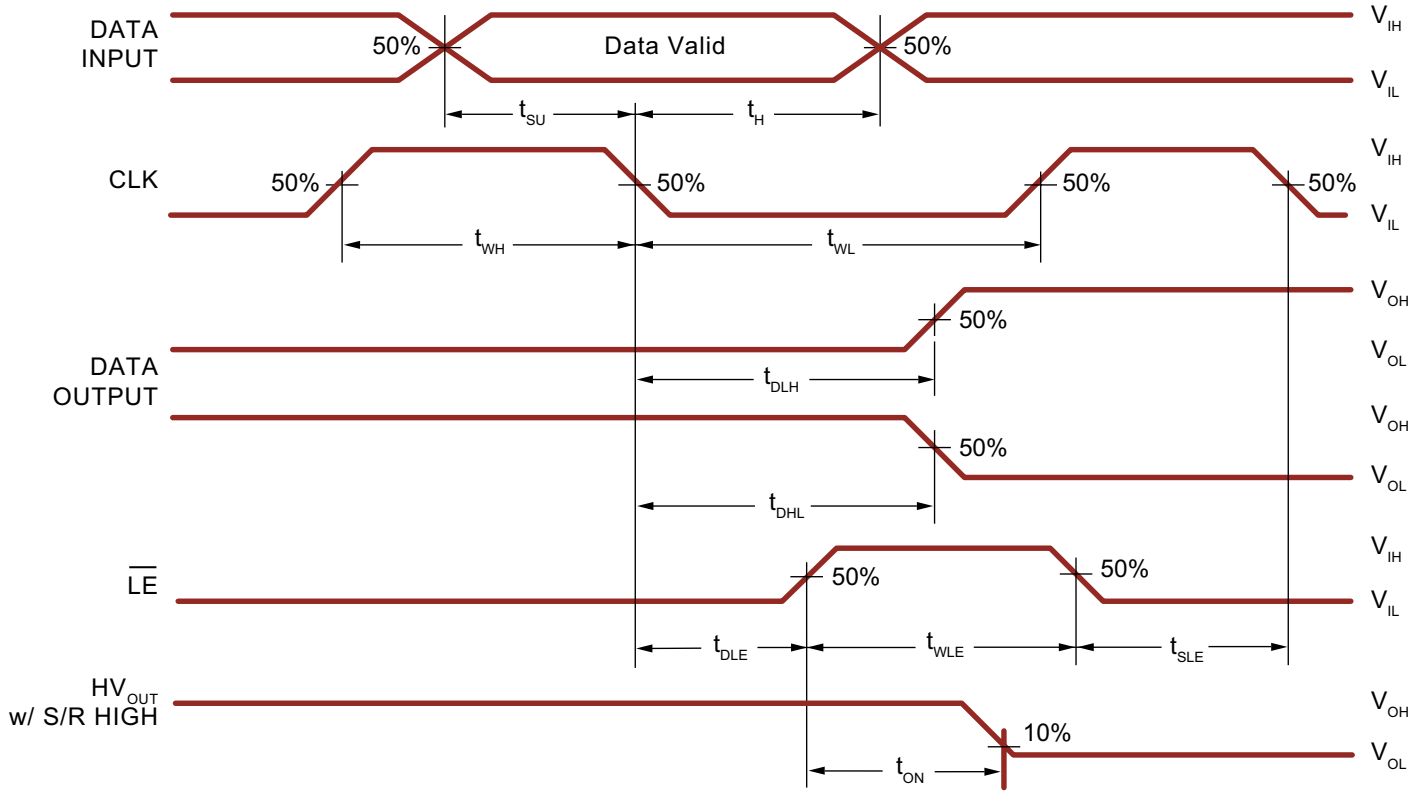


Logic Data Output



High Voltage Outputs

Switching Waveforms



Function Table

Function	Inputs					Outputs		
	Data	CLK	$\overline{LE}$	$\overline{BL}$	$\overline{POL}$	Shift Reg 1 2...32	HV Outputs 1 2...32	Data Out *
All ON	X	X	X	L	L	* *...*	ON ON...ON	*
All OFF	X	X	X	L	H	* *...*	OFF OFF...OFF	*
Invert mode	X	X	L	H	L	* *...*	$\overline{*}$ $\overline{*...*}$	*
Load S/R	H or L	↓	L	H	H	H or L *...*	* *...*	*
Load latches	X	H or L	↑	H	H	* *...*	* *...*	*
	X	H or L	↑	H	L	* *...*	$\overline{*}$ $\overline{*...*}$	*
Transparent latch mode	L	↓	H	H	H	L *...*	OFF *...*	*
	H	↓	H	H	H	H *...*	ON *...*	*

Notes:

H = high level, L = low level, X = irrelevant, ↓ = high-to-low transition, ↑ = low-to-high transition

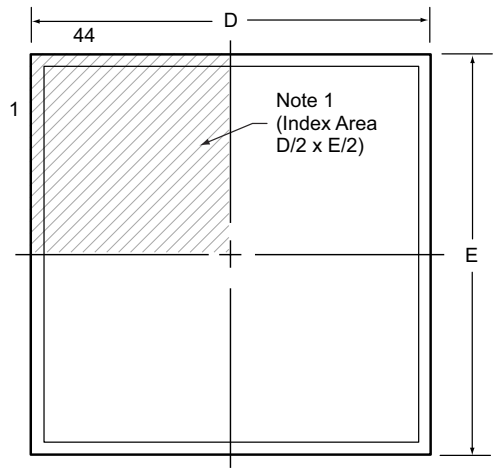
* = dependent on previous stage's state before the last CLK↓ or last $\overline{LE}$ high.

Pin Description

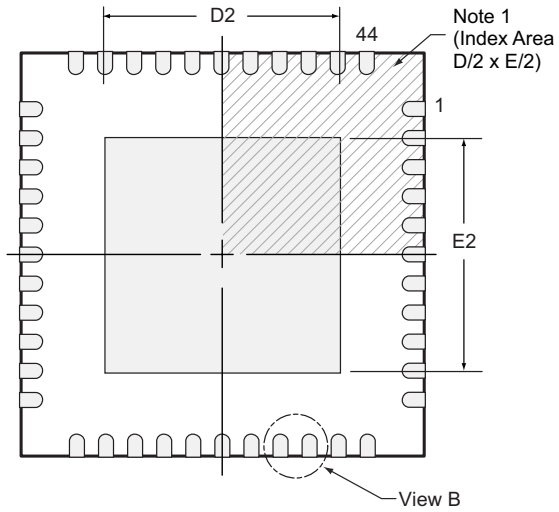
Pin #	Function	Description
1	$HV_{OUT}22$	High voltage outputs.
2	$HV_{OUT}21$	
3	$HV_{OUT}20$	
4	$HV_{OUT}19$	
5	$HV_{OUT}18$	
6	$HV_{OUT}17$	
7	$HV_{OUT}16$	
8	$HV_{OUT}15$	
9	$HV_{OUT}14$	
10	$HV_{OUT}13$	
11	$HV_{OUT}12$	
12	$HV_{OUT}11$	
13	$HV_{OUT}10$	
14	$HV_{OUT}9$	
15	$HV_{OUT}8$	
16	$HV_{OUT}7$	
17	$HV_{OUT}6$	
18	$HV_{OUT}5$	
19	$HV_{OUT}4$	
20	$HV_{OUT}3$	
21	$HV_{OUT}2$	
22	$HV_{OUT}1$	
23	DATA OUT	Data output pin.
24	N/C	No internal connection.
25	N/C	
26	N/C	
27	$\overline{POL}$	Inverts the polarity of the HV_{OUT} pins
28	CLK	Clock pin, shift registers shifts data on falling edge of input clock.
29	VSS	Reference voltage, usually ground.
30	VDD	Logic supply voltage.
31	$\overline{LE}$	Latch enable pin, data is shifted from shift register to latches on logic input high.
32	DATA IN	Data input pin.
33	$\overline{BL}$	Blanking pin sets all HV_{OUT} pins ON or OFF depending upon state of polarity. See function table.
34	N/C	No internal connection.
35	$HV_{OUT}32$	High voltage outputs.
36	$HV_{OUT}31$	
37	$HV_{OUT}30$	
38	$HV_{OUT}29$	
39	$HV_{OUT}28$	
40	$HV_{OUT}27$	
41	$HV_{OUT}26$	
42	$HV_{OUT}25$	
43	$HV_{OUT}24$	
44	$HV_{OUT}23$	
Center Tab		Connect to VSS

44-Lead QFN Package Outline (K7)

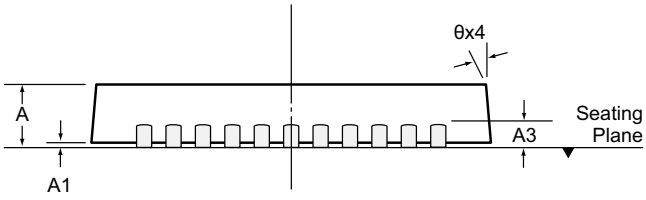
7.00x7.00mm body, 0.80mm height (max), 0.50mm pitch



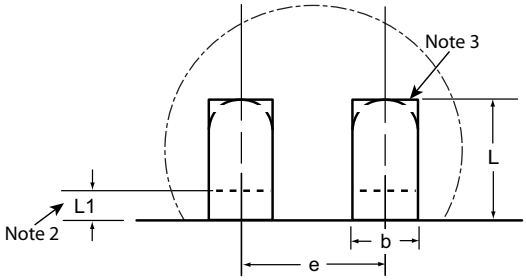
Top View



Bottom View



Side View



View B

Notes:

1. *A Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.*
2. *Depending on the method of manufacturing, a maximum of 0.15mm pullback (L1) may be present.*
3. *The inner tip of the lead may be either rounded or square.*

Symbol		A	A1	A3	b	D	D2	E	E2	e	L	L1	θ
Dimension (mm)	MIN	0.70	0.00	0.20 REF	0.18	6.85*	5.00†	6.85*	5.00†	0.50 BSC	0.45†	0.00	0°
	NOM	0.75	0.02		0.25	7.00	5.15†	7.00	5.15†		0.55†	-	-
	MAX	0.80	0.05		0.30	7.15*	5.25†	7.15*	5.25†		0.65†	0.15	14°

JEDEC Registration MO-220, Variation WKKD-3, Issue K, June 2006
** This dimension is not specified in the JEDEC drawing.*
† This dimension differs from the JEDEC drawing.
Drawings not to scale.
Supertex Doc. #: *DSPD-44QFNK77X7P050, Version A122309.*

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to http://www.supertex.com/packaging.html.)

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